EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH

CERN - SPS DIVISION

SPS/EBP/Note 79-17

IMPROVEMENTS ON XWCA / XWCM INTEGRATOR FOR USE AS BEAM INTENSITY MONITOR

P. Dreesen

Prévessin, 2 novembre 1979

CONTENTS

		Page
1.	INTRODUCTION	1
2.	STANDARD CIRCUIT	1
3.	LIMITATIONS OF THE STANDARD INTEGRATOR	3
4.	ANALYSIS OF THE PRESENT ELECTRONICS AND IMPROVEMENTS	4
	4.1 Offset at high measured charges	4
	4.2 Resolution of the electronics	4
	4.3 Memory	5
	4.4 Improved circuit	8
REFERENCES		9

1. INTRODUCTION

The Analog Wire Chambers XWCA and XWCM have proved to be a very useful instrument for beam tuning and monitoring, so that all charged secondary beams are equipped with them. They are described in Ref. 1 together with their electronics.

With the coming up of NAHIF beams, the problem of finding a reliable instrument for measuring beam intensities has been raised, and it has been suggested to use the XWCA for these purposes, either in the amplification or in the ionization mode (i.e. with the H.V. set at a value so low that the primary ionization is not amplified in the gas, the ions and the electrons are only collected at the electrodes; the gain G of the chamber is then = 1). The total beam intensity can be very easily obtained from a profile by adding, via software, the contents of the relevant channels.

Preliminary tests have been made by Henry W. Atherton in the M2 beam with the XWCM installed there, to see if the accuracy is good enough and if there appears to be problems. These tests lasted from June 1978 to the summer 1979, and improvements have been made to the electronics in order to correct for faults he noticed.

In the following we describe the principle of the measuring electronics, the actual circuit as it is installed on the chambers, its limitations, also in connection with the findings of H.W. Atherton and then a new circuit with improved performances.

2. STANDARD CIRCUIT

The physical basis of the measurement is the following :

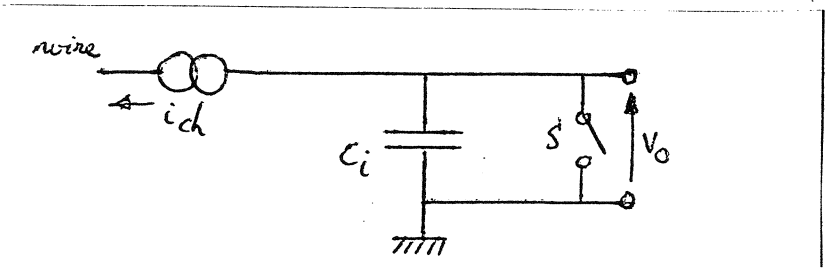

Fig. 1

Every wire of the chamber acts as a current source i_{ch} which is proportional to the beam intensity and to the chamber gain. The switch S is normally closed to ensure that the voltage across C_i is zero, before the beam arrives; then S is opened and the current from the wire is collected on C_i. At the end of the burst C_i has been charged by the integrated current coming from the wire, and by reading its voltage V_o with an ADC the total flux of particles across the sensitive region of the wire can be measured. After the measurement is made, S is closed again and C_i is discharged.

The actual implementation of the above circuit is the following :

The amplifier A serves the purpose of leaving the output voltage at the wire at about ground potential and instead putting V_o on the other side of the condenser, in order not to alter the operating voltage of the chamber.

with C_i : the integrating capacitor
S : the switch (MOS-FET)
i_s : leak current of the switch
C_m : memory capacitor
i_{ch}: current from the chamber

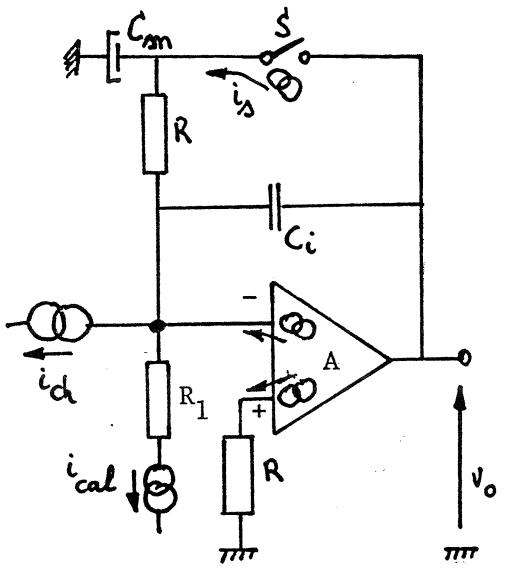

Fig. 2

The resolution of a normal integrator, defined by the leakage currents of the amplifier and of the switch, could be improved drastically by a system tested by M. Rabany, G. Vismara and the author. The system consists mainly in shunting into a large capacitor C_m the important leakage current of the switch i_s. The voltage on C_m is only slightly affected by i_s, and sends only a very little current into C_i. As a matter of fact, the compensation is a bit more complicated because it also takes into account the leak current of the amplifier. The resolution of the electronics becomes now of the order of 10 pC, after 1 sec. integration time (see Fig. 3), with the advantage of a good performance at a low price.

We can see the drift of the integrator when switch S is open. V_o < 10 mV after 1 sec on a 1 nF integrating capacitor $C_i \rightarrow Q_e$ < 10 pC

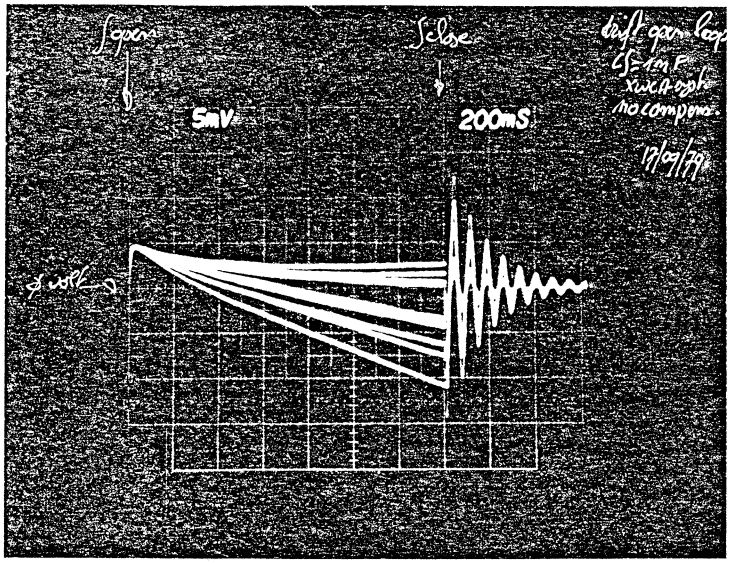

Fig. 3

The capacitor C_i converts charges to volts and it is chosen to match the expected current i_{ch} to be measured to the range of the ADC which measures V_o . The employed ADC has 10 bits and, in our case, spans a voltage range from 10 mV to 10 V.

3. LIMITATIONS OF THE STANDARD INTEGRATOR

The tests made by H.W. Atherton have been performed on chambers of the M2 beam, which was supposed to have the highest secondary beam intensity in the SPS. In view of this high intensity the capacitor C_i had the value of 100 nF, while for the normal XWCA it is only 3.3 nF.

The conclusions drawn were the following :

i) Offset : At high voltage and large charge in C_i , the chamber response seems to be linear with the beam intensity, at least for the limited swings in intensity which occurred during normal SPS operation. The linear relation is of the type XWCA = V_o + K × intensity

where V_o is an "offset" of the reading when extrapolating the linear relation to zero beam intensity.
This offset was however "charge dependent" in the sense that it was large when the chamber was operated at large collected charges and low for small collected charges.

ii) Resolution : At low voltage, and therefore small integrated charge, the chamber loses in accuracy. This is however compatible with the resolution of 1 ADC bit which corresponds to 10 mV at the output of the integration, being not negligible with respect to the actual reading.

iii) Memory : The chambers counted also during an empty SPS burst if this followed a normal beam burst.

Electronic tests have as a consequence been performed to see if the amplifier was responsible for these effects.

4. ANALYSIS OF THE PRESENT ELECTRONICS AND IMPROVEMENTS

4.1 Offset at high measured charges

This offset is most likely due to saturation of the chamber due to space-charge effects at high current, so that output charge is no longer proportional to beam intensity. The effect is only important for large currents on the wire : from measurements made we can set as a limit for linearity of a tested chamber the value of 1V on 100 nF, which corresponds to 10^{-7} Coulomb.

4.2 Resolution of the electronics

The resolution of 1 ADC bit is 10 mV, i.e. 10^{-9} C on C_i = 100 nF, whilst the intrinsic resolution of the electronics is of the order of a few times 10^{-11} C (more precisely 10^{-11} A in 1 sec; see Fig. 3, where 5 mV on C_i = 1 nF corresponds to 5 pC). By reducing by a factor 50 ÷ 100 the capacitor C_i it would be possible to better match the linearity region of the chamber to the ADC range.

Still, the 10^{-11} C resolution of the electronics, together with the 10^{-7} C limit of linearity of the chamber, leaves us a

10^4 range of linearity, which becomes a 10^2 range measured with 1 % precision. Any improvement on the resolution of the electronics - which is equivalent to the drift in Fig. 3 - would however result into an increase of the linearity region in the low current side, which is desirable. Any reduction of the drift would however necessarily imply a reduction of the leak current i_s or at least of its fraction flowing into C_i .

4.3 Memory

It turned out that the large effect noticed during the M2 measurement was partly due to an improper ground loop. This started however a search on possible memory effects on the electronics. In Fig. 4 the resetting is shown of the output voltage after a reading, and after closing the switch S . The system oscillates for 1.5 sec.

This is a picture of the oscillation of the voltage at the output. The switch S was closed after 1500 ms (V_o = 6 V at that moment) and on C_m the voltage is stabilised after another 1.5 sec but longer oscillations have been observed.

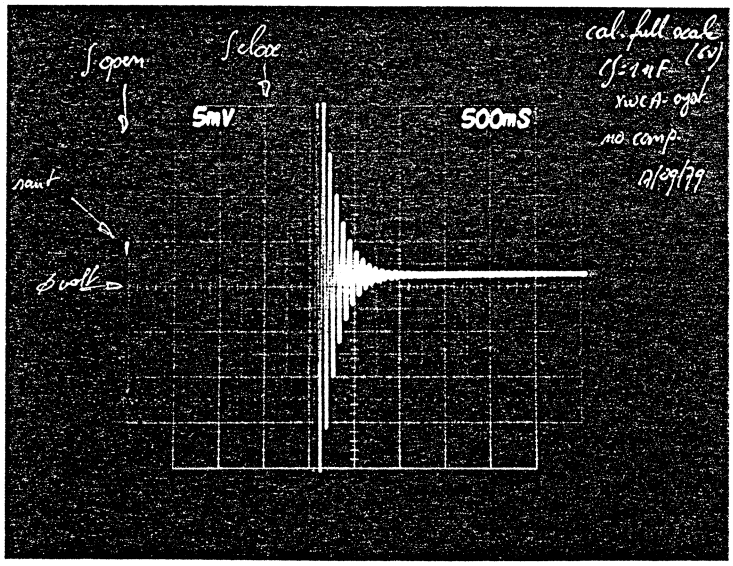

Fig. 4

The discharge circuit has therefore been modified (Fig. 5a)) in order to decrease this time: the new circuit is in equilibrium (Fig. 5b)) in 0.5 sec and the ringing after closing S has disappeared (Fig. 5c)).

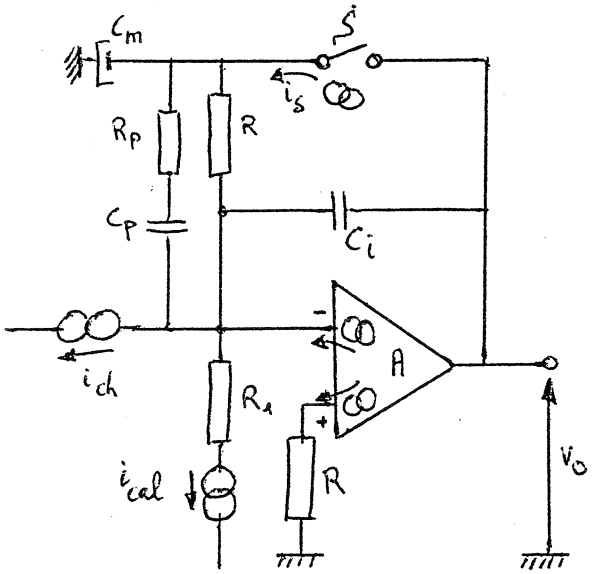

Fig. 5 a)

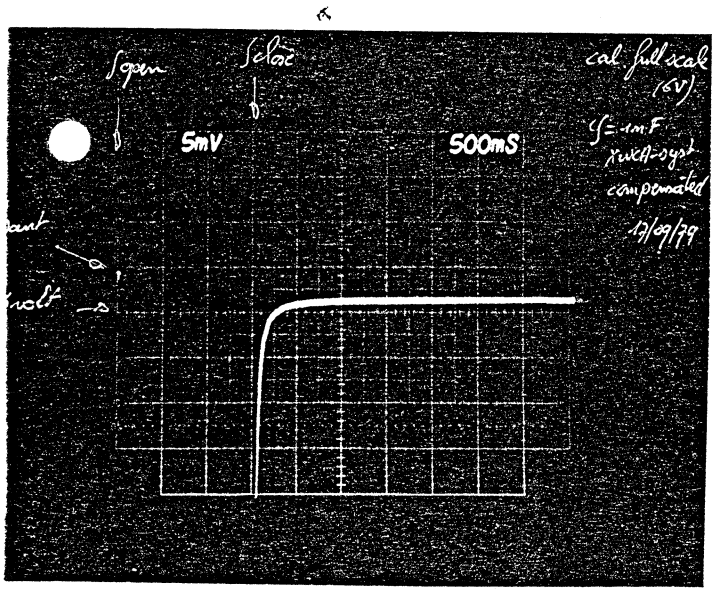

Fig. 5 b)

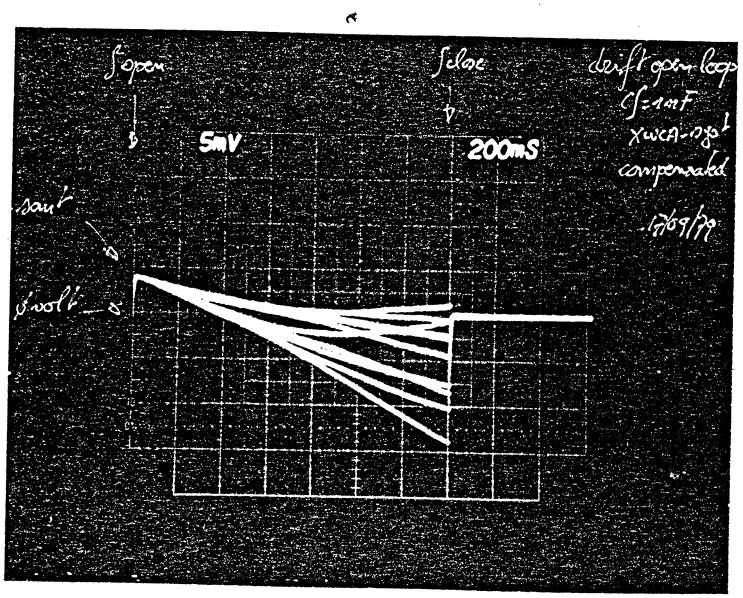

Fig. 5 c)

If, due to ageing or induced radioactivity, the chamber draws a dark current outside the burst, this current would change the voltage on C_m with S closed, proportionally to the value of the resistance R. This effect is shown in Fig. 6 where one can see the voltage on C_m for the 32 wires (in abscissa) of an old (Fig. 6a)) and of a new (Fig. 6b)) chamber.

This is what one can see when scanning the wires of an old XWCA and meanwhile rising the HT. The upper line is the dark current at about -4800 V on the chamber (10 µm Ø wires, 5 mm gap, 50 % Ar - 50 % CO_2 gas mixture)....

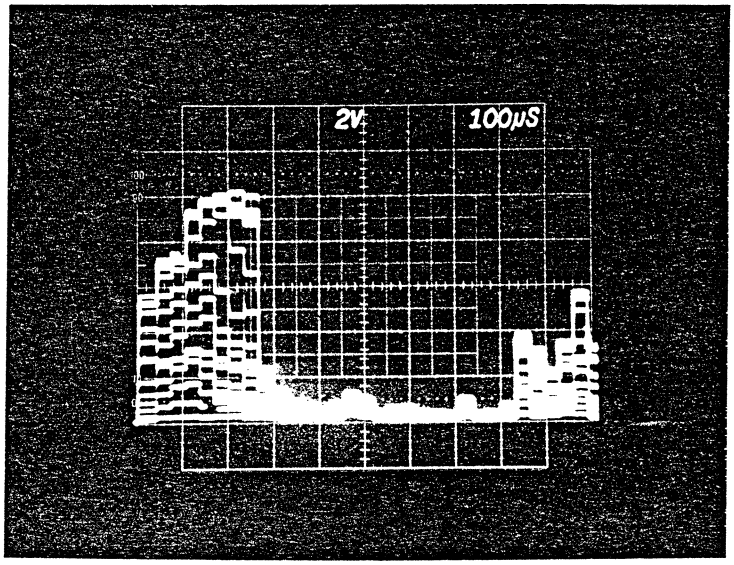

Fig. 6a)

... and this is a profile of the dark current of a new chamber in the same conditions

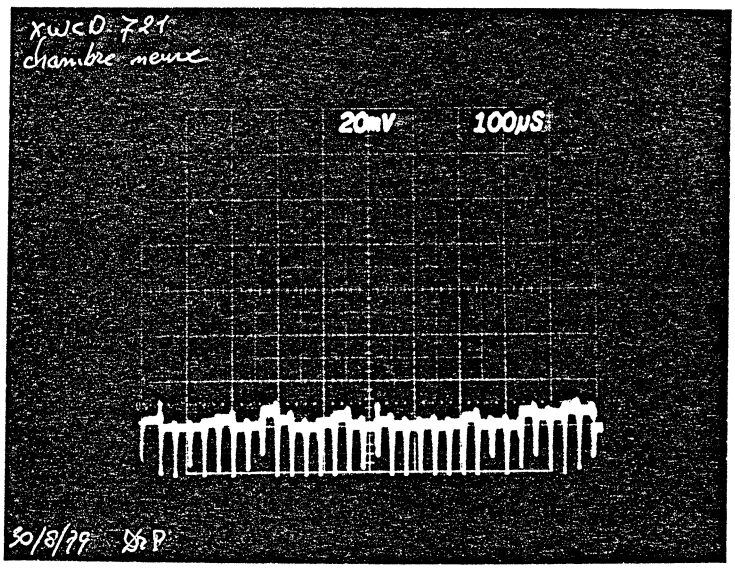

Fig. 6b)

If then we start a measurement with C_m charged, its charge will send a current through R into the integrator. C_m therefore acts as a memory of the dark current of the chamber.

4.4 Improved circuit

We have seen that the use of the system R - C_m for shunting the leak current i_s has some not negligible disadvantages, while reducing the leak current into C_i to still a few times 10^{-11} A.

We have been able to get rid of the condenser C_m and of the resistor R (see Fig. 7) by choosing adequate electronic components - as are the switch and the amplifier. This brings about several advantages.

An automatic offset and gain adjusting circuit are not represented on this scheme. Note the presence of C_i' to integrate the leak-current of the non-inverting input of the amplifier.

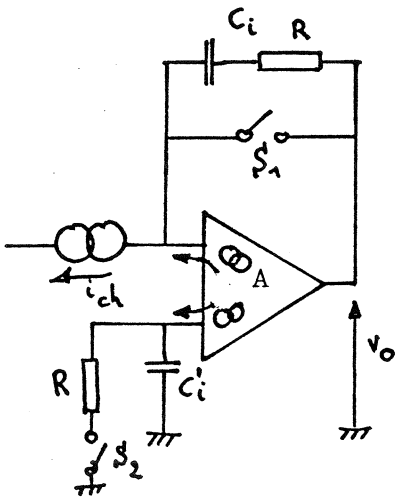

Fig. 7

In the first place, an important current from the chamber between bursts will not disturb the measurement anymore. Secondly, there is now the possibility of gating the integration time inside the burst. And thirdly it is possible to discharge C_i quickly and, as a consequence, to integrate several times between the beginning and the end of the extraction.

Getting rid of C_m has however not been done by letting a larger i_s flow into C_i. On the contrary the typical leak current into C_i is now of the order of 10 fempto-Ampère (10^{-14} A)/s, as can

be seen in Fig. 8, giving the integrator a resolution in the order of 10 femp to-Coul omb. This is a big improvement over the present situation, since it stretches the dynamical range of the actual integrator by a factor 10^3.

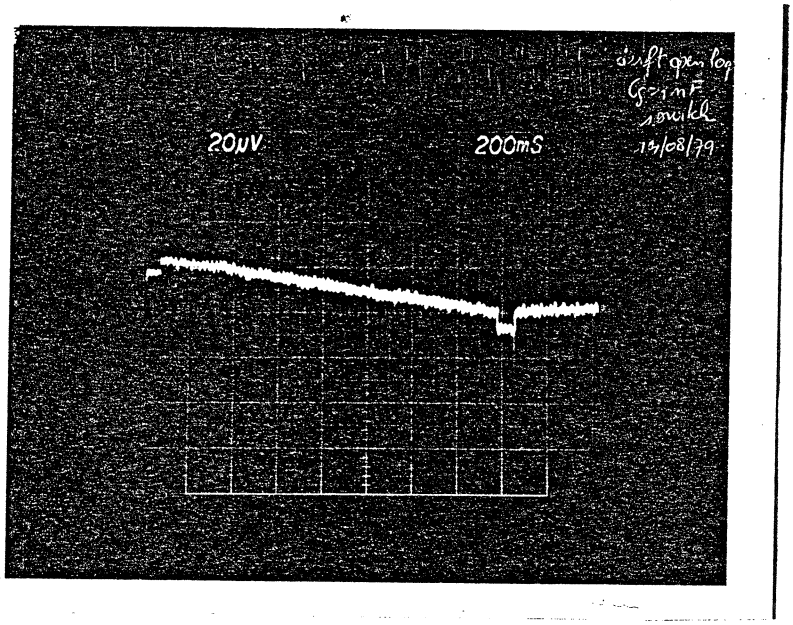

Fig. 8

Features of the prototype

- drift of the integrator : < 20 × 10^{-15} Coulomb per second with 10 m of coax cable (SCEM: 04.61.11.140) connected at the input;
- temperature drift : < 1 microV/^{o}C with unity-gain amplifier;
- good long-term stability (active compensation);
- output : 13 bits A/D convertion - 2's complement
  - pulse-train (1 MHz)
  - parallel-output with three-state logic

REFERENCES

1. P. Dreesen, G. Vismara, "Integrating wire chambers for beam tuning in the CERN SPS Experimental Areas", CERN-SPS/EA/78-4 (1.2.1978).