Global Trigger Versatile Module for ATLAS Phase-II upgrade

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on behalf of the ATLAS TDAQ Collaboration

***Abstract*– The ATLAS detector at the Large Hadron Collider will undergo a major Phase-II upgrade for the High Luminosity LHC. The upgrade affects all the main ATLAS systems including the Trigger and Data Acquisition. As part of the Level-0 Trigger System, the Global Trigger uses full-granularity calorimeter cells to perform algorithms, refines the L0Calo trigger objects and applies topological requirements. The Global Trigger uses an ATCA Global Common Module as the basis of its design. The additional, standalone, Global Trigger Versatile Module has been designed according to the prototype Global Trigger hardware specifications. The Global Trigger Versatile Module acts as an auxiliary hardware component that can be used for development, testing and operational purposes within and beyond the Global Trigger in projects requiring high bandwidth and processing capabilities. The Global Trigger Versatile Module hosts an advanced Xilinx Ultrascale+ VU13P FPGA and Finisar BOA optical modules running at data rates up to 25.8 Gb/s, as well as other hardware resources needed for the Global Trigger, located on a high-density PCB, optimized for high-speed data transmission. The Global Trigger Versatile Module successfully passed a full testing program, including verification of the main hardware functionality of the module, performance evaluation of the high-speed optical modules and the FPGA, and Global Common Module development firmware tests. Successful results demonstrating a good performance of the on-board components have been obtained.**

I. Introduction

The Global Trigger System is a part of the Phase-II upgrade of the ATLAS [1] Trigger and Data Acquisition (TDAQ) system [2]. It will replace the Phase-I Topological Processor [3] and extend its functions by using full-granularity calorimeter cells for refining the trigger objects calculated by the Level-0 Trigger System, performing offline-like algorithms, including iterative algorithms such as topoclustering, calculating event-level quantities and applying topological requirements (Fig. 1).

The Global Trigger is a time-multiplexed system, which concentrates the data of a full event into a single processor. The Global Trigger System is composed of three main layers: a Multiplexing (MUX) layer, a Global Event Processor (GEP) layer and a Demultiplexing layer, which implements an interface to the Central Trigger Processor (CTP) (Fig. 2).

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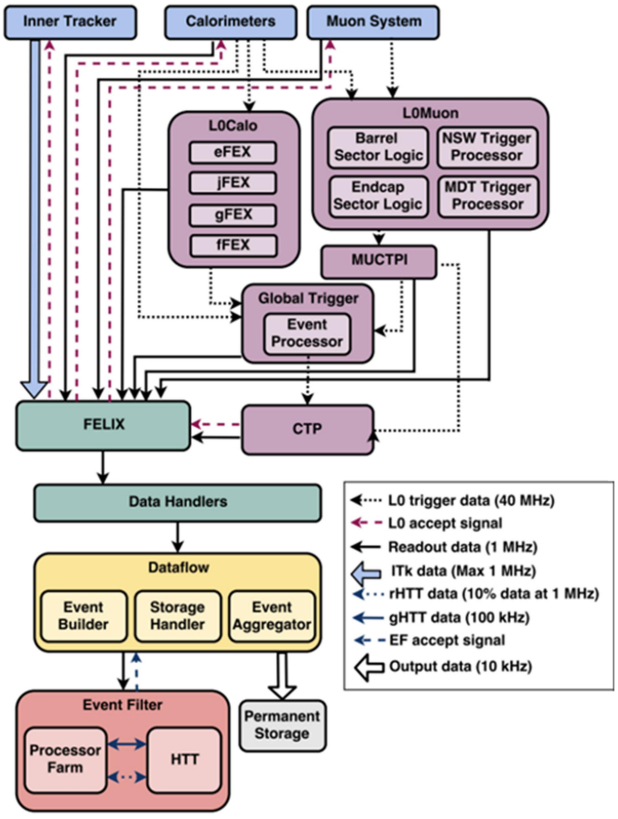

Fig. 1. TDAQ System after the Phase-II upgrade [2]. Receiving full-granularity calorimeter cells to refine L0Calo & L0Muon outputs, Global Trigger has a central location within the TDAQ System.

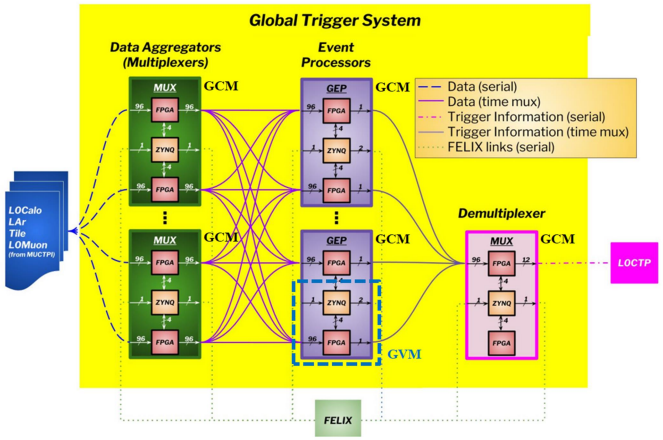

Fig. 2. Schematic view of the Global Trigger System [2] (in yellow), illustrating the detector inputs, multiplexing MUX layer, event-processing GEP layer, demultiplexing CTP Interface, and connections to other systems. GCM modules compose the hardware of the Global Trigger System. GVM module represents a slice of the GCM.

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The CTP takes the final trigger decision. The Global Trigger System accommodates more than 2300 input optical fibers with link speeds up to 25.8 Gb/s.

The basis of the Global Trigger is the Global Common Module (GCM) [4], a common hardware platform, which has to provide significant processing resources along with a high input and output bandwidth. GCM modules compose the hardware of every layer of the Global Trigger System. In total 50 GCMs are foreseen to be used within the Global Trigger. Various link speeds, including high-speed links up to 25.8 Gb/s, should be supported. The high-speed link support is essential in order to cope with the transmission of high-granularity calorimeter data which drives the bandwidth requirement for the upgraded TDAQ system.

An additional Global Trigger Versatile Module (GVM) has been designed according to the prototype Global Trigger hardware specifications. The GVM represents a slice of the GCM and can emulate a MUX or GEP. It hosts the new generation of optical modules and Field-Programmable Gate Arrays (FPGA) running at the required data rates, as well as other hardware resources needed for the Global Trigger, and acts as an auxiliary hardware component that can be used for development, testing and operational purposes within and beyond the Global Trigger in projects requiring high bandwidth and processing capabilities.

II. Board Overview

The GVM is designed in an ATCA form factor with the possibility of a standalone operation (Fig. 3). The main building blocks are the following: one large processing FPGA (Xilinx Ultrascale+ VU13P [5]), up to eight Finisar Board-Mount Optical Assembly (BOA) modules [6] for real-time data path, one Finisar BOA module for interface to Front-End Link eXchange (FELIX) system, one UltraZed board with Zynq UltraScale+, one IPM Controller (IPMC), one FPGA power mezzanine and two DDR4 RAMs. Dedicated clock distribution circuits are implemented as well in order to provide reference clocks for the multi-gigabit transceivers of the FPGA.

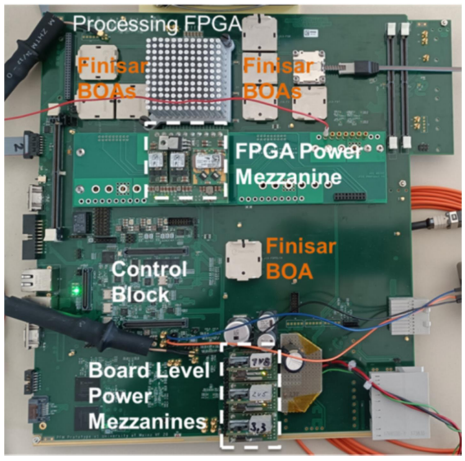


Fig. 3. GVM hardware top view with the most important building blocks labeled.

The detailed block diagram in Fig. 4 shows the multi-gigabit transceiver connections of the processing FPGA on the GVM.

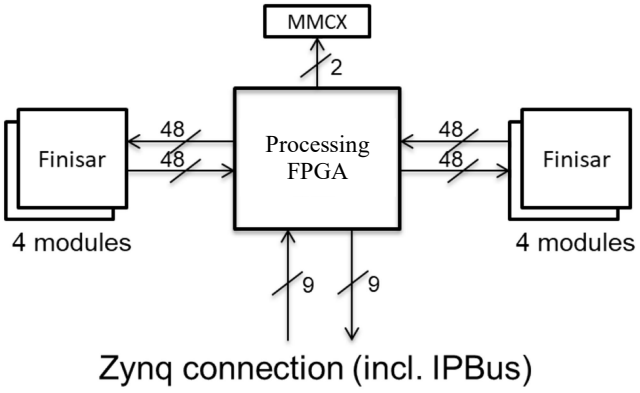


Fig. 4. Block diagram of the multi-gigabit transceiver connections of the processing FPGA on the GVM.

The design choice of Finisar BOA optical modules was possible thanks to the evaluations performed with the Global Trigger Technological Demonstrator [7].

IPBus is a protocol that runs over Ethernet to provide register-level access to hardware. The GVM provides IPBus functionality for high-level, functional control. This allows, for example, algorithmic parameters to be set, modes of operation to be controlled, spy memories to be loaded for playback and spy memories to be read.

The complete floor plan of the processing FPGA can be seen in Fig. 5. "OM" corresponds to Optical Module connection. Connections to a single optical module are grouped with braces. Connections to the SoC and DDR4 RAMs are shown as well as IPBus and dedicated MMCX lines for debugging purposes.

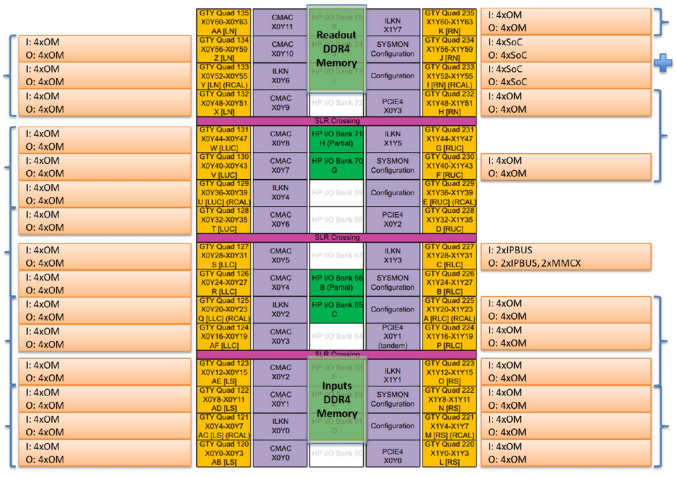


Fig. 5. The floor plan of the Processing FPGA of the GVM.

Two primary clock trees are implemented on the board, one crystal-based to support asynchronous high speed lines running at 25.78125 Gb/s, another based on the recovered LHC clock for synchronous links. The LHC clock is provided

by FELIX and the signal is recovered with the help of the control FPGA and distributed to one of the inputs of the jitter cleaner chip Si5345 placed on the main board. A dedicated local clock oscillator is used for the recovery of the system clock. A chain of fanout chips takes care of the recovered system clock distribution to the processing FPGA as well as back to the control FPGA. A corresponding block diagram can be seen in Fig. 6.

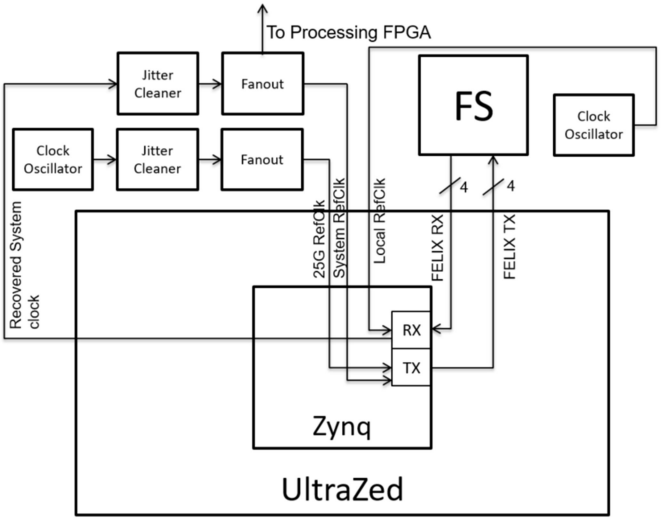


Fig. 6. Clock distribution for FELIX interface.

The default input of the Si5345 uses the recovered system clock. All the main reference clock trees are derived from the jitter cleaner outputs. Additionally, one local crystal and two SMA connectors (differential input) are connected to the remaining inputs of the jitter cleaner (Fig. 7). A backplane (Zone 2) clock connection is available as well.

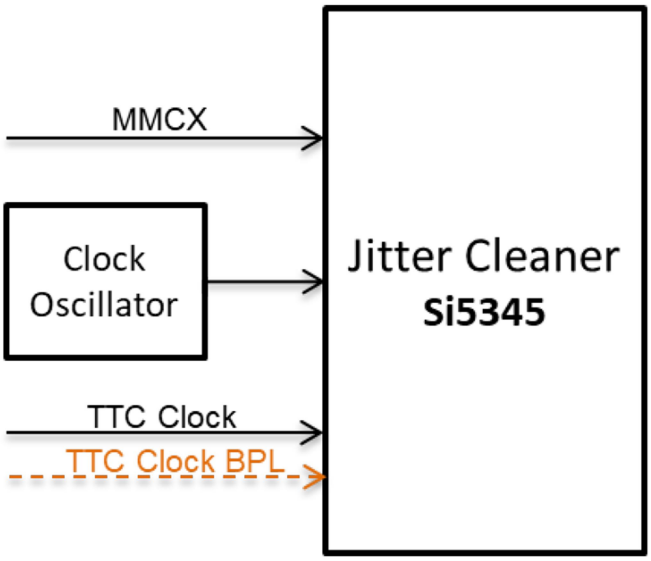


Fig. 7. Jitter Cleaner's input options.

From its inputs the PLL chip within the jitter cleaner can generate clocks of various multiples of the input frequencies. This flexibility allows the multi-Gb/s links on the GVM to be driven at a large range of different rates. The Si5345 settings are accessible via I2C.

Various reference clock trees, shown in Fig. 8, are implemented on the GVM, including two full MGT reference clock trees (for receivers and transmitters) and a partial MGT reference clock tree specifically for additional synchronization options between the processing and the control FPGAs. Two dedicated IPBus reference clock trees are also implemented. A global clock tree is present as well in order to synchronize programmable logic between the processing and the control FPGAs.

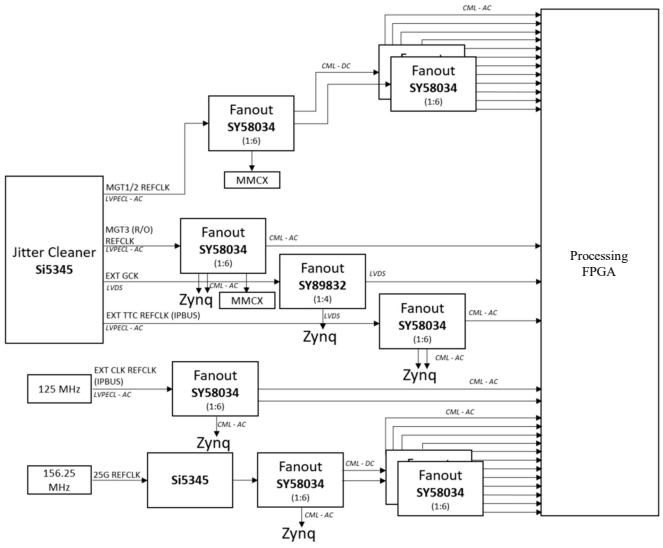


Fig. 8. Clock trees of the GVM.

The MGTs reference clock scheme is designed to minimize the number of signals routed on the PCB. Additionally, following constraints are respected:

- The reference clocks for a QUAD can be sourced from up to two QUADs below or above for slower data rates (below 16.375 Gb/s) [8]
- From up to one QUAD below or above for faster data rates (16.375 – 28.21 Gb/s)
- No crossing of clocking signals between different SLRs is allowed

The IPbus module control can either run from an on-board 125 MHz crystal clock, or from an output of the Si5345 chip. This allows the GVM module control function over IPBus to be independent or not from the system clock.

The control block is a mezzanine that provides many of the (non-real-time) services required on the GVM. It hosts mainly module control, clock/control and configuration circuitry. It also provides initialization circuitry for the FPGA and acts as an interface to environmental monitoring devices. Interface to FELIX (incl. TTC clock recovery) is implemented as well.

The "intelligent" module controller is a SoC which handles incoming IPbus requests and forwards the data and control packets to the processing FPGA via MGT links.

The configuration of the processing FPGA is controlled from the control block. To that end all control signal lines

required are routed between the module controller and the control block.

A JTAG chain, dedicated for configuration and testing of the processing and control FPGA, is implemented as well.

Environmental data (voltages, currents, temperatures) are collected on the board by I2C based sensors, and routed to the control block via the bidirectional I2C buses. Parameters in the respective devices are set via I2C as well. Data are originating from dedicated monitoring chips, or from monitor/control interfaces available in core functionality devices, e.g. BOAs. They are routed into the module controller with an optional breakout onto headers. The module controller allows for access to these data via IPbus. The status/control data exchanged that way are complementary to the IPMC data.

The IPBus communicates with its control PC(s) via an Ethernet PHY chip.

The detailed block diagram in Fig. 9 shows the multi-gigabit transceiver connections of the control FPGA on the GVM.

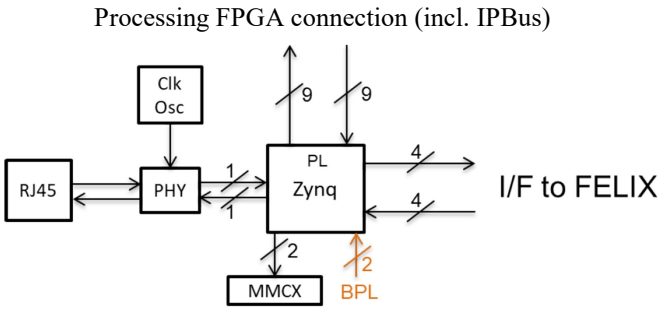


Fig. 9. MGT connections on the control FPGA of the GVM.

III. High-speed PCB design considerations

Dedicated high-speed PCB design routing techniques are used in order to optimize the signal integrity for the high-speed signals between the FPGA and optical modules as well as other high-speed components.

Thus, all the high-speed differential pairs adhere to strict physical and spacing constraints. Phase tuning is performed in order to stay within the phase tolerance limit. Appropriate in-pair spacing and trace width provide the 100 Ohm ± 10% differential impedance, while sufficient spacing across all pairs (4 times larger than the in-pair spacing) minimizes the crosstalk. Each high-speed signal trace is routed entirely on a single internal layer, apart from the transition areas between the outer and the inner layers, where ground vias are used in order to improve the signal integrity. The in-pair spacing is constant over the entire trace length.

Moreover, the stack-up (Fig. 10) is designed in such a way as to provide good signal integrity for high-speed signals. Signal planes are shielded by the ground planes, thus minimizing the crosstalk. For example, layers 2, 4 and 6 are ground layers dedicated to shield high-speed links to optical modules. High-speed signals occupy the top and bottom inner layers, and use microvias in order to avoid stubs on the signal lines. For example, layers 3 and 5 are dedicated for high-speed links to optical modules. Buried vias are used as well in order to provide a better connection between the top and the bottom microvia layers.

Ultra-low transmission loss and highly heat resistant PCB material (MEGTRON6 [9]) is used for the PCB due to its good dielectric constant and dissipation factor for high frequencies.

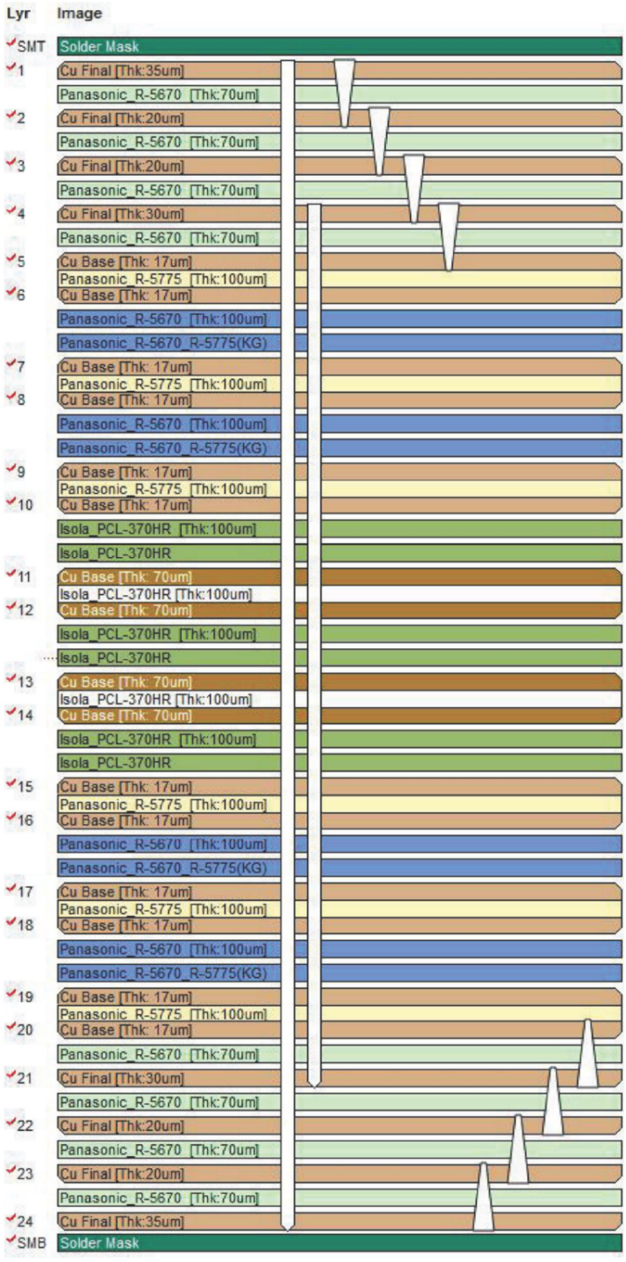


Fig. 10. Global Trigger Versatile Module stack-up. 24 layers in total. Layers 3 and 5 dedicated for high-speed links to optical modules. Layers 2, 4 and 6 are ground layers dedicated to shield high-speed links to optical modules.

IV. Performance Evaluation

The main hardware functionality of the module including power, clock trees, JTAG chain, main processing FPGA and control block has been verified.

Achieving a good performance of the high-speed optical modules and the FPGA poses the biggest challenge for the board design. The following long-run link tests have been carried out in order to evaluate this performance. An Integrated Bit Error Ratio Test (IBERT) loopback test has been performed for the Finisar BOA optical module. The optical channels of the module are grouped into two separate 12-lane rows compatible with a standard 2x12 bare MT ferrule. The first row contains all the receiver lanes, the second row all the transmitter lanes. Thus, in the test it was possible to loop 12 transmitter links of the optical module back to 12 receiver links of the same module with a help of a "24 to 2x12-fiber" Y-cable and a 12-fiber trunk cable (Fig. 11).

An IBERT test run at 25.78125 Gb/s, using a 31-bit PRBS pattern, has been performed. All 12 links are functional, and no bit errors have been detected (Fig. 12), measuring the BER down to $4.9 \cdot 10^{-15}$.

A typical eye diagram, obtained using a low power mode of the GTY receiver, is shown in Fig. 13. With an open area of 8712, a good performance of the Finisar BOA optical module is achieved.

Eye diagrams for other 11 optical links show a good eye-opening and overall good performance of the optical module as well (Fig. 14).

V. Firmware Tests

The GVM is available to developers and is currently in use for GCM firmware testing and development. For example, several tests for the topoclustering algorithm firmware, integrated into a custom firmware framework, have been performed.

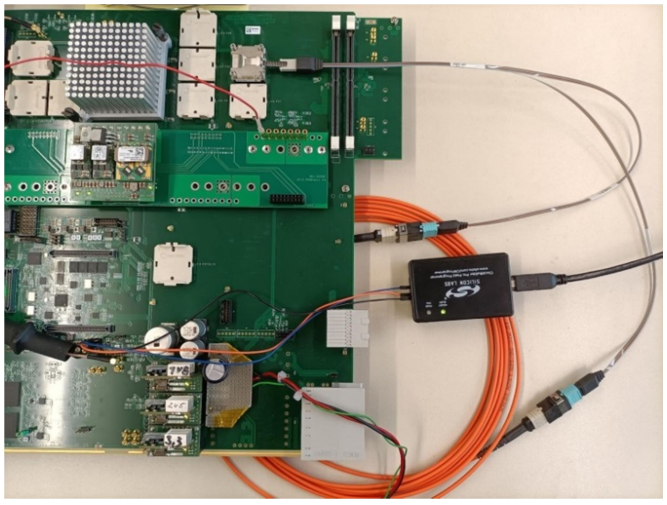
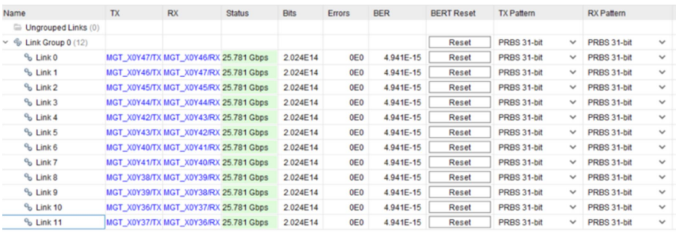


Fig. 11. Finisar BOA IBERT loopback test: test setup. BOA optical module mounted on the GVM as well as the "24 to 2x12-fiber" Y-cable and the 12-fiber trunk cable are shown.



Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern
Ungrouped Links (0)									
Link Group 0 (12)							Reset	PRBS 31-bit	PRBS 31-bit
Link 0	MGT_X0Y47/TX	MGT_X0Y46/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 1	MGT_X0Y46/TX	MGT_X0Y47/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 2	MGT_X0Y45/TX	MGT_X0Y45/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 3	MGT_X0Y44/TX	MGT_X0Y44/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 4	MGT_X0Y42/TX	MGT_X0Y43/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 5	MGT_X0Y43/TX	MGT_X0Y42/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 6	MGT_X0Y40/TX	MGT_X0Y41/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 7	MGT_X0Y41/TX	MGT_X0Y40/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 8	MGT_X0Y38/TX	MGT_X0Y39/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 9	MGT_X0Y39/TX	MGT_X0Y38/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 10	MGT_X0Y36/TX	MGT_X0Y37/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit
Link 11	MGT_X0Y37/TX	MGT_X0Y36/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit

Fig. 12. Finisar BOA IBERT loopback test: links status. "Status" column shows the link data rate, green background indicates that the link is functional. "Errors" column indicates the absence of errors.

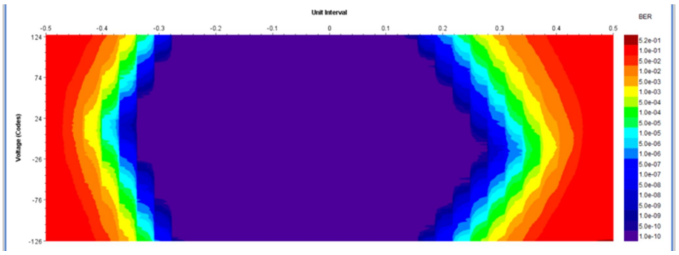


Fig. 13. Finisar BOA IBERT loopback test: a typical eye diagram. Open area: 8712 @ 25.8 Gb/s.

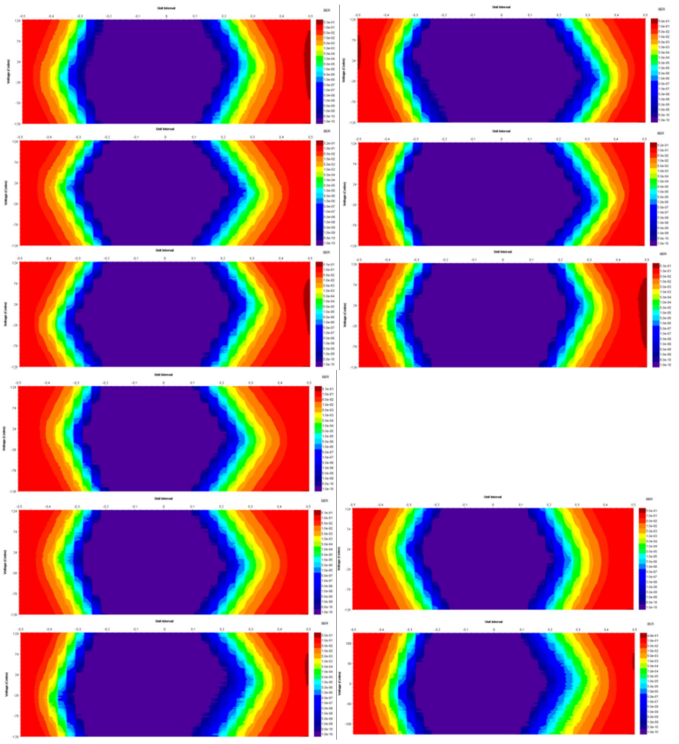


Fig. 14. Finisar BOA IBERT loopback test: eye diagrams for the rest of the optical links.

VI. Conclusion

A Global Trigger Versatile Module has been designed according to the prototype Global Trigger hardware specifications, hosting the new generation of optical modules (Finisar BOA) and FPGA (Xilinx Virtex UltraScale+ 13P) running at high data rates up to 25.8 Gb/s, as well as other hardware resources needed for the Global Trigger. The main hardware functionality of the module including performance

of the high-speed optical modules and the FPGA has been successfully evaluated. GCM development firmware tests are currently being performed on the GVM. Advanced hardware resources make the Global Trigger Versatile Module a valuable hardware component that can be used for development, testing and operational purposes within and beyond the Global Trigger in projects requiring high bandwidth and processing capabilities.

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