Performance of ALTIROC2 readout ASIC with LGADs for ATLAS HGTD picosecond MIP timing detector

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ABSTRACT: ALTIROC2 is a 225-channel ASIC designed in CMOS 130 nm to read out the 15 x 15 matrix of 1.3 mm x 1.3 mm Low Gain Avalanche Diodes (LGAD) of the ATLAS HGTD (High Granularity Timing Detector). The targeted combined time resolution of the sensor and its readout electronics from 35 ps/hit (initial) to 65 ps/hit (end of operational lifetime). Each ASIC channel integrates a high-speed preamplifier followed by a high speed discriminator and two TDCs for Time-of-Arrival and Time-Over-Threshold measurements as well as a local memory. This front-end must exhibit an extremely low jitter noise while keeping a challenging power consumption of less than 4.5 mW per channel. This conference proceeding summarizes the ASIC architecture, its measured performances compared to simulation, along with the requirements for the ATLAS HGTD experiments.

KEYWORDS: LGAD; ATLAS; HGTD; ASIC; picosecond

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1. Introduction

At CERN, the ATLAS experiment is preparing the next phase upgrade, where the average number of simultaneous interactions is expected to reach 200 [5].With this new pile-up conditions, the particle tracking becomes increasingly challenging. But because primary vertices where particles originate are close in space but separated in time, pile-up effects can be mitigated thanks to an accurate time measurement. Therefore, a new detector (HGTD) has been proposed to cover the forward region, with both timing and luminosity measurement capabilities.
Low Gain Avalanche Diodes have been chosen for their very good timing resolution in harsh irradiation conditions. [4] These sensors are 1.3 mm x 1.3 mm with a thickness of 50 µm. The thickness trade-off allows optimal drift time, collected charges and low capacitance. The detector capacitance is critical for the analog front-end performance, given its influence on the jitter and thus the time resolution of the full detector. Each silicon-based sensor will be bump-bonded onto two ASICs, and placed on both sides of a cooling plate. An overlap is introduced so each track registers at least two hits on average when going through the detector.

ALTIROC (Atlas Timing Read-Out Chip) design is led by time performances. In particular, the main sizing criterion is the timing resolution for a 4 fC charge that corresponds to the sensor MIP after irradiation. The total hit jitter (1) obtained for one particle interaction with the detector, is the root mean square of three contributions: the jitter from the sensor, also called Landau noise and the electronic jitter. [5]

$$\sigma_{hit}^2 = \sigma_{Landau}^2 + \sigma_{elec}^2 \quad (1)$$

The latter can be broken down again into a quadratic sum between the contribution due to the clock jitter, the time walk (which will be explain latter), the jitter due to the electronic noise of analog front-end [3] and the accuracy of the Time-to-Digital Converter (TDC, which is usually negligible compared to the other terms).

$$\sigma_{elec}^2 = \sigma_{clock}^2 + \sigma_{time\ walk}^2 + \sigma_{analog\ front-end}^2 + \sigma_{TDC}^2 \quad (2)$$

The main challenge in designing the front-end is to achieve low jitter, even while collecting only 4 fC charge from the sensor. As shown in (3) from reference [3], the jitter is dominated by the sensor characteristics.

$$\sigma_{analog\ FE} = \frac{Noise}{dV/dt} = \frac{e_n C_d \sqrt{t_d}}{Q_{in}} \quad (3)$$

With

e_n: Noise spectral density of the input transistor
C_d: Sensor capacitance (around 4 pF expected)
t_d: LGAD drift time (600 ps)
Q_{in}: MIP collected charge (10 /4 fC at the start/end of the detector lifetime after 200 MRad)

According to the formula (3), the noise spectral density e_n should be kept as low as possible, since the jitter follows mainly imposed parameters derived from the sensor. Table I below details the detector requirements in terms of timing constraints, noise performances, detectable charge, irradiation tolerance, and power dissipation.

2. Front-end architecture

ALTIROC2 is a first full size prototype that integrates a matrix of 15x15 channels with all the required analog and digital features. Each pixel includes a high-speed preamplifier followed by a discriminator, two TDC, and one local memory (SRAM). The ASIC is able to provide both measurements of Time-Of-Arrival (TOA) with a bin size of 20 ps, on a range of 2.5 ns (encoded on 7 bits) and Time-Over-Threshold (TOT) with a bin size of 160 ps, on a range of 20 ns (encoded on 8 bits). TOA and TOT measurements are used to perform time walk correction offline. Concatenated, the time information (Hit data) makes up 19 bits stored in the 38 µs depth-SRAM (with zero supress) until retrieval by the L1 trigger (1 MHz).

3. Testbench measurements

ALTIROC2 was tested ASIC alone and bump-bonded onto the sensor to allow tests with pion beam test campaigns. In order to test the analog part without test beam facilities, the ASIC includes a controlled internal calibration pulser. It simulates charge injections from 0 up to 100 fC by applying a voltage step through a capacitor at the preamplifier input. The test system integrates a tunable capacitor (Cd) that emulates the detector capacitance. Further details can be found in [2].

3.1 Minimum charge detectable

ALTIROC2 has proved capable to detect charges as low as 1.4 fC when only one out of the 15 columns is enabled. Nevertheless, the minimum detectable charge increases when all the 15 columns are enabled, as detailed in Table II. Static IR drops have been identified as responsible for shifting up the local analog ground, hence affecting the calibration pulse amplitude and the local threshold.

TABLE II. MINIMUM DETECTABLE CHARGE

Number of analog front-end column enabled	One column	All columns
ASIC alone irradiated up to 220 Mrad	1.4 fC	3.1 fC
Sensor (LGAD) + unirradiated ASIC	2.9 fC	3.8 fC

Furthermore, when bump-bonding the sensor onto the ASIC, the minimum detectable charge also increases. This effect can be explained by the ground impedance between the sensor and preamplifier. For one single channel, the differences between ASIC alone or with ASIC bump bonded onto a sensor are modelized on the following figure. On one hand, when the ASIC is alone, a sensor-like internal capacitor is used to emulate the LGAD capacitance and placed between the transistor input pad and the analog ground of the preamplifier. The ASIC to PCB wire bonding is represented here as a parasitic inductance. Any noise injected at the analog ground – whatever the origin – is seen by both preamplifier inputs to first order and therefore not amplified by the preamplifier.

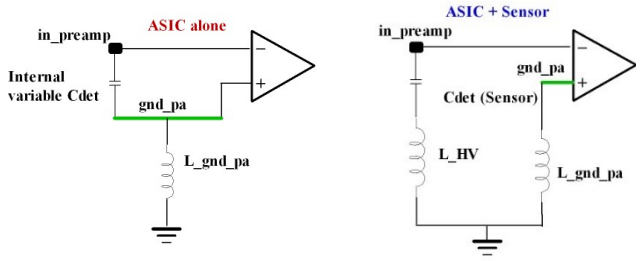

Figure 1: Sensor to preamplifier connections with the ASIC alone versus with a sensor

On the other hand, when the sensor is bump bonded to the channel input and biased by the external high voltage power supply, the grounding scheme changes. Indeed, the sensor biasing is achieved using wire-bonding and offers an AC-current path to ground through external high voltage capacitors. Both the sensor and the preamplifier are then connected to the same ground, but through parasitic inductances. Any noise injected inside the ASIC on the preamplifier ground is then amplified similarly as a detector signal, with the preamplifier acting as a differential mode gain stage. It therefore explains the minimum detectable charge shift observed with a bump bonded sensor. With the sensor, the slope of the trigger efficiency versus the charge at 50% detection is slower compared to the ASIC alone.
A minimum detectable charge reduction strategy can nevertheless be used, leveraging on the noise periodicity. As observed on the scope, when probing the preamplifier output, the noise ripple resembles an 80 MHz sine wave. Moreover, the ripple phase can be delayed thanks to the ASIC internal phase shifter over the full bunch-crossing clock period. As the LHC proton-proton collisions and signal injection are synchronous to the same LHC clock, we can skew the digital activity in order to reduce the minimum detectable charge, by placing the signal on top of the baseline ripple.

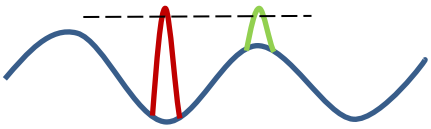

Figure 2: Output preamplifier baseline (in blue) with signal injected at 2 different digital clock phases. Green position allows to achieve the best minimum detectable charge.

3.2 Correcting time-of-arrival time walk using time-over-threshold

The finite rise time of the LGAD current and the fixed threshold make the threshold crossing time amplitude-dependent, requiring time-walk correction. It can be successfully performed with prior knowledge of the relationship between the TOA and the TOT.

3.3 Comparing jitter measurements with simulation

Figure 3 displays the time-of-arrival standard deviation as function of the input charge for 2 ASIC configurations. First, it can be seen that the measured jitter floor is above what is expected in simulation, despite simulating the analog front-end in post-layout view with a detector capacitance of 4 pF, a LGAD-like calibration pulse used in testbench and assuming a 10 ps clock jitter from the PLL. Second, jitter discrepancies appear at the lowest charge plotted when at least all the transimpedance channels are enabled.

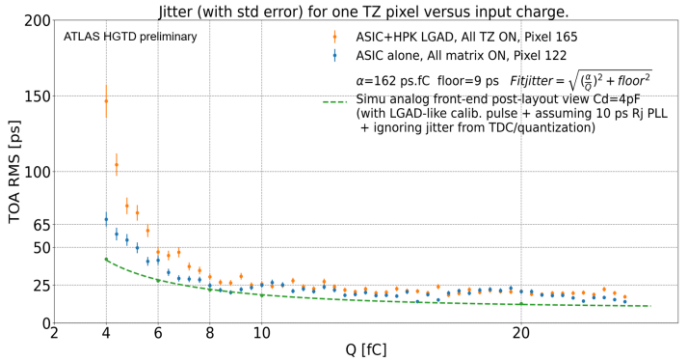

Figure 3: Jitter as function of charge with ALTIROC2 ASIC alone and ASIC+LGAD with at least all transimpedance (TZ) preamplifier channels enabled.

Recalling the jitter first-order relationship (Eq. 3) with the detector capacitance (emulating the LGAD's), one could argue that its value differs. However, the pulse reconstruction shows similar amplitudes ($V_{max} = Q_{in}/C_d$) and falling edge decay time ($\tau \propto Z_{in}.C_d$, Z_{in} preamplifier input impedance) with the real or 3.5 pF emulated capacitance. It proves the internal LGAD-like capacitance corresponds well to 3.5 pF.

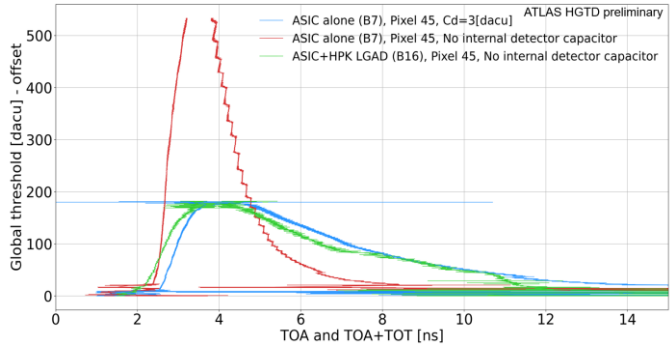

Figure 4: Pulse reconstructions of a voltage preamplifier (pixel 45) between 2 configurations : ALTIROC2 ASIC alone (with and without internal detector capacitance) versus ASIC+LGAD (without internal detector capacitance)

A possible other reason explaining such jitter difference is the fact that the jitter is not only charge-dependent but also threshold-dependent. Figure 3 plots the jitter versus the input charge for various discriminator threshold alignments. The jitter values correspond to the mean of all transimpedance channels for an ASIC alone. We first align the discriminator of all channels injected to a corresponding charge of 3.2 fC. We observe the typical hyperbolic jitter function with the charge. But if we redo the discriminator alignment to a lower charge, we can observe that the jitter increases at a faster pace than the hyperbola in the vicinity of the threshold alignment charge. The threshold-depend behaviour can be explained drawing the pulse slope for various thresholds. The closer the threshold to the top of the pulse, the worst the slope and thus the jitter, as recalled by equation 1.

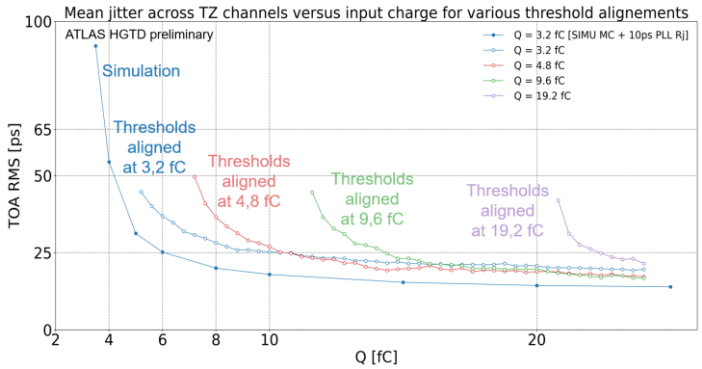

Figure 5: Mean jitter across transimpedance (TZ) preamplifier channels as function of charge with ALTIROC2 ASIC alone with all transimpedance preamplifier channels enabled and for various global discriminator alignments at various charges.

Similarly, for even lower minimum detectable charge alignment, the jitter suffers this slope effect, due to the system start-up time before maximum slew rate.

3.4 ASIC behaviour under irradiation

ALTIROC2 (ASIC alone) was tested under TID irradiations up to 220 Mrads. All the DC levels have remained unchanged under irradiation. The working behaviour of the ASIC has been verified at the system level measuring the jitter while repeating calibration test injections. Measurements have shown a stable jitter for calibration signal of 4 and 10 fC amplitude for the ASIC alone .

4. Conclusion

ALTIROC2 is a 225 channels ASIC designed to readout Low Gain Avalanche Diodes (LGAD) matrix that exhibits a 4 pF capacitance per channel. It embeds all digital functionalities to stream at 1.28 Gbps timing measurements performed by the low noise, 1 GHz bandwidth analog front-end. ALTIROC2 has demonstrated very promising analog performances on testbench and at system level. Testbench measurements gave an RMS jitter around 25 ps at the initial charge delivered by the LGAD (10 fC) and a threshold that could be set as low as 3.8 fC using the internal calibration pulser with the sensor. The next version of the ASIC is currently under design. ALTIROC3 will go one step closer from the HL-LHC conditions, insuring SEE hardness with triplicated digital logic, always keeping in mind the stringent low power budget. Next version will also leverage on bunch crossing synchronicity to skew digital noisy activity from analog low signal timing measurements.

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