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Testing of the HCC and AMAC functionality and radiation tolerance for the HL-LHC ATLAS ITk Strip Detector

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ABSTRACT: For the High-Luminosity phase of the LHC, which begins operation in 2029, the current ATLAS inner detector will be replaced by a new tracker, the ITk. The ITk consists of two subdetectors, one using pixels and the second using silicon-strips, the ITk Strip detector. The HCC and AMAC chip are radiation-tolerant ASICs that contribute to the front-end readout, monitoring and control of the ITk Strip subsystem. Low temperature startups and low internal regulated voltage tests have been performed on HCC and AMAC to guarantee their reliability at edge operation conditions. In addition, to ensure the operation of the HCC and AMAC under a radiation heavy environment, gamma and x-ray irradiation campaigns were conducted. HCC and AMAC successfully operated at harsher conditions than the ones expected during the HL-LHC.

KEYWORDS: Particle tracking detectors; Radiation-hard detectors; Radiation-hard electronics

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1 HL-LHC ATLAS Inner Tracker Upgrade

The High-Luminosity Large Hadron Collider (HL-LHC) is an upgrade of the LHC which is expected to reach a peak instantaneous luminosity of $7.5 \times 10^{-34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$. The effect of this upgrade on the ATLAS experiment [1] is a busy charged-particle environment that will require higher radiation tolerant components. Additionally, to obtain the desired tracking reconstruction efficiency and precision, a faster readout and finer granularity detector is required. To achieve the new requirements, the current ATLAS inner detector will be replaced with the Inner Tracker (ITk), an all-silicon based charged-particle detector composed of the ITk Pixel [2] and ITk Strip [3] subsystems.

2 HCC and AMAC

The ITk Strip detector is composed of carbon composite structures that support modules, where each module contains up to 2 silicon sensors and three types of custom ASICs designed for the readout, monitoring and control of the module: ATLAS Binary Chip (ABC), Hybrid Control Chip (HCC) and Autonomous Monitoring and Control Chip (AMAC) [3].

The HCC receives and forwards clock and control signals to up to 11 ABCs. Also, the HCC simultaneously collects data from the attached ABCs which is subsequently serialized and transmitted to the End of Substructure (EoS) board at up to 640 Mbps.

The AMAC provides control of the module and monitors key module temperatures, voltages and currents. Additionally, the AMAC has programmable limits for monitored quantities that allow for the autonomous turnoff of the DC-DC converter, ASICs, and/or sensor high bias voltage via an interlock mechanism.

3 Functionality testing

In addition to the various tests and checks performed on HCC and AMAC [8–11], the HCC and AMAC functionality was tested at edge operational conditions such as low temperature startups and low regulated voltage.

One of the main effects of radiation damage is an increase in current of active components [4]. Increased current leakage in addition to the limitations on the output power delivered by the bPOL12V [6] and linPOL12V [7] could cause a decrease in the input voltage to the ITk Strip subdetector ASICs internal low-dropout regulator (LDO). This could require the ITk Strip subdetector ASICs to operate at a lower regulated voltage than ideally desired. Furthermore, the increase in current leakage decreases the signal to noise resolution of sensors. This effect can be damped by running the detector at colder temperatures. Therefore, the ASICs will need to start at cold temperatures although they will be operating at significantly warmer temperatures.

3.1 Low regulated voltage

HCC and AMAC are expected to operate at an internal low-dropout regulated voltage of 1.2 V. HCCStarV1 has been tested at regulated voltages ranging from 1.06 to 1.45 V and at Bunch Crossing clock (BCO) frequencies ranging from 32 to 48 MHz to verify operating margins. A shmoo scan performed on HCCStarV1 at -45 °C is shown in Figure 1, where it was verified that there is plenty of operating phase-space around the nominal operating parameters. AMACStar was successfully tested at regulated voltages as low as 1.0 V. In general, both ASICs operated without complications at the lowest regulated voltage considered.

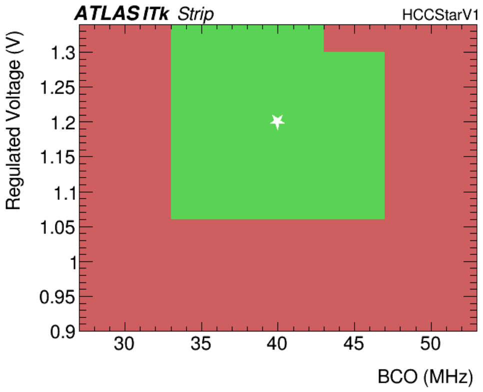

Figure 1: Shmoo scan showing operational range of a HCCStarV1 cooled to -45 °C as a function of regulated voltage and frequency of the Bunch Crossing clock (BCO). The successful operating phase space is shown in green, while failing or untested phase-space is shown in red. The white star denotes the nominal operating parameters of 40 MHz and 1.2 V.

3.2 Low temperature

The ITk Strip subdetector is expected to have start up temperatures as low as -35 °C. Although HCC and AMAC will need to be able to start at low temperatures, they are expected to run at significantly higher temperatures because of heat dissipation from normal operations. HCCStarV1 was tested as cold as -45 °C and AMACStar was tested down to a temperature of -70 °C. Both HCCStarV1 and AMACStar successfully operated at the coldest temperatures and only minor benign features developed at extremely low temperatures as shown in Figure 2.

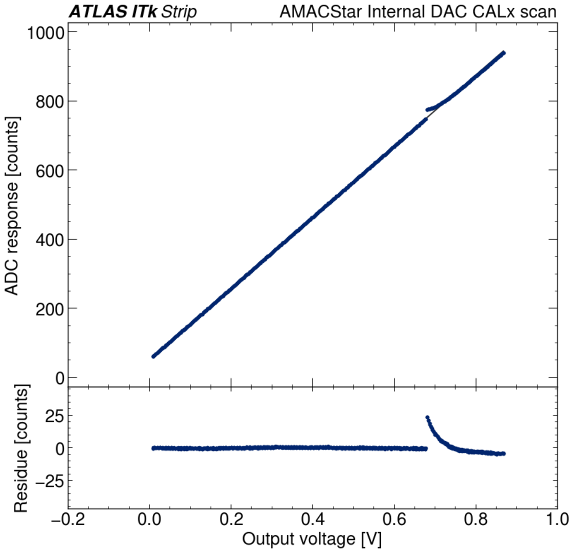

Figure 2: AMACStar CALx Analog Monitor response as a function of an independent ADC output voltage measurement obtained at -70°C. A nonlinearity is observed in the response of the AMAC's Analog Monitor (AM) near 700 counts due to cold temperature effects present at the comparator swap. This effect is not present in the temperatures expected during operation.

4 Radiation tolerance

HCC and AMAC are expected to receive a maximum dose rate of 50 Mrads [3]. To test the reliability of HCC and AMAC, slow and fast total ionizing dose (TID) irradiation campaigns were conducted.

4.1 Slow total ionizing dose

The prototype versions of HCC and AMAC, HCCStarV0 and AMACv2a, were irradiated with 1 MeV gammas from a Co^{60} source at Brookhaven National Lab (BNL). The dose rate received by both ASICs was 1.1 krad/hr and they were operated at a controlled temperature of -10 °C.

As expected, the build up of electron-hole pairs on the p-n junction of the chip's transistors increased the current leakage of both ASICs [5], reaching a maximum current before a TID of 1 Mrad. Past the maximum current, a constant current decrease is observed due to the shielding of the created holes which subsequently dissipate the electron build-up responsible for the increase in current leakage [5]. The current of the HCCStarV0 throughout the slow TID irradiation for different driver currents can be seen in Figure 3. Both AMACv2a and HCCStarV0 performed well up to the end of the irradiation corresponding to a TID of 50 Mrad.

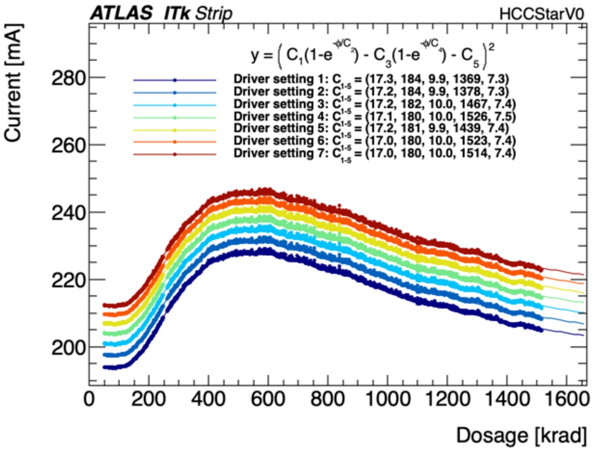

Figure 3: Current increase under slow gamma irradiation for HCCStarV0 for seven different driver currents. The HCC received a dose rate of 1.1 krad/hr at -10 °C. Each current distribution is fit with the functional form displayed on the plot, and the best-fit parameters are given in the legend.

4.2 Fast total ionizing dose

The HCCStarV1 and AMACStar were irradiated with X-rays at Lawrence Berkeley National Laboratory (LBNL). A total of eight ASICs per design were irradiated. A subset of the ASICs were irradiated at a dose rate of 0.8 Mrad/hr up to 5 Mrads while two ASICs per design were irradiated (further irradiated) with a dose rate of 2.36 Mrad/hr up to 75 Mrads. All the ASICs were irradiated at a controlled temperature of 20 °C.

The main difference between fast and slow TID is that the maximum current is dependent on dose rate. The AMACStar current during the fast TID irradiation can be observed in Figure 4, where variation of maximum current consumption can be observed for AMACStars irradiated at similar dose rates. In all cases, the maximum current is reached around 1 Mrad.

Some functionality of both the AMACStar and HCCStarV1 was affected near the current peak, but the long TID runs show that normal operation was recovered past the current peak. An example of affected functionality can be observed in Figure 5. However, this is not expected to be a problem since pre-irradiation of ASICs will avoid operation near the current peak.

In general, both AMACStar and HCCStarV1 performed well and were fully operational up to the end of each irradiation cycle.

5 It’s all good

Functionality and radiation tolerance tests were performed on different versions of the HCC and AMAC designs. Both ASICs pass the functional verification even after receiving doses of radiation comparable to the doses expected in the lifetime of the ITk Strip subdetector.

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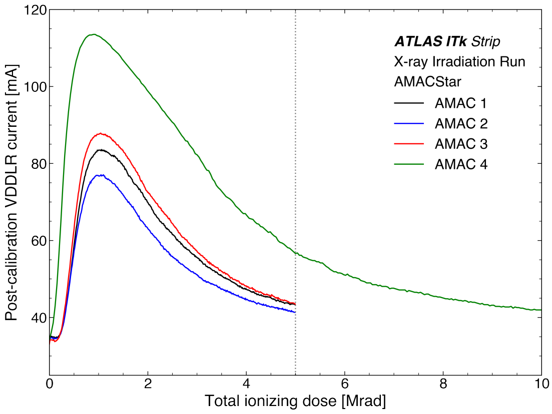

Figure 4: Current consumption of the 1.4 V line for four AMACStars as a function of TID. AMACs 1 through 3 were irradiated at a dose rate of 0.8 Mrad/hr over 6 hours for a TID of 5 Mrad. AMAC 4 was irradiated at a dose rate of 2.36 Mrad/hr over 32 hours for a TID of 75 Mrad.

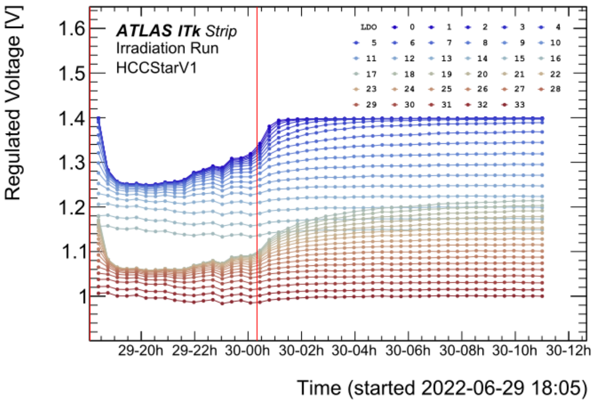

Figure 5: Regulated voltage as a function of time for a HCCStarV1 undergoing X-ray irradiation at a rate of 0.8 Mrad/hr. Values are shown for 34 consecutive settings of the internal LDO, split into two voltage range domains (blue to grey and grey to red). Vertical red lines denote the start and end of irradiation, with a total dose of 5 MRad. A temporary gap in achievable regulated voltage appears between the two domains. A nominal input voltage of 1.5 V was provided, which varied by no more than 20 mV during irradiation.

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