Prepared for submission to JINST

Topical Workshop on Electronics for Particle Physics 19-23 September 2022
Bergen, Norway

Design and testing of long Flexible Printed Circuits for the ATLAS High Granularity Timing Detector demonstrator

M. Robles Manzano on behalf of the ATLAS-HGTD Collaboration, [c,1] **A. Brogna**[b] **J. Ehrecke**[a] **A. Kurt**[b] **L. Masetti**[c] **J. Patel**[a] **B. Pham** [b] **P. Theobald**[b] **Q. Weitzel**[b]

[a] *Institute of Physics, Johannes Gutenberg University Mainz, Germany*
[b] *Detector Laboratory, PRISMA$^+$ Cluster of Excellence, Johannes Gutenberg University Mainz, Germany*
[c] *Institute of Physics and PRISMA$^+$ Cluster of Excellence, Johannes Gutenberg University Mainz, Germany*

E-mail: mroblesm@uni-mainz.de

Abstract: The High Granularity Timing Detector for the ATLAS upgrade is under construction to meet the challenges of the HL-LHC. In order to connect a module, the basic detector element, to the surrounding peripheral electronic board, a flexible printed circuit (FPC) is used as an interconnection for data transmission and power distribution. An identical design for all FPCs is required except for their length, depending on the module position on the detector active area. The design and qualification of a preliminary FPC version, manufactured in 13 different lengths (from 28.5 to 73.2 cm), are presented.

Keywords: Analogue and digital electronic circuits, special cables, Timing detectors

Dedicated to Peter Bernhard

ATL-HGTD-PROC-2022-003
12 October 2022

[1] Corresponding author.

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1 The ATLAS High Granularity Timing Detector

The ALTAS detector at CERN [1], is being upgraded to face the new challenges of the High Luminosity LHC [2]. The increase in the number of collisions per bunch crossing at the LHC leads to an overlap of events in the current detector, called pileup effect, which can be mitigated by providing precise timing information, with a resolution of 30 ps per track. A High Granularity Timing Detector (HGTD) is being built to mitigate pileup in the ATLAS forward region where two identical wheels are to be installed between the barrel and the end-cap calorimeters, see figure 1. Each wheel consists of two instrumented double-sided layers. The active area is dedicated to placement of 8034 modules. A module consists of two Low Gain Avalanche Detectors (LGADs) [3] each bump-bonded to an ASIC, to form a hybrid. The hybrids are glued and wire-bonded to a module flex, a Flexible Printed Circuit (FPC) with passive components, forming the module with an area about $2\,\text{cm} \times 4\,\text{cm}$. The Peripheral Electronic Boards (PEB), dedicated PCBs for readout, power and High Voltage (HV) delivery, surround the active area. A further FPC, called in the following flex tail, serves as interconnection between the modules and the PEBs.

2 Requirements and design of the flex tail for the demonstrator

The flex tail must include several type of signals, listed in table 1. The ASICs require signals for communication at a maximum rate of $1.28\,\text{Gbit/s}$, slow control and dedicated planes for both ground and power, while HV is delivered to the LGADs via a single track. The geometry of the flex tail is defined by the arrangement of the modules in the so-called readout rows, see figure 1. The longest readout row is populated with 19 modules. The space available to stack the corresponding 19 flex tails is defined by the space between two instrumented disks, 4.2 mm, limiting its thickness to a maximum of $220\,\mu\text{m}$. The nominal length is defined by the position of the module on the readout row and the connector on the PEB. Nevertheless, extra length should be considered to avoid

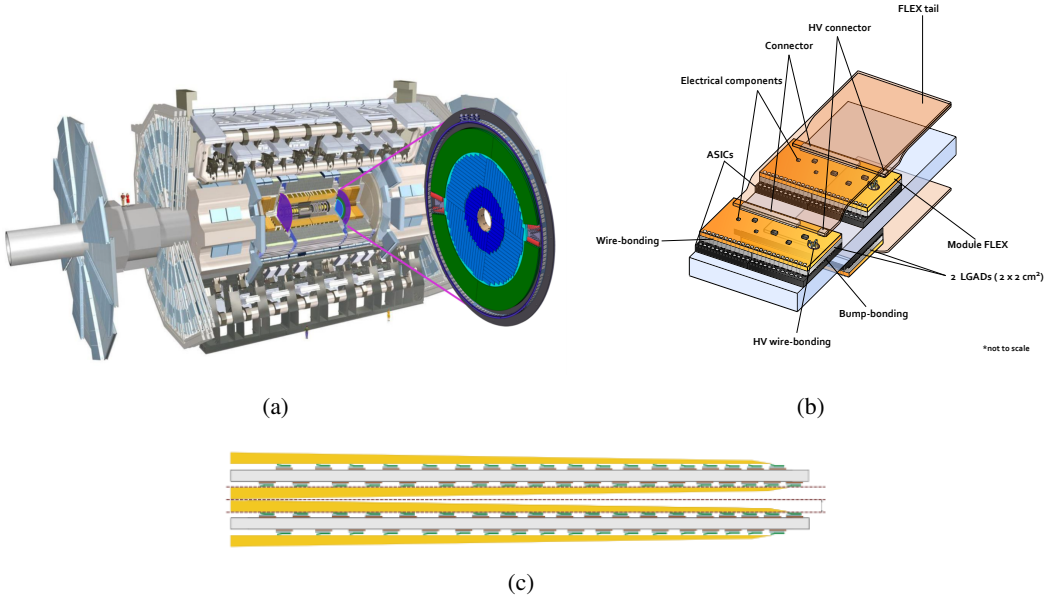


Figure 1. (a) Illustration of the HGTD and its position within the ATLAS experiment, showing the peripheral on-detector electronics in green and the layout of the readout rows, containing modules mounted on half disk support plates (blue) [2]. (b) Schematic drawing of two adjacent modules on the top side and one at the bottom side of the support plate [2]. (c) Illustration of a cross section of HGTD the longest readout-out, 19 modules and flex tails on two support plates. Copyright CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license, re-used with permission [4].

mechanical stress due to differences in contraction and expansion as a function of temperature. The nominal lengths range from 3 cm to 69 cm. The width of the flex tail is 36 mm. In comparison with traditional PCBs, the FPC technology can fulfill the aforementioned requirements due to its versatility in terms of geometry and electrical capability.

In order to validate the different components of the detector during the R&D phase, a demonstrator is being built. It is planned to tests the performance of the longest readout row in terms of electrical, mechanical and thermal performance. A PEB prototype is being designed, including 6 flex tails attached for the outer modules, while the interconnection for the 13 inner modules requires individual flex tails, see figure 2 (b). A 2-layer flex tail has been designed and produced by two vendors with two different stack-ups in terms of materials and thicknesses: 90 pieces of prototype A [5], see figure 2 (a), with a nominal thickness of 206 µm in lengths ranging from 28.5 to 73.2 cm plus 40 extra 6.5 cm long pieces for module testing purposes, and 5 pieces of prototype B with a nominal thickness of 186 µm and 73.2 cm long. The track topology was adapted to meet the impedance specifications, in a range from 90 Ω to 120 Ω for differential and from 50 Ω to 65 Ω for single-ended lines. Dedicated PCBs were designed and produced to test the flex tails.

(a) (b)

Figure 2. (a) 13 flex tail lengths of prototype A. (b) Sketch of the single readout-row demonstrator [2]. Copyright CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license, re-used with permission [4].

Table 1. Type and number of signal lines per module included in the flex tail [2].

Signal name	Signal type	No. of wires	Comments
HV	1 kV max.	1	Clearance, Insulation resistance > 2.7 MΩ
POWER	1 × Vdda, 1 × Vddd, 1.2 V	2 planes	$R < 2.7\,\mathrm{m\Omega/cm}$
GROUND	Analog, Digital	1(2) plane(s)	Dedicated layer $R < 0.7\,\mathrm{m\Omega/cm}$
Slow control	Open drain (SCL, SDA), CMOS	2, 3	I^2C link
Input clocks	320 MHz, Fast command e-link (opt. 40 MHz clock)	4 or 8	CERN Low Power Signalling (CLPS)
Data out lines	Readout data	4 pairs	4 e-links differential CLPS, Max. 1.28 Gbit/s
ASIC reset	ASIC_rst	1	Digital
Monitoring	Temperature, Vdda, Vddd	6	DC voltage
Debugging	ASIC_debug	2	Analog

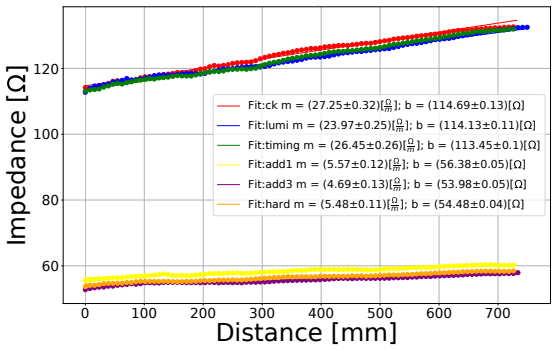
3 Flex tail signal integrity standalone and system level tests

3.1 Impedance control tests: Time Domain Reflectometry

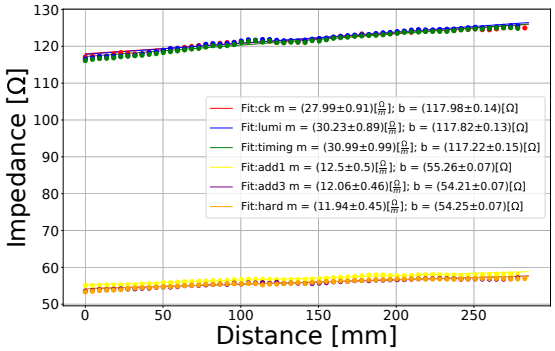
The impedance homogeneity has been characterized for selected length prototypes via the Time Domain Reflectometry technique. Three differential pairs and three single lines in a flex tail were connected to TDR module 80E08 together with the DSA8200 oscilloscope by Tektronix [6] via a custom adapter board. The results for two prototypes, respectively 73.2 cm and 28.5 cm long, are shown in figure 3. The results at the connection region fulfill specifications in section 2. As expected for a real transmission line, where the resistive effects of the copper tracks and dielectric material play a role [7], the impedance increases linearly along the flex tail. See figure 3.

3.2 Bit Error Rate Test and eye diagram

To emulate the digital transmission from the ASIC, an FPGA based on the Kintex Ultrascale+ evaluation kit [8] has been programmed and connected to the flex tail via an adapter board to build



(a)



(b)

Figure 3. Results of the impedance for single lines and for the differential pairs in the 73.2 cm and 28.5 cm long prototypes of the type A. The legend represents the labelling of each line on the prototypes. m and b represent the parameters after linear fitting, $y = m * x + b$. Copyright CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license, re-used with permission [4].

an automatic test setup. The FPGA injects test patterns at 1.25 Gbit/s and checks the response with the Integrated Bit Error Rate Test (IBERT). Two differential pairs are connected in loopback configuration via SMA connectors in a dedicated PCB at the opposite end of the flex tail with respect to the FPGA, see figure 4[1]. No errors were detected during the IBERT for 24 hours, reaching a BER result of less than 10^{-14}. This value is well below the acceptable error rate of 10^{-12}. The same test was repeated while delivering HV up to 1000 V (3 mA) with no errors.

3.3 Jitter measurements and results

The jitter contribution of the flex tail must be below 5 ps since the length of the tracks may impact the jitter performance. Flex tails of different lengths were tested at the High Precision Timing Distribution lab at CERN [11] using the Time Interval Error method. The measured jitter values of the prototype A flex tails ranges from 2.6 ps for the 6.5 cm long flex tail to 5 ps for the 73.2 cm

[1]The test configuration and the I/O drivers are compatible with the VC707 FPGA [9] used by the LpGBT system [10] in order to guarantee the same conditions for the signal transmission as for the on-field operation.

(a)

Figure 4. IBERT setup, from right two left: Kintex Ultrascale+ evaluation board, adapter board, 73.2 cm flex tail prototype, testboard for loopback configuration. Copyright CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license, re-used with permission [4].

long one including the contribution of the clock generator. A more detailed analysis to subtract this contribution is ongoing, but it can already be concluded that the flex tails fulfill the jitter specification.

3.4 System level tests and integration in the demonstrator

Prior to their integration in the demonstrator, communications tests between module and the PEB prototype are required. Selected pieces of flex tail prototypes A and B were connected to both the PEB protype and module emulators[2]. Communication tests at high speed rate, 320 Mbit/s and 1.25 Gbit/s reached BER $<10^{-12}$. Similarly, multi I^2C communication tests were successful in a setup replacing the module emulators by digital modules, i.e., modules excluding LGADs, see figure 5.

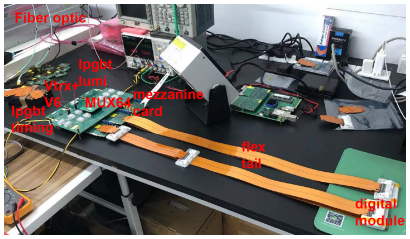


Figure 5. Seven flex tail prototypes A and B connecting a PEB prototype and seven digital modules for multi I^2C communication tests. CC-BY-4.0 license, re-used with permission [4].

4 Summary and outlook

A 2-layer flexible printed circuit, the flex tail, for the HGTD demonstrator of the longest readout row has been designed and produced for different lengths. Signal integrity evaluation test results for selected length prototypes such as impedance control, BER and jitter measurements are within specifications. Power integrity tests are planned for voltage drop evaluation in addition to systematic tests for the remaining prototypes. Moreover, mechanical tests are crucial to ensure the proper functionality in the full temperature range and avoid damage due to mechanical stress. The integration of the flex tails in the demonstrator will provide essential information on the performance of the HGTD.

[2]Modules based on FPGA Spartan-7 to emulate the ASIC performace.

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