Global Trigger Versatile Module for ATLAS Phase-II upgrade

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ABSTRACT: The ATLAS detector at the Large Hadron Collider will undergo a major Phase-II upgrade for the High Luminosity LHC. The upgrade affects all the main ATLAS systems including the Trigger and Data Acquisition. As part of the Level-0 Trigger System, the Global Trigger uses full-granularity calorimeter cells to perform algorithms, refines the L0Calo trigger objects and applies topological requirements. The Global Trigger uses an ATCA Global Common Module as a building block of its design. The additional, standalone, Global Trigger Versatile Module has been designed according to the Global Trigger hardware specifications. The Global Trigger Versatile Module acts as an auxiliary hardware component that can be used for development, testing and operational purposes within and beyond the Global Trigger in projects requiring high bandwidth and processing capabilities. To achieve a high input and output bandwidth and substantial processing power the Global Trigger Versatile Module hosts an advanced Xilinx Ultrascale+ VU13P FPGA and Finisar BOA optical modules, running at high data rates up to 25.8 Gb/s, as well as other hardware resources needed for the Global Trigger, located on a high-density PCB, optimized for high-speed data transmission. A testing program of the Global Trigger Versatile Module includes verification of the main hardware functionality of the module, performance evaluation of the high-speed optical modules and the FPGA, and Global Common Module development firmware tests. Successful results demonstrating a good performance of the on-board components have been obtained.

KEYWORDS: LHC; ATLAS; FPGA; Optical Modules.

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1. Introduction

The Global Trigger System is a part of the Phase-II upgrade of the ATLAS [1] Trigger and Data Acquisition (TDAQ) system [2]. It will replace the Phase-I Topological Processor [3] and extend its functions by using full-granularity calorimeter cells for refining the trigger objects calculated by the Level-0 Trigger System, performing offline-like algorithms, including iterative algorithms such as topoclustering, calculating event-level quantities and applying topological requirements (Fig. 1).

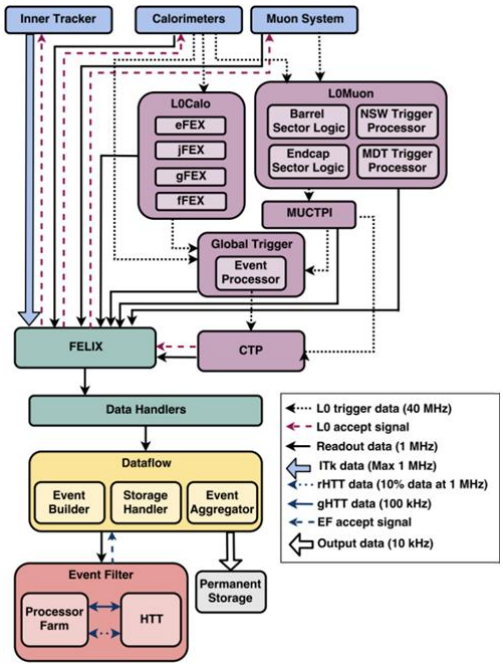

Figure 1. TDAQ System after the Phase-II upgrade [2]. Receiving full-granularity calorimeter cells to refine L0Calo & L0Muon outputs, Global Trigger has a central location within the TDAQ System.

The Global Trigger is a time-multiplexed system, which concentrates the data of a full event into a single processor. The Global Trigger System is composed of three main layers: a Multiplexing (MUX) layer, a Global Event Processor (GEP) layer and a Demultiplexing layer, which implements an interface to the Central Trigger Processor (CTP) (Fig. 2). The CTP then

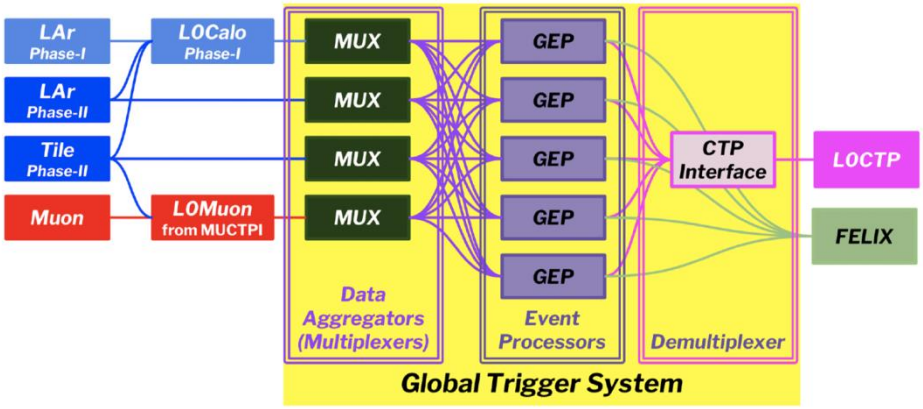

Figure 2. Schematic view of the Global Trigger System [2] (in yellow), illustrating the detector inputs, multiplexing MUX layer, event-processing GEP layer, demultiplexing CTP Interface, and connections to other systems.

takes the final trigger decision. The Global Trigger System accommodates more than 2300 input optical fibers with link speeds up to 25.8 Gb/s.

A building block of the Global Trigger is the Global Common Module (GCM) [4], which has to provide significant processing resources along with a high input and output bandwidth. Various link speeds, including high-speed links up to 25.8 Gb/s, should be supported. The high-speed link support is essential in order to cope with the transmission of high-granularity calorimeter data which drives the bandwidth requirement for the upgraded TDAQ system.

An additional Global Trigger Versatile Module (GVM) has been designed according to the Global Trigger hardware specifications. The GVM hosts the new generation of optical modules and Field-Programmable Gate Arrays (FPGA) running at the required data rates, as well as other hardware resources needed for the Global Trigger, and acts as an auxiliary hardware component that can be used for development, testing and operational purposes within and beyond the Global Trigger in projects requiring high bandwidth and processing capabilities.

2. Board overview

The GVM is designed in an ATCA form factor with the possibility of a standalone operation (Fig. 3). The main building blocks are the following: one large processing FPGA (Xilinx Ultrascale+ VU13P [5]), up to eight Finisar Board-Mount Optical Assembly (BOA) modules [6] for real-time data path, one Finisar BOA module for interface to Front-End Link eXchange (FELIX) system, one UltraZed board with Zynq UltraScale+, one IPM Controller (IPMC), one FPGA power mezzanine and two DDR4 RAMs. Dedicated clock distribution circuits are implemented as well in order to provide reference clocks for the multi-gigabit transceivers of the FPGA.

The design choice towards Finisar BOA optical modules was possible thanks to the evaluations performed with the Global Trigger Technological Demonstrator [7].

3. High-speed PCB design considerations

In order to optimize the signal integrity for the high-speed signals between the FPGA and optical modules as well as other high-speed components, dedicated high-speed PCB design routing techniques were used.

Thus, all the high-speed differential pairs adhere to strict physical and spacing constraints.

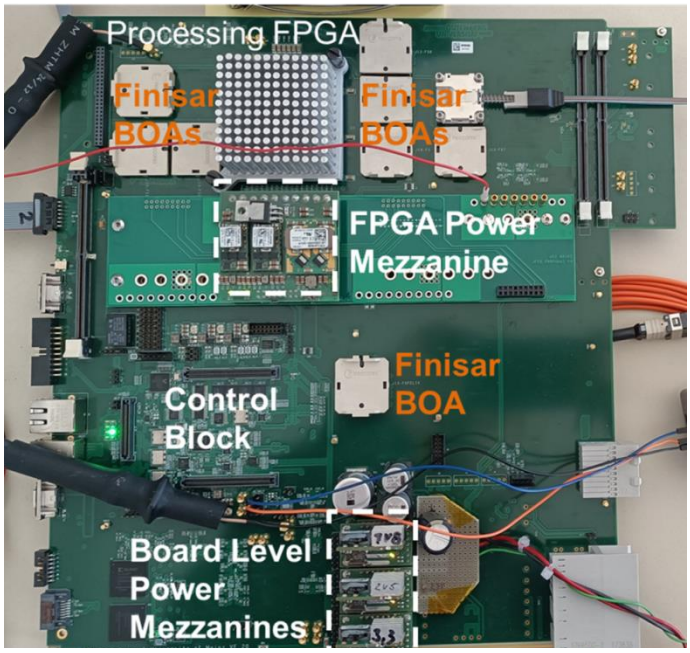

Figure 3. GVM hardware top view with the most important building blocks labeled

Phase tuning is performed in order to stay within the phase tolerance limit. Appropriate in-pair spacing and trace width provide the 100 Ohm ± 10% differential impedance, while sufficient spacing across all pairs (4 times larger than the in-pair spacing) minimizes the crosstalk. Each high-speed signal trace is routed entirely on a single internal layer, apart from the transition areas between the outer and the inner layers, where ground vias are used in order to improve the signal integrity. The in-pair spacing is constant over the entire trace length.

Moreover, the stack-up (Fig. 4) is designed in such a way as to provide good signal integrity for high-speed signals. Signal planes are shielded by the ground planes, thus minimizing the crosstalk. High-speed signals occupy the top and bottom inner layers, and use microvias in order to avoid stubs on the signal lines. Buried vias are used as well in order to provide a better connection between the top and the bottom microvia layers.

Ultra-low transmission loss and highly heat resistant PCB material (MEGTRON6 [8]) is used for the PCB due to its good dielectric constant and dissipation factor for high frequencies.

4. Performance evaluation

The main hardware functionality of the module including power, clock trees, JTAG chain, main processing FPGA and control block has been verified.

Performance of the high-speed optical modules and the FPGA has been evaluated with long-run link tests. An Integrated Bit Error Ratio Test (IBERT) loopback test has been performed for the Finisar BOA optical module. The optical channels of the module are grouped

into two separate 12-lane rows compatible with a standard 2x12 bare MT ferrule. The first row contains all the receiver lanes, the second row all the transmitter lanes. Thus, in the test it was

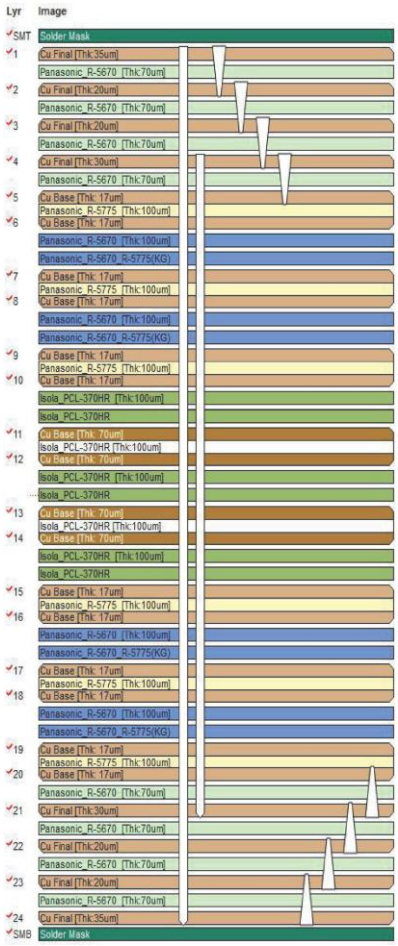

Figure 4. Global Trigger Versatile Module stack-up. 24 layers in total. Layers 3 and 5 dedicated for high-speed links to optical modules.

possible to loop 12 transmitter links of the optical module back to 12 receiver links of the same module with a help of a “24 to 2x12-fiber” Y-cable and a 12-fiber trunk cable (Fig. 5).

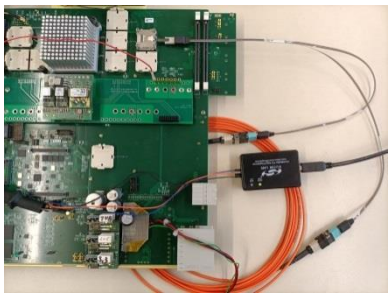

Figure 5. Finisar BOA IBERT loopback test: test setup. BOA optical module mounted on the GVM as well as the “24 to 2x12-fiber” Y-cable and the 12-fiber trunk cable are shown

An IBERT test run at 25.78125 Gb/s, using a 31-bit PRBS pattern, has been performed. All 12 links are functional, and no bit errors have been detected (Fig. 6), measuring the BER down to $4.9 \cdot 10^{-15}$.

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Post-Curs
Ungrouped Links (0)											
Link Group 0 (12)							Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 0	MGT_X0Y47/TX	MGT_X0Y46/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 1	MGT_X0Y46/TX	MGT_X0Y47/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 2	MGT_X0Y45/TX	MGT_X0Y45/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 3	MGT_X0Y44/TX	MGT_X0Y44/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 4	MGT_X0Y42/TX	MGT_X0Y43/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 5	MGT_X0Y43/TX	MGT_X0Y42/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 6	MGT_X0Y40/TX	MGT_X0Y41/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 7	MGT_X0Y41/TX	MGT_X0Y40/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 8	MGT_X0Y38/TX	MGT_X0Y39/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 9	MGT_X0Y39/TX	MGT_X0Y38/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 10	MGT_X0Y36/TX	MGT_X0Y37/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000
Link 11	MGT_X0Y37/TX	MGT_X0Y36/RX	25.781 Gbps	2.024E14	0E0	4.941E-15	Reset	PRBS 31-bit	PRBS 31-bit	0.00 dB (00000)	0.00 dB (0000

Figure 6. Finisar BOA IBERT loopback test: links status. “Status” column shows the link data rate, green background indicates that the link is functional. “Errors” column indicates the absence of errors.

A typical eye diagram, obtained using a low power mode of the GTY receiver, is shown in Fig. 7. With an open area of 8712, a good performance of the Finisar BOA optical module is achieved.

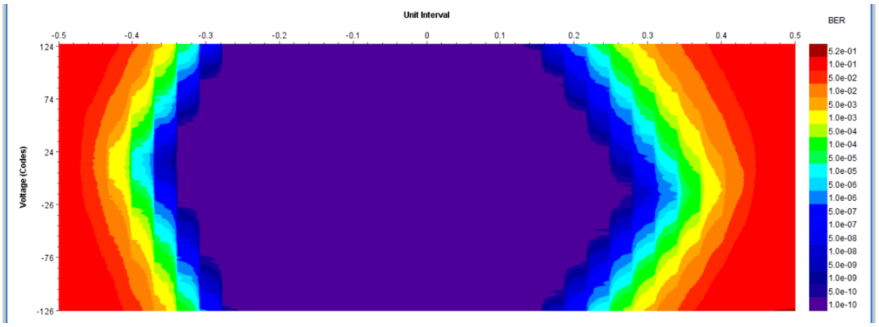

Figure 7. Finisar BOA IBERT loopback test: a typical eye diagram. Open area: 8712 @ 25.8 Gb/s.

Eye diagrams for other 11 optical links show a good eye-opening and overall good performance of the optical module as well.

5. Firmware tests

The GVM is available to developers and is currently in use for GCM firmware testing and development. For example, several tests for the topoclustering algorithm firmware, integrated into a custom firmware framework, have been performed.

6. Conclusion

A Global Trigger Versatile Module has been designed according to the Global Trigger hardware specifications, hosting the new generation of optical modules (Finisar BOA) and FPGA (Xilinx Virtex UltraScale+ 13P) running at high data rates up to 25.8 Gb/s, as well as other hardware resources needed for the Global Trigger. The main hardware functionality of the module including performance of the high-speed optical modules and the FPGA has been successfully evaluated. GCM development firmware tests are currently being performed on the GVM. Advanced hardware resources and adherence to the Global Trigger hardware specifications make the Global Trigger Versatile Module a valuable hardware component that can be used for development, testing and operational purposes within and beyond the Global Trigger in projects requiring high bandwidth and processing capabilities.

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