Upgraded data readout and transmission electronics for the Resistive Plate Chambers of the ATLAS Muon Trigger System for the High Luminosity LHC

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***Abstract*—The Muon Spectrometer of the ATLAS detector will be significantly modified during the Phase-II upgrade in order to maintain low-momentum trigger thresholds at an acceptable trigger rate also in the increased particle rates, integrated radiation and pile-up of the High Luminosity LHC runs. The new requirements for trigger rate and latency impose the replacement of the current trigger and readout electronics of the Resistive Plate Chambers. New Data Collector and Transmitter boards will be installed to collect and digitize the Resistive Plate Chambers data. This paper presents the new trigger and readout scheme of the Resistive Plate Chambers and the results of a test bench developed to evaluate the data transmission between the Data Collector and Transmitter board and its back-end counterpart. The communication test bench has been performed using evaluation boards implementing an emulator of the Low Power Gigabit Transceiver, the Data Collector and Transmitter component that handles the data transmission.**

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I. Introduction

The High Luminosity LHC (HL-LHC) will deliver to the LHC experiments an instantaneous luminosity up to $7.5 \times 10^{34}\ \mathrm{cm^{-2}s^{-1}}$, well above the original LHC design value of $10^{34}\ \mathrm{cm^{-2}s^{-1}}$, with a consequent increase of the pile-up and radiation levels which will pose a challenge to the on-detector electronics of the LHC experiments.

In order to maintain its excellent trigger and tracking performances even in the extremely high particle rate condition of HL-LHC, the Muon Spectrometer (MS) of the ATLAS detector [1] will undergo a significant upgrade during the Long Shutdown 3 (Phase-II upgrade), which foresees the improvement or the replacement of many detector components [2]. In particular, the entire trigger and readout electronics of the Resistive Plate Chambers (RPCs) of the ATLAS barrel region will be replaced to satisfy the requirements of the new trigger scheme [3]. The new first level hardware trigger (L0) will require a trigger rate up to $1\,\mathrm{MHz}$ and a latency of $10\,\mu\mathrm{s}$, while maximum values of trigger rate and latency accommodated by the current trigger and readout electronic system are $100\,\mathrm{kHz}$ and $3\,\mu\mathrm{s}$. In place of the current Pad and Splitter boxes [4], the new Data Collector and Transmitter (DCT) boards will be installed to collect the hit data from the RPCs and transfer them to the off-detector trigger and readout system.

After the description of the new RPC trigger and readout system foreseen for HL-LHC, this work presents the setup and the results of a test bench performed to evaluate the communication between the on-detector DCTs and the off-detector Sector Logic (SL) boards.

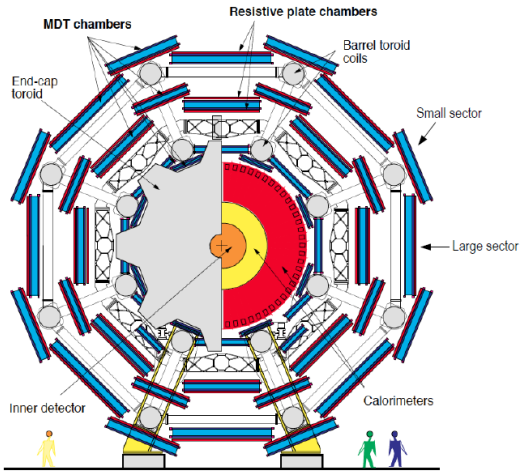

Figure 1. Schematic view of the transverse section of ATLAS barrel region [2].

II. Upgrade of the RPC System

The barrel region of the ATLAS Muon Spectrometer (Figure 1) consists of several layers of RPCs, employed for muon track reconstruction and trigger, and Monitored Drift Tubes (MDTs), used for precision muon tracking, arranged in three concentric regions around the beam axis, referred to as barrel inner (BI), middle (BM) and outer (BO) region. An RPC consists in a large planar capacitor with two parallel high bulk-resistivity electrode plates made of bakelite, separated by a $2\,\mathrm{mm}$ gap filled with a suitable gas mixture, target for the ionizing radiation. An electric field of several $\mathrm{kV/mm}$ across the gas gap starts an electron avalanche immediately after the primary ionization due to a crossing charged particle.

The current ATLAS RPC system is made of three layers of doublet chambers, each one composed of two gas gaps with readout electrodes and electronics. Two RPC doublets are situated in the BM region and the third one in the BO region. There are presently no RPCs in the BI region. Front-end boards

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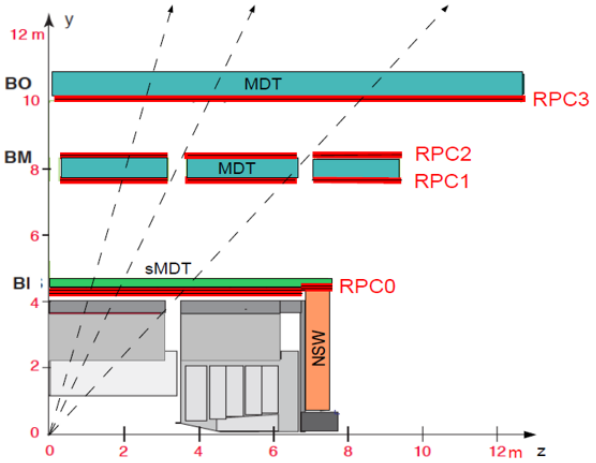

Figure 2. Schematic view of the longitudinal section of ATLAS barrel after the Phase-II upgrade [2].

collect the RPC signals and transmit them to the readout chain. The front-end boards are fully compatible with the HL-LHC operation and do not need to be replaced.

In the worst case scenario, to avoid the effects of ageing, there is the possibility that the RPC chambers will operate at a lower voltage at HL-LHC which would produce a reduction of the RPC efficiency. To restore the full trigger efficiency in that case, or anyhow to increase the redundancy of the trigger system, and at the same time to cover the current acceptance holes due to the barrel toroid coils and their support structures, a new layer of RPC triplet chambers will be added in the BI region of the spectrometer during the Phase-II upgrade (Figure 2). This new RPC inner layer is designed to increase the trigger acceptance and the trigger efficiency by loosening the requirements on the number of hits in the BM and BO chambers and, at the same time, adding the requirement of a coincidence with the BI layer. So any coincidence of hits in at least three chambers out of four will be accepted by the trigger. Furthermore, a coincidence of hits in the BI and BO chambers will be used to cover the remaining acceptance holes. With this scheme, the trigger efficiency times acceptance is foreseen to reach 92% in the worst case scenario.

III. Upgraded RPC Trigger and Readout System

To achieve the best physics performance at HL-LHC, the ATLAS Trigger and Data Acquisition System will undergo a major upgrade. The new trigger scheme foresees a first-level hardware trigger (L0 trigger), combining data collected by the Muon Spectrometer and the calorimeters, and a software-based High-Level Trigger (HLT), that will perform a full event reconstruction. The new requirements for the L0 trigger rate and latency, up to 1 MHz and 10 µs respectively, will allow to maintain low p_{T} thresholds on trigger objects, and thus a good acceptance for the most important physics channels, and at the same time will allow to run more complex trigger algorithms with respect to the current ones. The full hit data collected by the MS detectors will be sent to the SL boards in the counting room, which will implement the trigger algorithms (Figure 3).

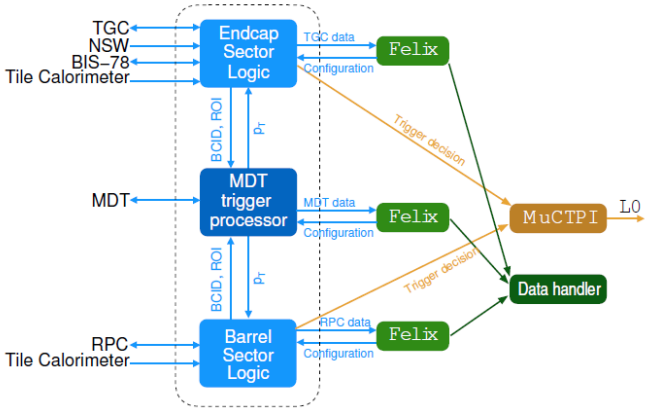

Figure 3. Muon trigger and readout scheme for HL-LHC [2].

In order to satisfy the Phase-II requirements for trigger rate and latency, all the RPC on-detector trigger and readout electronics, except for the front-end boards, will be replaced. Instead of the present Pad and Splitter boxes, 1 572 DCT boards will be installed to collect the RPC front-end signals and send them to the SL boards. The present front-end boards of the BM and BO RPC layers, which perform the amplifier, shaper and discriminator (ASD) logic, will be kept at HL-LHC. For the BI chambers, instead, a new type of front-end board is under development, which will implement not only the ASD logic, but also the TDC logic to digitize the RPC hit signals with 100 ps time resolution. Each DCT will collect the RPC data coming from up to 288 front-end channels, will digitize the signals for the BM and BO layers (with 800 ps time resolution) and will transmit zero-suppressed data to the counting room (USA15). In the counting room, 32 barrel SL boards, based on a Xilinx Virtex Ultrascale+ FPGA, will receive the hit data sent from the DCTs. Each SL board will be connected with up to 51 DCTs through bidirectional optical fibres.

Using information from the RPCs and the Tile calorimeter, the barrel SL boards will determine trigger candidates and will pass them to the MDT trigger processors, which will perform an improved measurement of muon momentum. This information will be sent back to the barrel SL boards, which will use it to confirm or reject the trigger candidates. The barrel SL boards will then send the trigger decision to the Muon Central Trigger Processor Interface. The SL boards will be also provided with local memories to store the hit data, which will be then transmitted to the HLT and the readout system through the Front-End Link Interface eXchange modules, upon the decision to accept the event from the ATLAS Central Trigger Processor.

The first barrel SL board has been produced and is currently under test.

IV. The Data Collector and Transmitter Boards

The DCT is a board based on a FPGA from the Xilinx Artix-7 family (Figure 4). In the Phase-II trigger and readout scheme, the DCTs will have the task of sending the hit data collected by the RPC to the counting room and will be controlled by the barrel SL boards through a bidirectional optical fibre. The

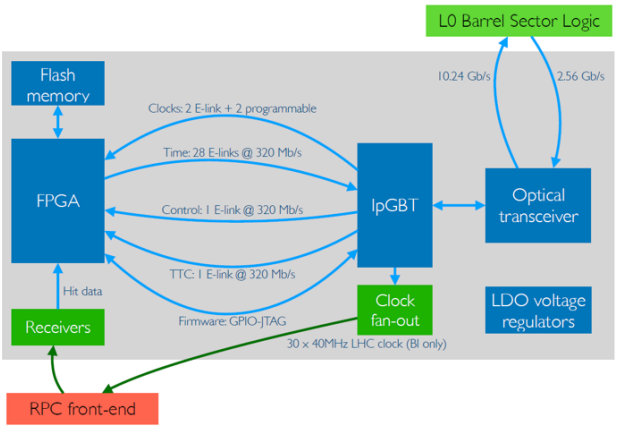

Figure 4. DCT block diagram.

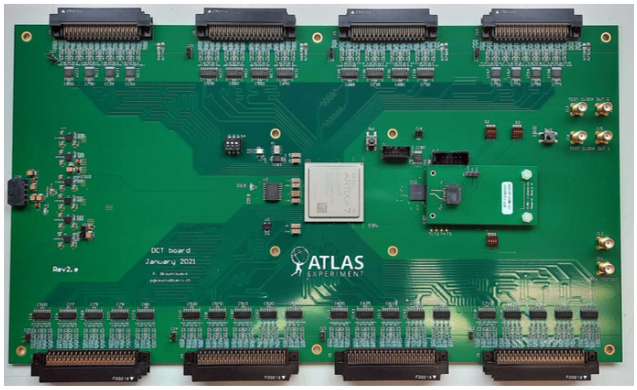

Figure 5. The first DCT prototype.

logic implemented in the FPGA will be different between the BM/BO and the BI layers: for the DCTs in the BM and BO regions, the FPGA will receive the RPC hit pulse signals and will perform the TDC and zero-suppression logic, while for the DCTs in the BI layer, the RPC data will arrive already digitized by the front-end boards, so the FPGA will implement only the zero-suppression logic. In both DCT types, the zero-suppressed data will be stored into the FPGA memory before being sent to the Low Power Gigabit Transceiver (lpGBT) [5], a radiation tolerant ASIC that will work as a serializer/deserializer and will handle the data transmission between the DCT and the barrel SL board.

The FPGA communicates with the lpGBT through electrical connections called *E-links*. 28 E-links at 320 Mb/s will transmit the RPC hit data and other monitoring parameters (temperature, voltage, hit rate) from the FPGA to the lpGBT. On the other direction, from the lpGBT to the FPGA one E-link at 320 Mb/s will send Time Trigger and Control signals and one E-link at 320 Mb/s will send control data. The lpGBT will provide four clocks to the FPGA, two with fixed phase and two fully programmable. Moreover, there will be a Slow Control E-link in both directions for general purpose usage (for example to upload the FPGA firmware into the flash memory).

The DCT will interface with the SL using the Versatile Link Plus module [6], consisting in a radiation tolerant optical transceiver (VTRX+). However, there are currently ongoing tests to evaluate if much less expensive commercial transceivers could be used in place of the VTRX+, without loosing in performance. The link from the SL board to the DCT is called *downlink* and has a bandwidth of 2.56 Gb/s with a user bandwidth of 1.28 Gb/s. The data are organized in 64-bit frames and are received by the lpGBT every 25 ns. 4 bits are used for the frame header, 2 for the IC-field (control information from SL), 2 for the EC-field (general purpose), 32 for the data and 24 for the Forward Error Correction (FEC) code to detect and correct transmission errors due to noise or Single Event Upsets. The link from the DCT to the SL board is called *uplink* and has a bandwidth of 10.24 Gb/s with a user bandwidth of 8.96 Gb/s. The data are organized in 256-bit frames and are encoded using FEC5 coding. The 256-bit frames are sent to the SL every 25 ns and are composed of 2 bits for the header, 2 bits for the IC-field, 2 bits for the EC-field, 6 bits for the LM-field (that carries back the downlink IC-field), 224 bits for data and 20 bit for FEC code.

V. LPGBT-SL Communication Test

One of the first fundamental tests that the DCT boards should undergo concerns certainly the communication with the SL. It is of primary importance indeed to check if the lpGBT ASIC [7] employed by the DCTs is able to encode and serialize the RPC hit data and if the FPGA of the SL board manages to deserialize and retrieving the original data frames. Moreover it is necessary to check if the data transmission is correctly carried out also in the opposite direction, from the SL to the lpGBT (and therefore to the DCT).

The first DCT prototype (Figure 5) has been produced and delivered at CERN, where it is currently undergoing the first tests to check if all components work properly. Therefore, the communication test presented in this work has been performed using KC705 Evaluation Boards of the Xilinx Kintex-7 family [8]. Since loopback mode for a lpGBT self-testing is prevented by the asymmetry between uplink and downlink data rates, two KC705 boards have been used for the test setup. On one board, the lpGBT-FPGA firmware, which provides the functions to be implemented by the FPGA of the SL boards, has been uploaded. On the other one, instead, a firmware implementation of the lpGBT ASIC, the lpGBT-Emulator, has been uploaded. The lpGBT-FPGA firmware [9] is made up by two main components: the downlink, to send data from the SL board to the lpGBT, and the uplink, to receive the data from the lpGBT. The downlink consists of a scrambler, an encoder, an interleaver and a TX gearbox. The uplink is made up by a frame aligner, an RX gearbox, a deinterleaver, a decoder and a descrambler. The MGT component, which serializes the outgoing data frames and deserializes the incoming ones, is not part of the lpGBT-FPGA project, and it has been instantiated on purpose. Also the logic to wrap up the downlink, uplink and MGT components has been implemented according to the specifications of the KC705 board. An MGT instantiation has been added also to the lpGBT-Emulator, and its firmware has been adapted to work with the KC705 board. For the communication test, the

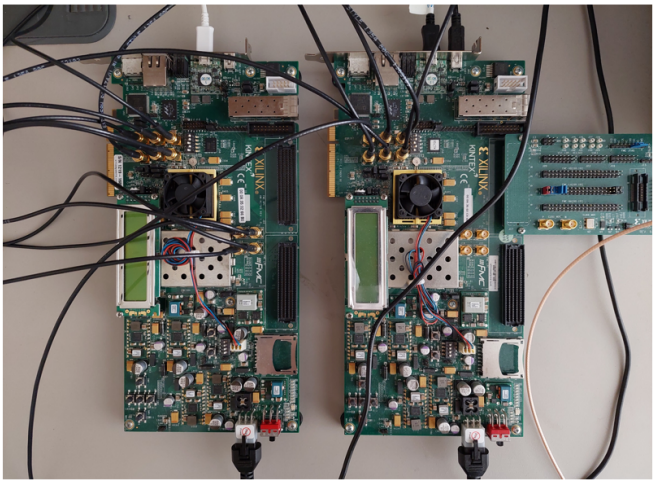

Figure 6. lpGBT-SL communication test setup.

differential signal coming from the lpGBT-FPGA MGT has been mapped to the input differential signal of the lpGBGT MGT, and viceversa the output signal of the lpGBT has been mapped as input signal to the lpGBT-FPGA MGT. To evaluate if the communication is successful, two simple counters have been used as user data to be transmitted from one board to the other one. One counter made of 32 bits and incremented every $25\,\mathrm{ns}$ is generated before the downlink chain in the board that stores the lpGBT-FPGA firmware. Another counter made of 224 bits, and incremented every $25\,\mathrm{ns}$ as well, is generated at the beginning of the uplink chain in the lpGBT-Emulator firmware. In both firmwares, some logic has been added to check if the counter has been retrieved and decoded correctly, and, if so, one of the LEDs on the board flashes with $1\,\mathrm{Hz}$ frequency.

The communication test described above has been done first with a software simulation using the Xilinx Vivado Design Suite software (2020.2 version) [10]. After having checked that both uplink and downlink work as expected, the hardware test setup has been prepared (Figure 6). The two firmwares have been uploaded on the corresponding KC705 boards, whose input and output signals has been connected as described above using coaxial cables. Since it is very important for the reference clocks of the two MGTs to be in phase with great precision, the $200\,\mathrm{MHz}$ clock necessary for the MGT operation has been generated in one of the two boards and then passed through coaxial cables both to the MGT of the same board and to the MGT of the other one. After the firmware upload, one LED on both the boards has started flashing with the expected frequency, meaning that the encoding, the transmission and the decoding of the frames works properly both for the uplink and the downlink. However it will be necessary to add in both firmwares some logic to check if there are any transmission errors.

VI. Conclusion

The much harsher conditions of operation at HL-LHC will make it necessary a substantial upgrade of the trigger and readout system of the ATLAS barrel Muon Spectrometer. During the Phase-II upgrade in Long Shutdown 3, a new layer of RPC will be installed and the RPC trigger and readout electronics will be replaced by new DCT boards, that will collect the RPC hit data and send them to the barrel SL boards, where the trigger algorithms will be run.

Waiting for the possibility to test directly the first DCT prototype, which is now undergoing other types of tests, a test bench has been developed using two KC705 Evaluation Boards to check that the data transmission between the lpGBT ASIC and the SL is performed correctly. For the test, a firmware that emulates the lpGBT functionalities has been uploaded on one of the two boards, and its back-end counterpart (the lpGBT-FPGA firmware) on the other one. The hardware test has given a positive result, pointing out that the communication between the two boards works properly.

The next step for the DCT testing is the adaptation of the lpGBT-FPGA firmware to the Virtex Ultrascale+ FPGA that will be effectively used by the SL boards at HL-LHC. The communication test will then have to be repeated using that FPGA and the DCT prototype sending in uplink some simulated RPC hit data, and eventually using cosmic ray data collected by a real RPC detector.

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