ATLAS LAr Calorimeter Commissioning for LHC Run-3

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Liquid argon (LAr) sampling calorimeters are employed by ATLAS experiment at the Large Hadron Collider (LHC) for all electromagnetic calorimetry in the pseudo-rapidity region $|\eta| < 3.2$, and for hadronic and forward calorimetry in the region from $|\eta| = 1.5$ to $|\eta| = 4.9$. After detector consolidation during a long shutdown, the LHC Run-2 started in 2015 and about 150 fb^{-1} of data at a center-of-mass energy of 13 TeV was recorded. With the end of Run-2 in 2019, a long period of shutdown began for the Phase-I detector upgrades. As part of the Phase-I upgrade, new trigger readout electronics of the ATLAS LAr calorimeter have been developed. Installation began at the start of the LHC shutdown in 2019 and is now completed, while a commissioning campaign is still underway to fully validate and improve stability of the new, higher granularity and precision Level-1 trigger system. This contribution gives an overview of the new trigger readout installation and commissioning, as well as the preparations for Run-3 detector operation and changes in the monitoring and data quality procedures to cope with the increased luminosity and pile-up.

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1. Introduction

The Liquid Argon (LAr) calorimeter [1] is one of the ATLAS majors sampling calorimeter with full azimuthal coverage, designed to measure primarily the trajectory, time and energy of electrons, photons and jets. The calorimeter is divided into various subdetectors with different segmentation geometries and absorber materials, such as a cooper, lead and tungsten (Figure 1). The LAr calorimeter system is composed of an electromagnetic (EM) calorimeter covering the region of pseudo-rapidity $|\eta| < 3.2$, a hadronic endcap (HEC) calorimeter covering $1.5 < |\eta| < 3.2$, and a forward calorimeter (FCAL) covering $3.1 < |\eta| < 4.9$. These elements are housed in two "endcap" and one "barrel" cryostats cooled at 87 K. When a collision takes place, incoming particles hit the absorber generating an electromagnetic shower which ionize the liquid argon by creating electric charges. These charges then drift due to the high voltage applied to the liquid argon and the electrodes measure generated current by a capacitive effect. Afterward, this signal is shaped, sampled and digitized, and four samples are used to reconstruct a pulse where the amplitude represents the amount of energy deposited at a given position in the detector.

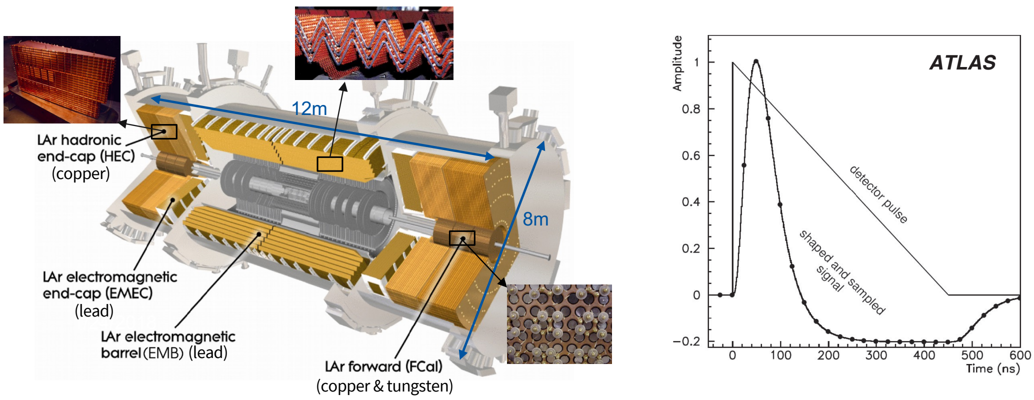

Figure 1. (left) Layout of the different subdetectors of the ATLAS Liquid Argon system [2]. The different sections of the calorimeter are labeled, along with their respective absorber materials. Photographs of the hadronic end-cap (HEC), electromagnetic barrel (EMB) and forward (FCal) calorimeters are overlaid [3]. (right) Overlap of the triangular ionization signal collected directly by the electrodes and the reconstructed signal after the shaper and sampler.

With a bunch collision frequency of 40 MHz, the system readout is not able to store every event, and trigger signals are used to select only the events of interest. The LAr calorimeter is expected to operate at a maximum frequency of 100 kHz, implying a reduction of the collision rate by a factor of 400. This reduction results in an allocated latency for the computation of the energies of up to 2.5 us. To satisfy such requirements, the adopted solution consists of reducing the units of the readout for which an energy deposit is calculated. This is achieved with the so-called Trigger Towers (TT), which are a combination of about 60 cells in depth for detector regions of $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$. A total of ~5400 TT signals cover the full calorimeter. The electronic trigger system combines the electric signals from the cells into TTs and the coarser granularity makes possible a fast enough computation of the corresponding energies.

After a successful period of data taking during Run-2 (years 2015-18), the LHC will operate with higher instantaneous luminosity and pile-up in Run-3 (years 2022-24). The mean number of proton-proton interactions per bunch crossing is expected to increase from $\langle\mu\rangle = 33$ to $\langle\mu\rangle \approx 80$, the luminosity from 1.9×10^{34} cm^{-2} s^{-1} to 3×10^{34} cm^{-2} s^{-1} and the center of mass from $\sqrt{s}$

=13 TeV to ~14 TeV. To keep the same L1 trigger bandwidth of 100 kHz without raising the transverse energy (E_T) threshold, the trigger discrimination performance is improved during Phase-I upgrade (years 2019-2021). This is achieved by enhancing the granularity of the trigger. The TTs are replaced by the so-called Super Cells (SC), which have higher lateral and longitudinal segmentation. Approximately 34000 SC will provide up to four-layer information and a tenfold increase in granularity. Precisely, $\Delta\eta \times \Delta\varphi = 0.1 \times 0.1$ for the pre-sampler and back layers and $\Delta\eta \times \Delta\varphi = 0.025 \times 0.1$ for the front and middle layers. This will allow improving L1 algorithms for a better discrimination between photons, electrons, taus and jets, and new Feature EXtractor (FEX) modules will be able to use topological shower shape variables to discriminate between these different objects.

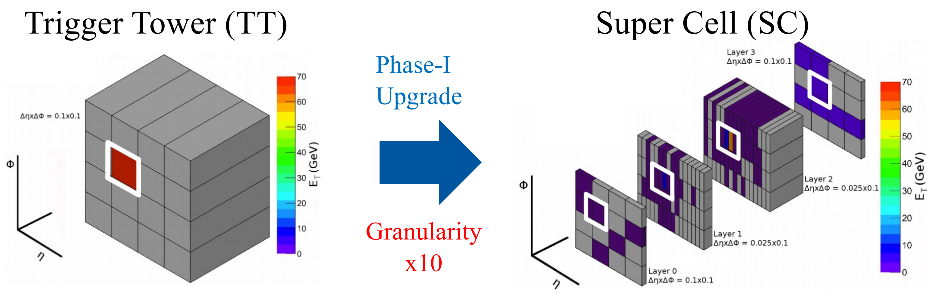

Figure 2. Simulation of the energy deposit of a 70 GeV electron in the EM calorimeter reconstructed with a legacy Trigger Tower (left) and the equivalent for the new Super Cell (right) [4].

2. LAr readout electronics

The LAr readout electronics is divided into a front-end and a back-end system, both interconnected with optical fibers and cables. The front-end system is mounted directly on the detector and is designed to tolerate harsh radiation, while the back-end system resides in an underground service cavern separated from the experiment.

The LAr calorimeter has 182418 channels which are routed from the cryostat to the baseplanes of the Front End Crates (FEC) [5]. A total of 58 FECs are installed radially around the detector, where each crate has two baseplanes hosting the following legacy system boards: Front End Boards (FEB), Tower Builder Boards (TBBs), calibration boards and controller boards. The FEBs are responsible for processing up to 128 channels for a specific layer of the calorimeter. The incoming ionization signal for each channel is first split into one of the three different gains (low, medium, and high), and then for each gain the signal is shaped using a CR-$(RC)^2$ analogue filter by producing the pulse shape presented in Figure 1. The shaped signals are sampled at LHC bunch-crossing frequency of 40 MHz and stored in a Switched Capacitor Array (SCA) analog memory buffer until a Level-1 (L1) trigger [6] is received. Upon the arrival of the L1 trigger signal, the stored analog signals are digitized and transmitted using optical fibers to the Readout Drivers (ROD) on the back-end side. In addition, the signals going out of the amplifier are routed to the Linear Mixer electronics and the Layer Sum Boards (LSB) housed on the FEB, to prepare the analog sums needed for the trigger system. These analog sums are then transmitted through the FEB backplanes to the TBBs, which sum data from the four layers of the calorimeter to form the legacy Trigger Towers (TT). With respect to the other two boards housed on the FEC, the calibration boards are used to inject known pulse shapes into the detector for calibration of the electronics; and the controller boards are used to receive the configuration and monitoring commands as well as the Timing Trigger and Control (TTC) signals from the TTC crates on the back-end side.

3. LAr trigger readout upgrade

In order to provide the higher granularity trigger information from the SCs to the L1 Calorimeter (L1Calo) system, both front-end and back-end electronics have been upgraded. Figure 3 illustrates a schematic block diagram of the Phase-I trigger upgrade, where the new components are indicated with red outlines and arrows.

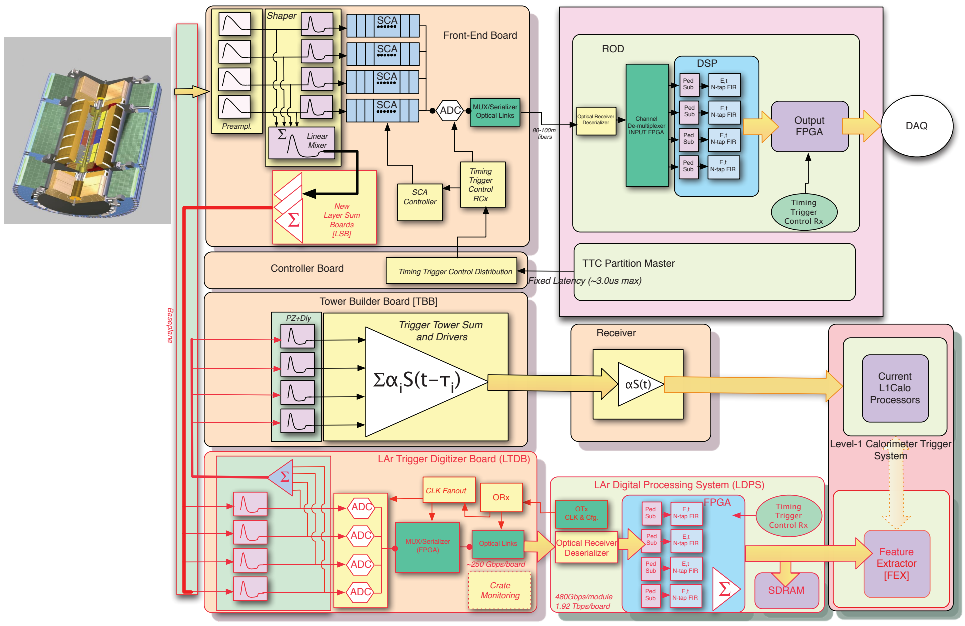

Figure 3. Schematic block diagram of the Phase-I upgrade LAr trigger readout architecture [4]. The new components are indicated by the red outlines and arrows.

The most significant difference is the addition of 124 new on-detector LAr Trigger Digitizer Boards (LTDB), which process and digitize up to 320 SC for every collision at 40 MHz. In order to house the new LTDBs in the FEC, the baseplanes have been replaced with new ones including the necessary number of slots. The new baseplanes also introduce changes to accommodate the routing of the new paths: (1) the routing of SC sums from the LSB to the LTDB, and (2) the routing of TT sums from the LTDB to the TBB. The LSBs, hosted in the FEBs, have also been replaced to provide additional analog sums onto the baseplanes to form the SCs. These updates allow operating the legacy and new digital triggers concurrently, which eases the commissioning of the new system and offers a fallback solution in case of unforeseen problems. Another goal of the LTDB is to transmit the digitized SC values to the back-end via serial optical links (~7 k fibers in total). Each LTDB has up to forty fibers for the datalinks at 5.12 Gbps (8 SC per fiber) and ten fibers for the control and monitoring links at 4.8 Gbps. The reception of this SC data on the back-end side and its transmission to the new FEXes is handled by the new LAr Digital Processing System (LDPS). The LDPS receives the ADC data and align timing information, reconstructs the E_T for each SC, identifies the bunch crossing ID, corrects the baseline, and transmits the results to the L1 trigger modules with a latency smaller than 375 ns. This system is composed of four LAr Trigger processing Mezzanines (LATOMEs), one LAr Carrier (LArC) card and one Rear transition Module (RTM). The four LATOMEs are hosted in one LArC, and the RTM connects with the LArC by forming a single blade that is plugged into a slot of an Advanced-TCA (ATCA) crate. In addition, a Platform Management Controller (IPMC) is housed into the LArC to deal with the hardware control and monitoring of each blade. To achieve a good enough compacity and attain required high throughput demand and strict latency requirements, the LArC and LATOME are operated by high-performance commercial FPGAs, Xilinx Virtex 7 and Intel® Arria-10 respectively.

3.1 Installation status

The end of the long shutdown (LS2) is approaching, and according to planned schedule the installation of both new front-end and back-end LAr electronics is now finalized. On the front-end side, the replacement of all baseplanes (114) have been completed. A tedious work in a restricted space which first required the removal of all the boards in the FECs. These boards were then transported to the surface by crane (~1700 boards) to replace all the cooling plates and aging hoses, as well as to exchange the LSBs on the FEBs (1524). This operation, which also involved leak tests, is now completed and all the FEBs, TTBs and new LTDBs (124 boards, 7 flavors) are reinserted in the new baseplanes on the FECs.

On the back-end side, the LDPS installation in the ATLAS service cavern proceeded in parallel to the front-end installation. At this moment, all the LDPS boards are installed and cabled with corresponding LTDB using optical fibers. In total 30 LArC hosting 116 LATOME grouped by readout regions are connected in three ATCA crates ready to process the signal of approximately 40 k channels. In addition, all the network, TTC, TDAQ/local readout, Detector Control System (DCS) and run control infrastructure is in place.

3.2 Commissioning status

Even if the main readout electronics has remained unchanged during the Phase-I upgrade, the routing path and much of the contributing electronics have been updated or refurbished. The LSBs on the FEBs have been replaced and now the signals are routed through new baseplanes, as well as refurbished FEBs are now reinstalled in different slots within the various FECs. Therefore, verifying the performance of the main redout is indispensable to guarantee that the system is operating as it was before the upgrade. Connectivity scans have been used to check that all the channels and FEBs are connected correctly, while calibration runs have been taken for comparison with reference runs from Run-2. The calibration runs provided detailed information on noise levels and calibration coefficients, which served to confirm that the system is performing as it was in Run-2: (1) no significant deviations in the electronics noise levels and (2) comparable calibration coefficients. For instance, Figure 4 shows the overlap between the noise levels between the collected data in the middle layer of the EMBA before and after the upgrade.

The legacy trigger readout path has also been updated, as mentioned in Section 3, the analog legacy sums are now routed through the LTDBs before arriving to the TTBs. This longer path introduces a delay in the L1 system for the reception of the TT sums of the different layers, that must be measured and calibrated to achieve a reliable trigger decision. This is an important step to guarantee the expected performance of the trigger. Following the refurbishment of each crate, gain and timing scans have been conducted in order to check the connectivity and measure the introduced timing shift between the different layers. As an example, Figure 4 depicts the obtained results before and after applying the timing corrections in the EMBA, where a 10 ns difference is found that is consistent with the increased path length.

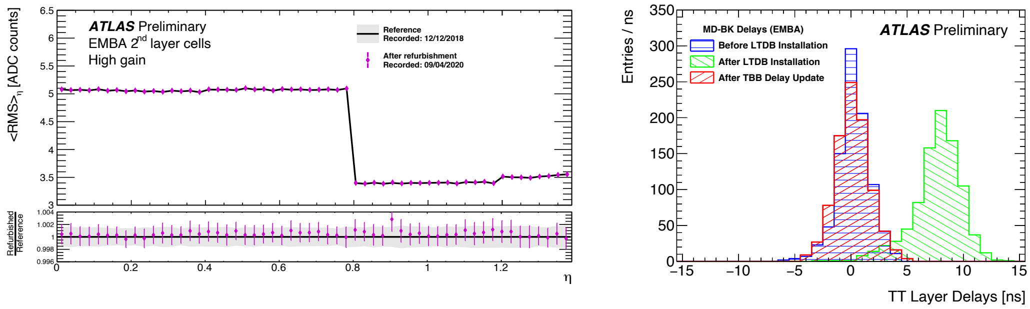

Figure 4. (left) The mean value of the RMS of the pedestal for a given η range measured during Run-2 (black line) compared to values measured after the Front End Boards refurbishment (purple dots) during LS2 [7]. The displayed uncertainties are computed as $\sigma_{rms,cells}/\sqrt{N_{cells}}$, where $\sigma_{rms,cells}$ are the RMS values over the cells in the given η range and N_{cells} is the number of cells in the given η range. The step at η=0.8 can be related to a change of the electrode geometrical structure in this region. (right) The delays of signals from the back-layer (BK) with respect to the middle-layer (MD) introduced by the new LTDBs for the L1 TT signals at the L1Calo system [8].

Concerning the validation of the new digital trigger readout path, different calibration patterns are used for comparison with the main readout. For instance, Figure 5 shows a delay run pattern used to reconstruct the full pulse shape by generating pulses with a single-input current signal with increasing time steps of 1.04 ns. Similarly, Figure 5 shows a ramp run, ADC versus DAC, where the ADC increases linearly with deposited E_T up to the saturation of the SC pulse around 800 GeV. From these runs, calibration constants for energy reconstruction such as the pulse position or gain slope are determined from the understanding of the expected SC output. Once the system is calibrated, computed energies by the LDPS are compared with offline results. In this case a strong agreement is found with differences below 1%.

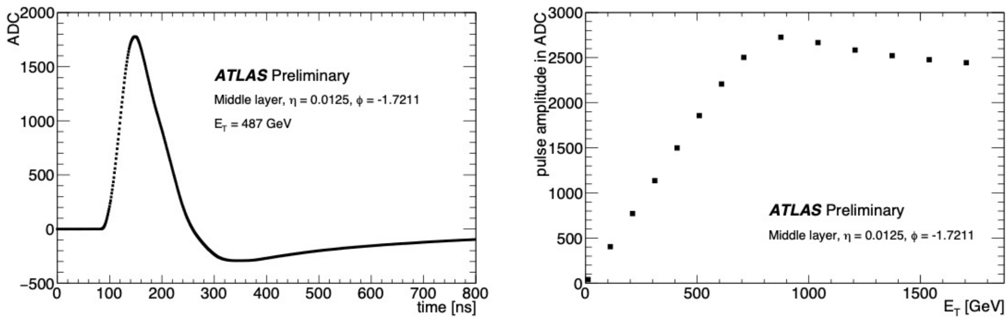

Figure 5. Calibration pulse shapes are recorded with the Phase-I trigger system [7]. (left) Pulse shape of a SC in EMBA obtained from a delay run with an injected charge of DAC = 4400, corresponding to a transverse energy of 487 GeV. (right) Measured amplitude (ADC) of calibration pulses as a function of injected current (DAC) from a ramp run for the same SC.

4. Conclusion

In this contribution, an overview of the installation and commissioning of the ATLAS LAr calorimeter trigger readout for Phase-I upgrade has been presented. Despite the challenges imposed by recent pandemic, the installation of both front-end and back-end electronics has been effectively completed. The commissioning is still in progress, but excellent results have been obtained so far. The main readout has been already validated, demonstrating no major deviations from the performance observed during Run-2. Connectivity and mapping checks have been used to validate newly connected hardware, and calibration constants have been applied to synchronize the legacy and new trigger system. Required firmware and software essential functionalities are in place, and the new trigger system has already proven the ability to reconstruct and digitize calorimeter signals. Currently, an extensive campaign is still ongoing to improve stability, efficiency and robustness of the system; however outstanding progress has been made and obtained results serve to confirm that the system is in the right direction to keep providing excellent performance during Run-3.

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