Development of the ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

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ABSTRACT: A new era of hadron collisions will start around 2027 with the High-Luminosity LHC, that will allow to collect ten times more data that what has been collected since 10 years at LHC. Five times higher instantaneous luminosity i.e. 8 billion collisions per second will happen. In order to withstand with the new specifications, the ATLAS Liquid Argon Calorimeter readout electronics will be upgraded during the 2025-2027 shutdown. Four subsets of the whole readout chain are concerned and are described here.

Two of them are front-end electronics dedicated to the precise sensing of the detector cells, the digitization, the serialization and the optical transfer of the data to the off-detector electronics. The front-end electronics has to be tolerant to radiation up to 1.4 kGy.
The first subset is the new front-end board. It will amplify, shape and digitize on two gains the ionization calorimeter signal. Multiple silicon circuits have been designed for this purpose. The second is the new calibration board which will allow the precise calibration of all 182 468 channels of the calorimeter by injecting well known amplitude and shape pulses.

The off-detector electronics is also made of two subsets. One is taking care in distributing the timing, trigger and control interface to the on-detector electronics. The other handles the processing of huge data bandwidth coming from the 1 524 front-end boards, i.e. 31 912 optical fiber at 10.24 Gbps corresponding to about 320 Tbps to compute signal energy, time-stamping and send the data to the online processing system.

KEYWORDS: High-Luminosity Large Hadron Collider; Liquid Argon calorimeter; Readout electronics.

ATL-LARG-PROC-2021-009
15 November 2021

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1. Introduction

ATLAS detector[1] is one of the four experiments of the Large Hadron Collider (the LHC) which is the world's largest and most powerful particle accelerator. The detector is designed to detect some of the tiniest yet most energetic particles ever created on earth. The High Luminosity LHC (HL-LHC) is an upgrade of the current LHC which aims to increase the nominal instantaneous luminosity by a factor five with a start of operation from 2027. Following five years of design study and R&D, this challenging project will require about ten years of developments, prototyping, testing and implementation.

The ATLAS LAr calorimeter readout electronics upgrade for HL-LHC is carried out in two steps. The Phase-I Upgrade ending in October 2021 increases the granularity of the calorimeter trigger system. The Phase-II Upgrade will allow to digitize and readout the full 182 500 calorimeter cells at a 40 MHz frequency and provide data to the trigger and acquisition systems. This paper will focus on this Phase-II readout electronics.

As illustrated in **Figure 1**, the signals created in the sensing cells of the detector are preamplified, shaped and digitized by the Front-End Boards (FEB) before being transmitted via optical links to the Liquid Argon Signal Processor boards. These will calculate energies and will send data to the trigger and the online acquisition system. To get the best precision measurements, very precise clocks and timing is needed. This is carried out by the Timing System boards. Calibration boards are also designed to provide accurate pulses to calibrate the channels' readout.

These Phase-II electronics will be described in the following sections and will be organized distinguishing the front-end electronics mostly related to analog design and the off-detector electronics which is related to digital design electronics.

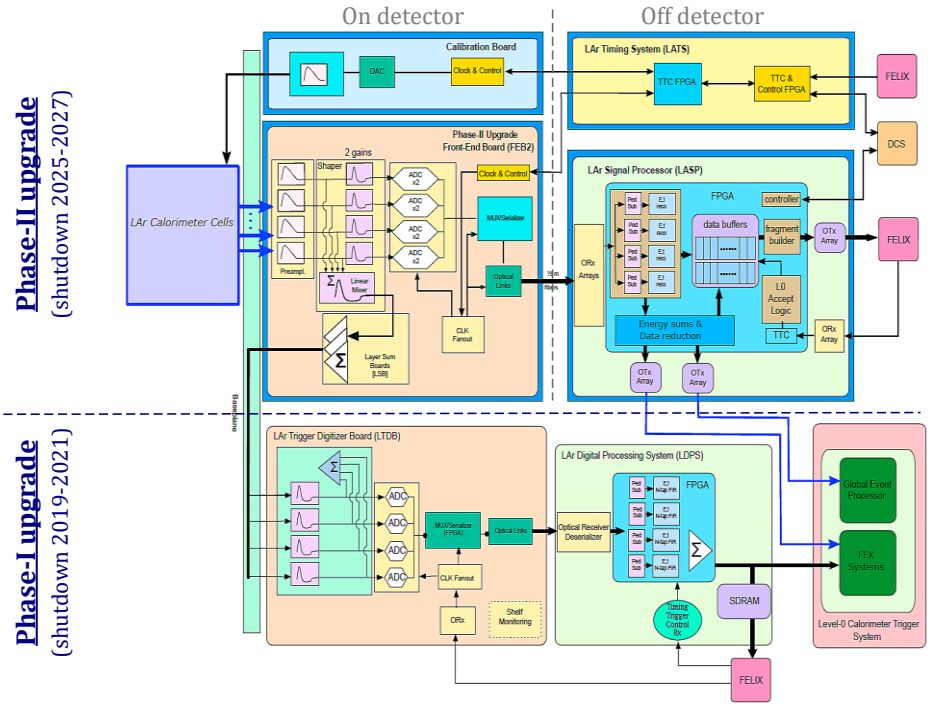

Figure 1. Scheme of the Phase-I and Phase-II Upgrade readout electronics pointing out the On- and Off-detector electronics as well as timing, calibration (to detector), and readout path (from detector).

2. On-detector electronics

2.1 On-detector specifications

The on-detector electronics specifications are driven by the performance requirements regarding the measurement of the particle energy deposit in the calorimeter cells.

Considering the minimum and maximum energy deposited without saturating, the energy must be digitized with a 16-bits dynamic range. The linearity must be better than 0.1% at least on the first 10% of the dynamic range. The front-end electronics has to be radiation hard [2] up to a total ionizing dose of 1.4 kGy, a non-ionizing energy loss of 4.1×10^{13} neq/cm² and a single event effect tolerance such that no upsets are observed in exposure to 10^{13} h/cm². The front-end electronics must be able to readout the entire calorimeter at a 40 MHz frequency and to pre-amplify, shape, digitize and send the raw data at this rate to the off-detector electronics.

2.2 Front-end boards

To readout the 182 500 calorimeter cells, 1 524 front-end boards are foreseen. Each front-end board will readout up to 128 LAr calorimeter channels with two pre-amplification gains to get the desired 16-bit dynamic range. Therefore 163 Gbps per board will be transferred via custom serializers and transceivers on 10 Gbps optical links.

The analog signal pulse is split into two overlapping gain scales with a gain ratio of around 23 and shaped by a CR-RC² shaping function. Two prototypes have been developed in 130 nm TSMC CMOS technology, namely the ALFE (ATLAS Liquid Argon Front-End) and LAUROC (Liquid Argon Upgrade Readout Chip). ALFE has been chosen after the preliminary design review. An Integral Non Linearity below 0.2% on the high-gain output has been reached, together with an equivalent noise current (ENI) below 350 nA (120 nA) for a 25 ohm (50 Ohm) termination

and a power-supply rejection ratio (PSRR) larger then 10 dB up to 1MHz as shown in Figure 2, left.

Another Application Specific Integrated Circuit (ASIC), the COLUTA ASIC, has been designed in 65 nm TSMC CMOS technology to digitize the pre-amplified and shaped signals at 40 MHz with two gains with a 14 bit resolution. The proposed ADC is divided into a first-stage 3.5-bit multiplying digital–analog converter (MDAC) and a second-stage 12-bit SAR (Successive Approximation Register) ADC. Each circuit deals with 4 channels, meaning 8 ADC per chip. Low noise and good long-term stability have been observed. The following performances have been measured: a cross-talk bellow 0.1%, a coherent noise bellow 0.2 LSB and an Effective Number Of Bit (ENOB) of 11.32 bit as illustrated in **Figure 2**, right.

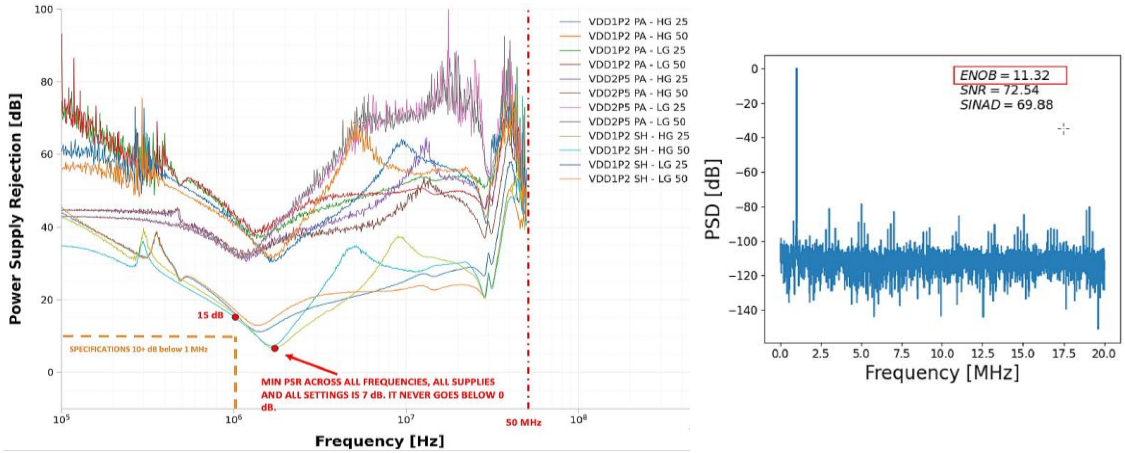

Figure 2. Left: the power supply rejection ratio of the ALFE ASIC for the pre-amplifier and shaper, for the two gains and 25 and 50 Ohm termination.
Right: the Power Spectrum Density of the COLUTA ASIC.

2.3 Calibration boards

The front-end readout will be calibrated and characterized through the injection of pulses with well known amplitude and shape provided by dedicated calibration boards. Such boards are designed to fulfill the on-detector specification requirements described in section 2.1.

A calibration board is foreseen to embed 32 ASICs and each of them has 4 output channels. Each calibration line will allow to calibrate eight calorimeter channels. A total of 130 boards will be installed on detector.

The pulsing system and the DAC are implemented on two separate ASICs. The CLAROC (Calibration of Liquid ARgon Output Chip) pulser has been designed in a 180 nm XFAB HighVoltage CMOS technology and contains a high-frequency switch and current mirrors. Then a 16-bit DAC has been implemented on the LADOC (Link And DAC of CLAROC) chip using 130 nm TSMC CMOS technology. A 32-channels board CABANON (CAlibration Board with 32-chANnels for demonstratiON) has also been developed for test and characterization.

2.4 On-detector integration

The integration of the front-end ASICs into the FEB is done with a succession of partially integrated board (slices) with increasing complexity.

The slice test board integrates the main components of the final system which are: the powering network and input protection, the slow control of all the ASICs via I²C communication, the data readout of 8 COLUTA chips and the data transmission thanks to custom radiation-hard gigabit transceivers. It also embeds the signal inputs via backplane connectors for subsequent crate integration. The board will be used to characterize the FEB prototypes and to develop the software and firmware for the final production boards.

3. Off-detector electronics

3.1 Off-detector specifications

The off-detector electronics upgrade concerns two subsystems, each with its own specifications.

The LAr timing system distributes the Timing, Trigger and Control interface (TTC) to the whole on-detector electronics (FEB and calibration boards). That means to deliver a precise 40 MHz clock synchronized to the LHC machine clock with a jitter at the FEB level of 5 ps RMS, as well as bunch crossings and calibration signals. It also handles the configuration and monitoring of the thousands ASICs and components embedded on the 1 524 FEBs and 130 calibration boards.

The LAr Signal Processor (LASP) will receive the 182 500 LAr calorimeter cells' data coming from the FEBs on 31 912 optical fibers at 10.24 Gbps, i.e. 320 Tbps to process. This processing consists in transmitting relevant data to the trigger, buffering all data until a trigger decision is received, and finally forwarding triggered data the data acquisition (DAQ) systems..

3.2 LAr timing system

The LAr timing functionalities will be achieved by the Liquid Argon Timing trigger cOntrol distribUtion and fRoNt End moniToring/ConfiguraTion (LATOURNETT) board. The design is carried out gradually. A first step consists in associating a custom FMC board embedding the foreseen SI5394 clock component and SFP+ optical transceivers together with a Cyclone 10 devkit. The goal is to validate clocks and data communication. As a second step a LATOURNETT power board has been designed to verify the power tree.

3.3 LAr signal processor

The LASP system will be composed of 200 to 400 LASP boards, depending on the number of FEBs that a LASP will be able to process. As described in the section 3.1, the requirements are tough. Indeed, a LASP test board has been designed to validate crucial design challenges such as power and cooling. The ATCA shelf cooling limits to 350 W/slot. The high speed links can provide up to 25 Gbps and the high density and complexity of the board is important.

This ATCA LASP test board embeds two Intel Stratix 10 FPGAs. In order to test different technologies embedded on Stratix 10 variants, a SX type with ARM processor (2.8M logic elements) and a MX type with high-bandwidth DRAM memory (2.1M logic elements) have been chosen. An INTEL MAX10 FPGA is also used as a controller and 24 Firefly optical transceiver modules are mounted, 12 per FPGA (8 x 12 RX at 11Gbps, 3 x 12 TX at 11 Gbps, 1 x 4 RX/TX at 25 Gbps). The PCB itself is a high end design with more than 4 000 components, 20 layers (6 for signals, 14 for power and ground), fabricated in Megtron 6 dielectric material and 2.4 mm thickness.

As shown on **Figure 3**, the first test board has been produced and is currently under test.

This LASP board is associated to an sRTM board designed to extend the LASP optical links capabilities. It embeds 40 TX links at 25 Gbps to the forward feature extractor trigger.

In addition, in order to support the LASP firmware development before the LASP test board being available, a custom FMC mezzanine board embedding a voltage controlled crystal oscillator, a SI5395 clock synthesizer and 4 Firefly optical transceivers has been designed. The aim of this board is to provide a mezzanine card for the Intel Stratix 10 devkit via the FMC connector. This will extend the capabilities of the devkit and thus obtain a mini-LASP system.

Finally these LASP electronics under development will be a platform that will also allow to implement and experiment with machine learning on FPGAs. First results are promising [3].

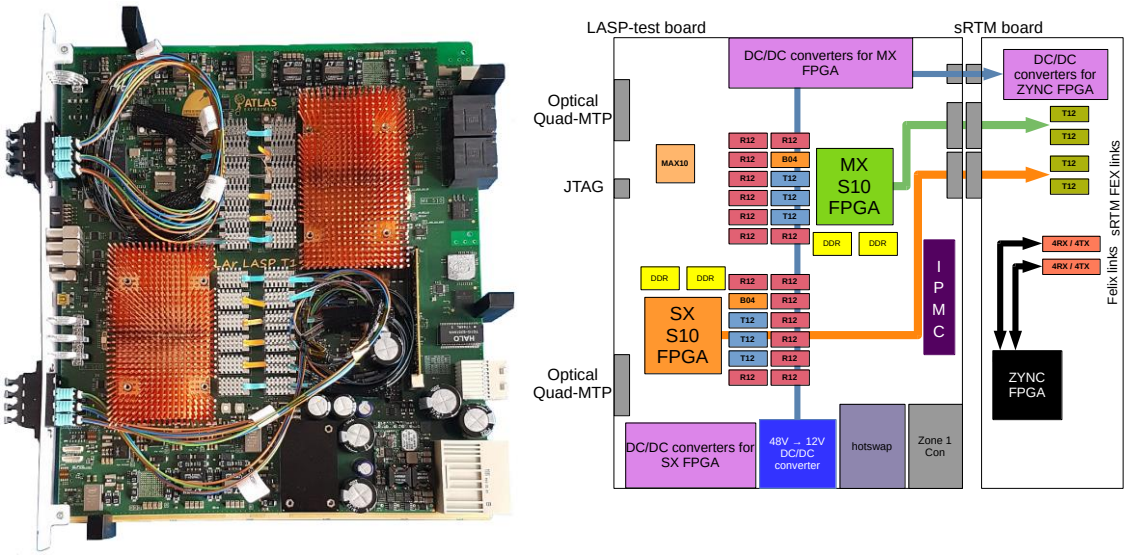

Figure 3. Left: the ATCA format LASP test board with all the components mounted.
Right: the synoptic of the LASP test board and the associated sRTM board.

4. Summary

The ATLAS Liquid Argon Calorimeter readout electronics will be upgraded during the 2025-2027 shutdown. Such electronics have to fulfill the crucial long term reliability to be operated during more than a decade. The architecture and test results from the front-end to back-end electronics have been described.

Acknowledgments

The author would like to thank the organizers for a very fruitful online conference.

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