Prepared for submission to JINST

Topical Workshop on Electronics for Particle Physics - TWEPP2021
20 - 24 September, 2021
CERN

Integration and commissioning of the ATLAS Muon-to-Central-Trigger-Processor Interface for Run-3

S. Perrella,[a,1] **Y. Afik,**[a] **A. Armbruster,**[a] **P. Czodrowski,**[a] **N. Ellis,**[a] **S. Haas,**[a] **A. Koulouris,**[a] **A. M. Kulinska**[a,b] **A. Marzin,**[a] **T. Pauly,**[a] **V. Ryjov,**[a] **L. Sanfilippo,**[a] **R. Simoniello,**[a] **R. Spiwoks,**[a] **P. Vichoudis,**[a] **M. Wyzlinski,**[a,b] **and T. Wengler**[a] **on behalf of ATLAS TDAQ Group**

[a] *CERN,*
Swizterland
[b] *AGH University of Science and Technology,*
Poland

E-mail: sabrina.perrella@cern.ch

Abstract: The Muon-to-Central Trigger Processor Interface was completely redesigned as part of the ATLAS Level-1 trigger upgrade for Run 3 of the Large Hadron Collider. The new system is implemented as a single AdvancedTCA module, using three large state-of-the-art FPGAs and high-density fiber-optic modules. Trigger information from the muon trigger detectors are received through 208 high speed links, while 60 links are used to send processed trigger information to the L1 Topological Trigger Processor and the Central Trigger Processor. Extensive integration tests with all input and output systems have shown that the data transfer is stable and reliable. We present results from integration tests with connected sub-systems as well as commissioning of the The Muon-to-Central Trigger Processor Interface in the ATLAS experiment.

Keywords: Trigger concepts and systems (hardware and software); Large detector systems for particle and physics; Digital electronic circuit.

ATL-DAQ-PROC-2021-017
15 November 2021

[1] Corresponding author.

Contents

1 Introduction

The Muon-to-Central Trigger Processor Interface (MUCTPI) is part of the Level-1 trigger system (Figure 1) of the ATLAS experiment [1]; a system with the aim of reducing the event rate from the bunch crossing (BC) rate of 40 MHz to a maximum rate of 100 kHz.

The MUCTPI receives information on muon candidates from the Resistive Plate Chambers (RPC) and the Thin Gas Chambers (TGC). It counts the muon candidates with a transverse momentum (p_T) within one of the sixteen programmable thresholds (trigger multiplicity), avoiding the double counting of muon candidates in different sectors (overlap handling). It sends the trigger multiplicity of each p_T threshold to the Central Trigger Processor, CTP, which makes the final Level-1

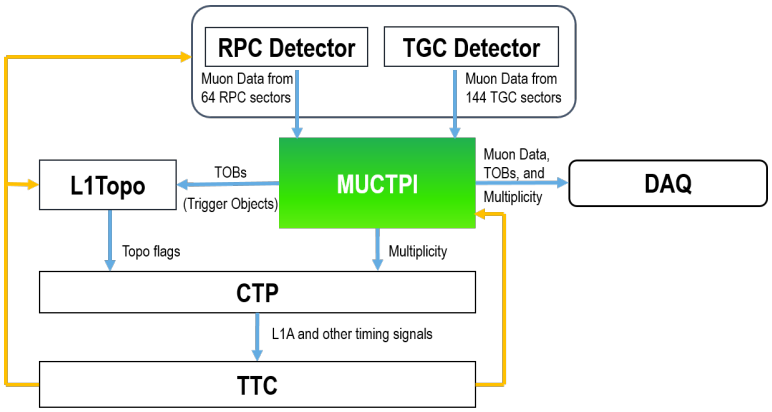


Figure 1. The Level-1 Trigger System showing the data path to and from the MUCTPI.

Accept decisions (L1A). The MUCTPI also extracts information on muon candidates relating to topological signatures, sorts them by their transverse momentum and sends Trigger Objects (TOBs) to the Level-1 Topological Processor (L1Topo). Upon arrival of the L1A signal, the MUCTPI further sends the TOBs and the multiplicity to the Data Acquisition (DAQ) system. The data transfer from and to the MUCTPI is synchronous with the 40 MHz BC clock being distributed via the Timing, Trigger and Control (TTC) system.

2 MUCTPI System

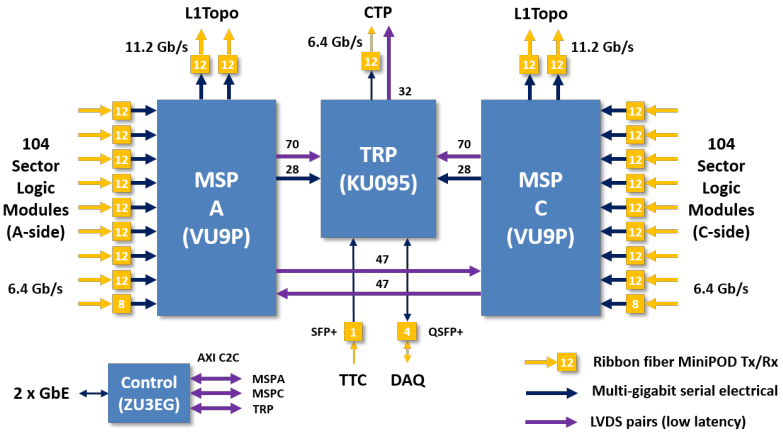


Figure 2. MUCTPI architecture.

The MUCTPI for Run 3 was completely redesigned [2]. The new MUCTPI is a highly-integrated system implemented on a single AdvancedTCA module, which replaces the 18 VMEbus modules used until the end of Run 2 [3]. The new MUCTPI system (Figure 2) is based on three large state-of-the-art Xilinx FPGAs: two VU9P FPGAs, namely Muon Sector Processor, MSP, and a KU095 FPGA namely Trigger Readout Processor, TRP. Taking advantage of the large number of multi-gigabit transceivers (GTs) and the 12-channel ribbon fiber optics transmitter and receiver modules (MiniPODs), it allows a higher aggregate bandwidth of around 2 Tb/s, compared to ~280 Gb/s for the old MUCTPI.

The two MSP FPGAs receive the muon candidates through 208 serial optical links running at 6.4 Gb/s. They take care of the input data timing alignment, the synchronization to the BC clock, and the overlap handling. The MSPs also send up to 16 TOBs to two L1Topo modules, using 16 of the 48 optical links running at 11.2 Gb/s. The TRP collects and merges the trigger information received from the two MSP FPGAs and sends trigger multiplicity information to the CTP over an optical link running at 6.4 Gb/s. The TRP FPGA also receives, decodes and distributes the TTC information. In addition, it sends all relevant information to the DAQ system.

A Xilinx ZU3EG multiprocessor System-on-Chip (SoC) Controller runs the software to interface the MUCTPI to the ATLAS run control system. It loads the configuration bitstreams into the three FPGAs. It is also used to access the MUCTPI functionality via software for testing and monitoring.

Three different prototypes were designed, built, tested, and fully qualified for Run 3. They differ in the architecture of the MSP FPGAs (Ultrascale for version 1 vs Ultrascale+ for version 2 and 3), and of the SoC (32-bit for version 1 and 2 vs 64-bit for version 3).

3 Integration Tests

Integration tests have been performed with the MUCTPI transmitting data to L1Topo and to the CTP in order to confirm the reliability of the data transfer. The Integrated Bit Error Ratio Tester (IBERT) core from Xilinx was used to acquire eye diagrams, bi-dimensional plots of the error distribution across the Unit Interval (UI), and to estimate the Bit Error Rate (BER) for the all 60 optical links. For all cases, the test data pattern was set to 32-bit Pseudo Random Binary Sequence (PRBS-31). In addition, latency measurements and synchronization tests were performed.

3.1 L1 Topo

The integration tests with the L1Topo were performed with the MUCTPI version 2 and the L1 Topo prototype, both using UltraScale+ GTY transceivers. For all the 48 optical links, the BER test showed an error-free transmission of more than 560 Tb. Zero errors were found when performing the BER tests with a 7 dB optical attenuator. The acquired eye diagrams show a wide open eye (see Figure 3a), with a horizontal opening ranging from 54% to 72%.

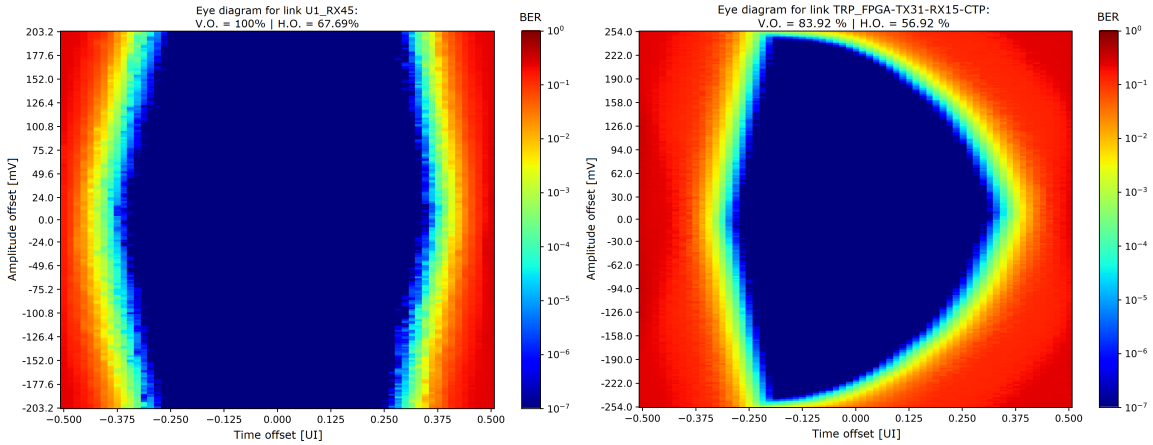
Synchronization tests were done in order to verify if data sent by the MUCTPI could be received by the L1Topo synchronously to the BC clock and without errors. For each MSP, a playback memory was used to generate specific values for 16 TOBs and snapshot memories on the L1Topo board were used to record data during 4 096 bunch crossings. No errors were detected on the recorded data and on the Cyclic Redundancy Check (CRC), even after multiple resets.

In order to measure the data transfer latency from the MUCTPI output to the input of the L1topo, dedicated firmwares were used. On the two boards, flags were generated when data belonging to a specific Bunch Crossing Identifier (BCID) were transmitted and received. Connecting the flag signals to the oscilloscope, a latency value of ~4.5 BC clock period was measured. The phase of transmitter and receiver flags stayed unchanged after power cycling and resetting both systems.

3.2 CTP

The integration tests with the CTP were performed with the MUCTPI version 3 and the CTPCORE+ board [4]. For this setup, the MUCTPI uses UltraScale+ GTY transceivers, whereas the CTP uses series-7 GTX transceivers. After an overnight BER test (~320 Tb data transmitted), no errors were found on any of the 12 optical links. Also, the eye diagrams look good, with a vertical opening ranging among 80% and 86%, and the horizontal opening among 54% and 60%. Figure 3b shows a typical eye diagram.
Tests were done in order to verify the correctness of the multiplicity sent from the MUCTPI to the CTP. Playback memories were used for generating specific patterns in the TRP, and an Integrated Logic Analyzer Core was connected to the synchronized inputs of the CTP to record data. No errors were detected on the recorded data and on the CRC value, even after multiple link reconfigurations.

In addition, the latency was verified to be constant, checking that the data belonging to a specific BCID are always received with the same offset with respect to the BCID internally generated on the CTP board; the offset kept constant after multiple resets.



(3a) Typical eye diagram for the MSP to L1Topo link. (3b) Typical eye diagram for the TRP to CTP link.

Figure 3. Eye diagrams acquired by the L1Topo Ultrascale+ FPGA (a), and the Virtex-7 CTPCORE+ FPGA (b).

4 Software

In the MUCTPI system the software is used for systematic diagnostic tests in the laboratory and in the experiment, for firmware validation, and for the regular running in the experiment.

4.1 Firmware Validation

In order to test the MUCTPI internal data path (Trigger and DAQ) custom software was developed for generating files which reproduce the trigger candidates of RPC and TGC. In parallel, a collection of high-level Python simulations were developed, which generate output files identical bit-per-bit to the expected MUCTPI hardware outputs.
The muon data generator produces files, which are loaded into the hardware and the simulation. The output from the hardware is then written to one or more files, which are then compared with the files produced by the simulation. Using this procedure, the main MUCTPI firmware features (overlap handling, multiplicity calculation, TOBs encoding and sorting, event monitoring) have been validated as well as the DAQ path (at least partially, since high rate tests are yet to be done).

4.2 TDAQ Run Control Applications

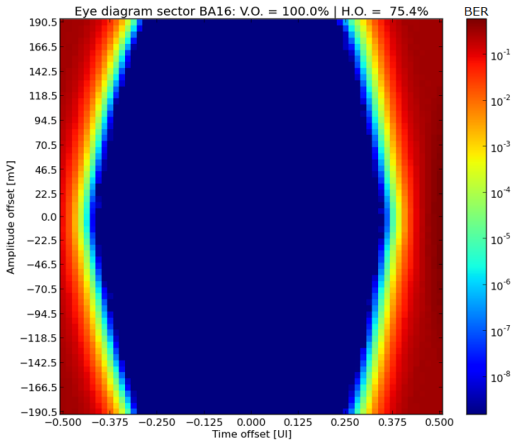
According to the recipe described in [5], all the software was developed and ported to the GitLab Continuous Integration scheme. The TDAQ run control applications, which run directly on the SoC were tested in the laboratory, and they were partially integrated in the Run Control online software for booting, configuring, and running the MUCTPI in the experiment.

5 Commissioning

Since the end of August 2021, the MUCTPI version 1 has been installed in the ATLAS counting room, and all the 208 connections with RPC and TGC have been established, see Figure 4a. The MUCTPI was successfully configured for running in the ATLAS TDAQ framework, and all the

fiber mapping was validated. Using the In-System IBERT core, nondestructive eye diagrams were recording during normal operation, which confirm the results achieved in the integration tests (Figure 4b).

(4a) Fully populated MUCTPI rack in the ATLAS counting room.



(4b) Eye diagram recorded during the normal operation of an RPC to MUCTPI link in the experiment.

Figure 4. Commissioning of the MUCTPI in the ATLAS experiment.

6 Summary and Outlook

The new MUCTPI hardware was validated and tested. It is fully functional and was installed in the ATLAS underground counting room. It is based on almost final hardware; final hardware will be produced in order to provide a sufficient number of spares. All the external interfaces with the subsystems were successfully validated during the integration tests. The trigger and the readout firmware have been validated. The software framework has been tested and verified, and has been partially integrated into the TDAQ control system: it is possible to configure the MUCTPI, and more control and monitoring features are currently being developed. The MUCTPI is getting ready for data taking in Run 3.

References

[1] ATLAS Collaboration, *The ATLAS Experiment at the CERN Large Hadron Collider*, *JINST* **3** (2008) pg. S08003–S08003.

[2] A. J. Armbruster et al., *The ATLAS Muon to Central Trigger Processor Interface Upgrade for the Run 3 of the LHC*, *2017 IEEE NSS/MIC* (2017) pg. 1-5.

[3] S. Haas et al., *The ATLAS Level-1 Muon to Central Trigger Processor Interface*, *Proceedings TWEPP-07* (2007).

[4] G. Anders et al., *Hardware and firmware developments for the upgrade of the ATLAS Level-1 Central Trigger Processor*", *JINST* **214** (2019) pg. 01034

[5] R. Spiwoks et al., *CentOS Linux for the ATLAS MUCTPI Upgrade*, *IEEE Transactions on Nuclear Science* **PP** (2021) pg. 1-1.