

CONTROL SYSTEM OF UPGRADED HIGH VOLTAGE FOR ATLAS TILE CALORIMETER

F. Martins^{1,*}, F. Cuim¹, G. Evans^{1,2}, R. Fernandez¹, L. Gurriana¹, A. Gomes^{1,2}, J. Soares Augusto^{2,3}

¹ Laboratory of Instrumentation and Experimental Particle Physics (LIP), Lisbon, Portugal

² Faculdade de Ciências da Universidade de Lisboa, Lisbon, Portugal

³ Inesc-ID, Lisbon, Portugal

Abstract

The preparation of the upgrade of the ATLAS electronics for the High Luminosity LHC is in full swing. The Tile Calorimeter is preparing the upgrade of its readout electronics and power distribution systems. One of such systems is the High Voltage (HV) regulation and distribution system. The new system is based on HVRemote boards mounted in crates located at the counting room. The HV will be delivered to the on-detector electronics using 100 m long cables. The crates will be equipped with a system-on-chip that will be responsible for the control and monitoring of the HV boards. The control of the HVRemote and its dedicated HVSupply boards is done by means of a serial peripheral interface bus. A SCADA component is under development to communicate with and supervise the crates and boards, and to integrate the HV system in the control system of the detector. The control system will be able to send notifications to the operators when the monitored values are out of range, archive the monitored data and if required, perform automated actions.

INTRODUCTION

Located in the central region of the ATLAS detector [1], the Tile Calorimeter (TileCal) [2] is composed of iron plates interpolated with plastic scintillating tiles that work as active material. The light resulting from the interaction of the particles with the plastic tiles is guided by wavelength shifting optical fibers to the photomultiplier tubes (PMT). The signal generated by the PMT is then processed by the on-detector and off-detector data acquisition electronics. TileCal uses approximately 10^4 PMTs divided over the 256 modules that compose the four TileCal operational barrels (EBA, EBC, LBA and LBC). The operation of TileCal requires a high voltage system able to regulate and monitor the HV set to each individual PMT with a precision within 0.5 V rms. For the High Luminosity Large Hadron Collider (HL-LHC) a new high voltage system is under development [3, 4] for TileCal, along with other hardware upgrades [5, 6]. It will consist of HV source boards, regulation and monitoring boards housed in crates located in the off-detector area, with the HV being delivered to each PMT by 100 m long cables. With the regulation boards located off-detector, they are not required to be radiation hard and they have also the advantage of easier

access for repairs which can be executed during data-taking periods.

The Detector Control System (DCS) of TileCal is responsible for the supervision and control of the TileCal electronics and infrastructure, continuously monitoring temperatures, voltages and currents [7].

HIGH VOLTAGE BOARDS

HVSupply

The HVSupply board is responsible for providing the direct current (DC) HV and the three low DC voltage levels, (12 V, -12 V, 3.3 V) required by the HVRemote board to operate. The HV will be supplied by two commercial DC/DC converters (Hamamatsu C12446-12) with a combined maximum output current of 20 mA and adjustable voltages up to -1000 V. The supervision will include the monitoring of the supplied voltages and respective current consumption as well as the readings of on-board temperature probes and on-chip temperature. The digital control and monitoring is achieved by using a dedicated Serial Peripheral Interface (SPI) bus. An analog switch was also implemented in the board which will allow the HV DC/DC converters to be switched off when a hardware interlock signal is removed. The interlock signal can either be interrupted by the TileCal DCS or by the Detector Safety System (DSS).

HVRemote

The HVRemote board is composed of 48 HV channels for regulating and monitoring the individual channels voltages in the range from -500 V to -950 V. Enabling or disabling the output of the HV channel is available by software in groups of 4 channels. However it is possible to disable the output of any of the HV channels by hardware (by means of a jumper) allowing, for example, to isolate it from a short circuit in the long cable or in the HVBus board (located on-detector). Temperature probes are available to monitor the board temperature and assess the cooling conditions. Each of the boards will have a unique serial number allowing the crate controller and the Supervisory Control and Data Acquisition (SCADA) control system to identify each individual HVRemote board. The communication between the on-board circuits and the crate control is done via a dedicated SPI bus. Figure 1 shows a simplified diagram of the HVRemote board control.

* Corresponding author fmartins@lip.pt

† Copyright 2021 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license.

Content from this work may be used under the terms of the CC BY 3.0 licence (© 2022). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI

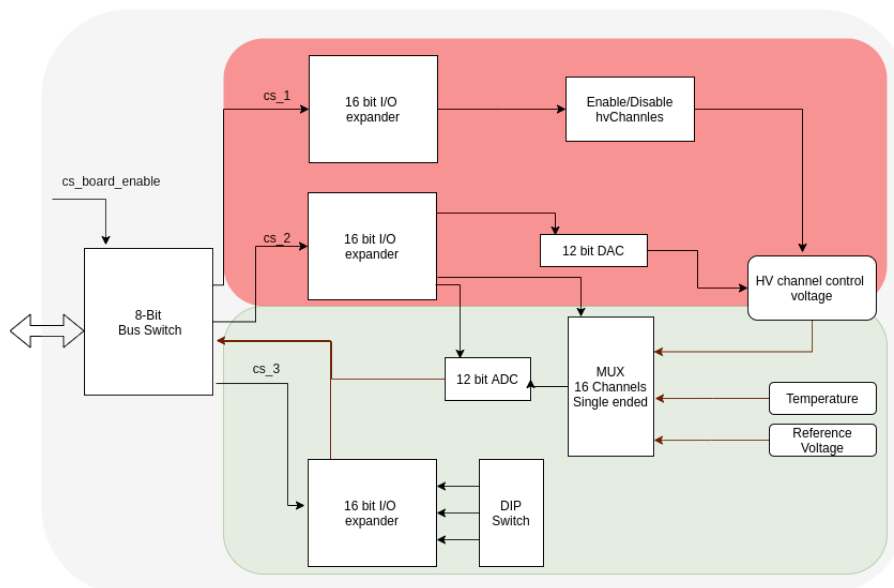


Figure 1: Simplified block diagram of the HVRemote control. The area of the diagram with the pink background represents the control of the HV and the one with the green background represents the monitoring path. The enabling of the Switch allows a specific board to receive the SPI commands from the controller.

HV Bus Board

The HV-bus boards root the HV delivered by the 100 m long cable to the designated PMT. Each board is equipped for 12 PMTs and 3 (in EBA/EBC) and 4 (in LBA/LBC) boards are needed per TileCal module. The HVbus is the only element of the HV distribution and regulation system which is located on-detector but since it does not have active elements (only resistors) there is no specific radiation requirement.

CRATE CONTROL

The control of the first HVRemote prototype was based in the Tibbo board and it was mounted directly on the HVRemote board [3]. Taking this approach, the final system would require the availability of more than 500 ethernet sockets and respective network cables, which would be a challenge due to space restrictions on the racks at the electronics rooms. At the end it would also be a complex system to maintain since a large number of Internet Protocol (IP) addresses would had to be kept and correctly mapped inside of DCS. To avoid dependencies on such constrains as well as to make the maintenance of the HV system easier and at the same time allowing the upgrade of the controller board if required, it was chosen to have a single controller installed on the crate. In this new design, the controller will be used to control both the HVRemote and the HVSupply, each with its dedicated SPI bus. Thus it was decided to use a System-on-chip (SoC) for the final crate control.

Interface Board

The interface board, that will be connected in the crates back-plane will hold a ZYBO board [8] and two port expanders. The ZYBO board is equipped with a Zynq-7000

SoC featuring a dual-core ARM processor and a Field Programmable Gate Array (FPGA) logic from Xilinx. The board is equipped with an EEPROM programmed with an unique Media Access Control (MAC) address, a built-in RJ45 connector for ethernet, Pmod connectors, among other features. The General Purpose Input and Output (GPIO) and SPI signals were assigned using Vivado and can be accessed at the assigned Pmod ports/pins. The boot of system was created with the PetaLinux tool integrating the design developed with Vivado. Relative to the Linux distributions, we are currently testing with CentOS 7 and Ubuntu. The root filesystem (rootfs) and boot are executed from the local Secure Digital (SD) card. There are two port expanders located on the interface board that will be used to select one board at a time, the boards on each SPI bus (each bus will be operated independently from the other). For this matter, a set of GPIO signals will be used to enable the assigned bus port expander, instead of the standard SPI chip select.

Software

The software running on the SoC (or in the Raspberry Pi used in the tests) operates as SPI controller [9]. The actual software for the board control has been written in Python and it has been used a Raspberry Pi 4 to develop it. Libraries implementing the required SPI instructions have been prepared to operate the control chips within each board. For example, setting I/O pins from the port expanders with a specific configuration. The communication between the DCS and the controller is (currently) a simple home-made protocol over TCP/IP allowing the commands or queries to be sent from the DCS to the controller and replies flow in the opposite direction, see Fig. 2. When the server is started it initiates the SPI bus and creates a socket which listens and

waits for commands or queries. At the restart of the server after a crash or un-programmed reboot of the SPI controller, the server does not initialize the boards, avoiding this way losing the previous configurations. From the DCS side, there are two types of requests; automatic queries (usually readings) which are updated regularly, and the commands which are initiated by the user and have priority over the automatic queries. Queries and commands handling are implemented in the software using a "to-do" list, where a process takes the command/query from the top of the list and sends it to the server to be handled. When the handling of the query or command is complete, the process takes the next item from the list and the process repeats itself. When the list is empty, the software updates the list with the group of automatic queries.

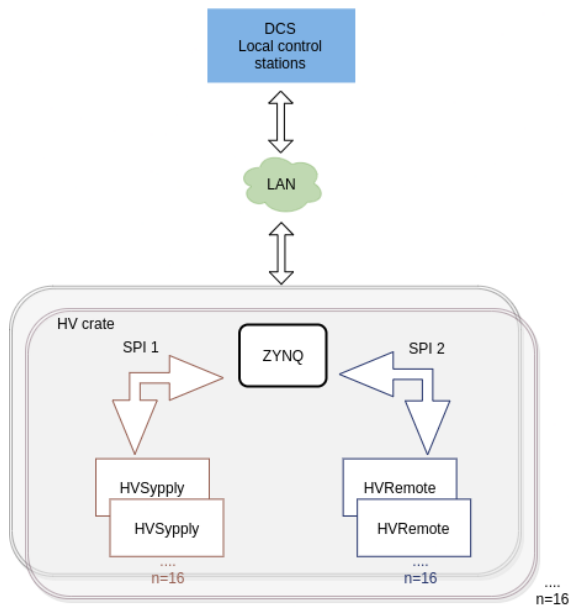


Figure 2: Architecture of the new HV system control tree.

INTEGRATION WITH TILECAL DCS

The slow control system of TileCal is based on the SCADA *WinCC OA* [10] and uses a set of software packages that ease the coherent integration of the hardware and its respective control component into the DCS. TileCal DCS is a distributed system comprising (currently) six individual SCADA systems, occupying two layers of the ATLAS DCS back-end hierarchy (see Fig. 3) taking different roles depending on the layer and type. The local control stations are the systems responsible for handling the hardware systems such as low voltages and high voltage [7].

The SCADA component for the HV Crates is being developed and under initial tests. Data point structures that represent the crate and respective boards were prepared, containing temperature probes, voltages and calibration values. The data arriving from the HVSypply and HVRemote are decoded and mapped to the respective data point element. It was also prepared a set of basic Graphical User Interfaces (GUI) which display the data located in the data points ele-

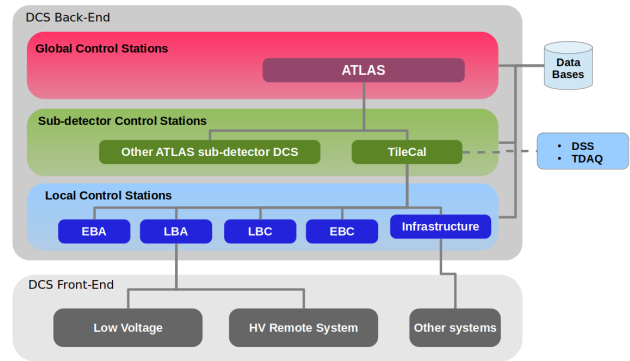


Figure 3: TileCal DCS hierarchy. Image adapted from [7].

ments and execute commands such as switching on/off HV channels (see Fig. 4), board resets (initialization), among others.

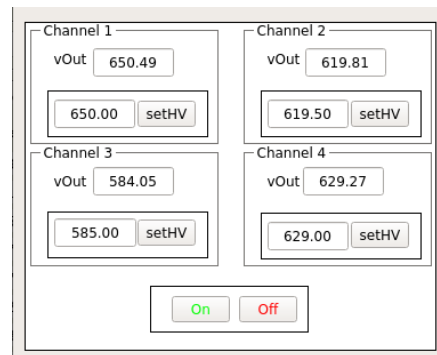


Figure 4: DCS test user interface. The measured HV is shown in the display "vOut" for a group of four channels. It shows the HV for each of the channels. It is also possible to enable or disable the HV for all four channels.

The archiving of the monitored data to the Oracle database is performed according to a set of rules or conditions (smoothing). The smoothing reduces the amount of data stored without losing important data, therefore making the archiving more efficient. For the HVRemote Channels, notifications are available in the form of alerts, which are triggered when the offset between the requested HV and the monitored HV is higher than 4 V (the value can be adjusted channel by channel). Notifications to experts such as emails or a short message service can also be configured, for example in the case of HVSypply failure. Actions can be triggered by alarms conditions as well, for example, in the case of high board temperature, the DCS should power down the HVSypply and HVRemote as a preventive measure.

Figure 5 shows the monitored HV by DCS from source 1 of an HVSypply board, without smoothing.

CONCLUSIONS AND FUTURE WORK

A new control is being prepared for the HV remote system which will consist on control software running on the crates and supervision software which is part of the TileCal DCS. As for the next steps the crate control software will be ported

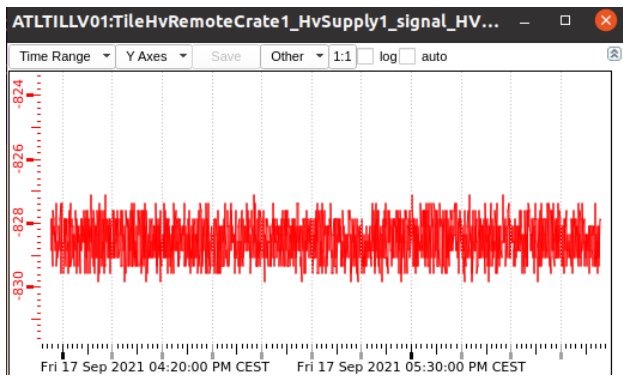


Figure 5: Plot of the output voltage (without smoothing) of one HV source located at the HVSupply during a test beam period with realistic data taking conditions.

to the ZYNQ controller and fully tested with the interface board and the other components of the system.

ACKNOWLEDGEMENTS

This work is funded in part by the "Fundação para a Ciência e a Tecnologia", Portugal, under the project "Upgrade da Experiência ATLAS", CERN/FIS-PAR/0033/2019.

REFERENCES

- [1] ATLAS Collaboration, "The ATLAS Experiment at the CERN Large Hadron Collider", *J. Instrum.*, vol. 3, p. S08003, 2008. doi:10.1088/1748-0221/3/08/S08003
- [2] ATLAS TileCal Collaboration, "Tile Calorimeter Technical Design Report", ATLAS Internal Note, CERN/LHCC/96-42, 1996. <https://cds.cern.ch/record/331062>

- [3] F. Martins, G.G. Evans, A. Gomes, L. Gurriana, A. Maio, C. Rato, J.M. Sabino, L. Seabra, and J.A. Soares Augusto, "Control System for Atlas Tilecal HVremote Boards", in *Proc. ICALEPCS2017*, Barcelona, Spain, Oct. 2017. doi:10.18429/JACoW-ICALEPCS2017-THPHA069
- [4] A. Da Silva Gomes, J.A. Soares, F. Cuim, G. Evans, R. Fernandez, L. Gurriana, and F. Martins, "Upgrade of the ATLAS Tile Calorimeter High Voltage System", in *Proc. of Topical Workshop on Electronics for Particle Physics — PoS(TWEPP2019)*, vol. 370, p. 062, 2020. doi:10.22323/1.370.0062
- [5] ATLAS Collaboration, "Technical Design Report for the Phase-II Upgrade of the ATLAS Tile Calorimeter", Sep 2017. <https://cds.cern.ch/record/2285583>
- [6] E.V. Santurio, "Upgrade of Tile Calorimeter of the ATLAS Detector for the High Luminosity LHC", *J. Phys. Conf. Ser.*, vol. 928, p. 12024, 2017. doi:10.1088/1742-6596/928/1/012024
- [7] F. Martins, "The ATLAS Tile calorimeter DCS for run 2," *IEEE Nuclear Science Symposium, Medical Imaging Conference and Room-Temperature Semiconductor Detector Workshop (NSS/MIC/RTSD)*, pp. 1-5, 2016. doi:10.1109/NSSMIC.2016.8069837
- [8] Diligent Zybo: <https://diligent.com/reference/programmable-logic/zybo/start>
- [9] Open Source Hardware Association: A Resolution to Re-define SPI Signal Names, <https://www.oshwa.org/a-resolution-to-redefine-spi-signal-names/>
- [10] Siemens SIMATIC SCADA Systems: <https://new.siemens.com/global/en/products/automation/industry-software/automation-software/scada.html>