RD53B Wafer Testing for the ATLAS ITk Pixel Detector

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Abstract. RD53 is the research and development group at CERN responsible for developing and producing the next generation of readout chips for the ATLAS and CMS pixel detectors at the HL-LHC. It has recently developed the ITkPix-V1/RD53B full-scale 65 nm hybrid pixel-readout chip. ITkPix-V1 consists of more than one billion transistors with high memory triplication ratio to cope with the high particle density at the heart of ATLAS. The chips will be located as close as possible to the interaction point to optimize impact parameter resolution. The ITkPix-V1 chip features a 5-Gbit connection, with special data compression to deal with high hit intensities. In addition, a low-power, low-noise analog front-end is used, to ensure high readout speeds and low detection thresholds. A failure of chips in ATLAS is problematic. Therefore, thorough testing before and during production is necessary. For this purpose, the Bonn ATLAS group has developed BDAQ53, a fast and versatile simulation, and testing environment, that allows for small- and large-scale testing for ITkPix-V1 and its successor chips. This conference note will give an overview of the testing environment while focusing on large-scale wafer testing to evaluate ITkPix-V1's suitability for its deployment at the HL-LHC.

1. Introduction

ITkPix-V1/RD53B (ITkPix-V1) is part of a two-silicon-die combination, a so-called hybrid module (Figure 1). This configuration allows the top die to be specialized in charge collection induced by a large density of traversing ionizing particles, while the other die offers enough space for a chip to house analog amplification circuits and digitization electronics in each pixel. In addition, the bottom chip (ITkPix-V1) offers a standardized interface to forward data from the pixel matrix to the detector readout (Figure 1). Each ITkPix-V1 offers a total of 0.15 megapixels distributed over an area of 2 cm x 2 cm. The ATLAS inner tracker (ITk) will consist of 33 092 ITkPix − V1 with an active area of approximately 12.7 m^2 distributed over five barrels and in total 14 disks in forward and backward direction [6]. Surrounded by an additional four silicon strip detector barrels [3].

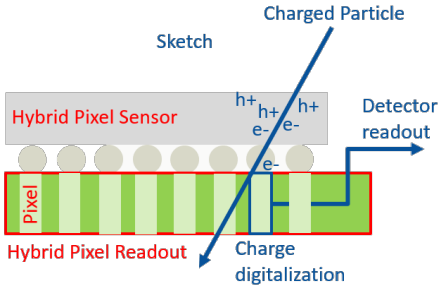


Figure 1: Charge produced by an ionizing particle is guided through a bump bond to the ITkPix-V1 readout chip.

2. ITkPix-V1

ITkPix-V1 has four critical points, which need to be tested on every single chip before further assembly. All conducted tests are designed to cover as much of the following four test domains as possible:

(i) **Analog Chip Bottom**: The analog chip bottom houses band gaps, power regulators, and sensors to supply the digital logic with correct frequencies and voltages necessary for operation.

(ii) **Digital Chip Bottom**: The digital chip bottom aggregates all the digital information from the pixel matrix and is responsible for chip control. It encodes and decodes data sent from and to the chip while handling logical functions.

(iii) **Analog Pixel**: The analog pixel electronics are responsible for charge integration, amplification, and measurement. This circuit is part of each pixel and therefore needs to be tested more than 150 thousand times per chip.

(iv) **Digital Pixel**: The digital pixel electronics are responsible for digitizing the analog signal, generated by the analog pixel electronics. This circuit is also part of each pixel and therefore needs to be tested more than 150 thousand times per chip.

3. ITkPix-V1 - Wafer Probing Setup

In chip production, it is common practice to test each chip on a wafer level. A perfect wafer yields up to 132 ITkPix-V1. To determine the yield, Bonn has developed the following wafer probing setup with the BDAQ53 test system at its heart. Figure 2 shows a simplified version

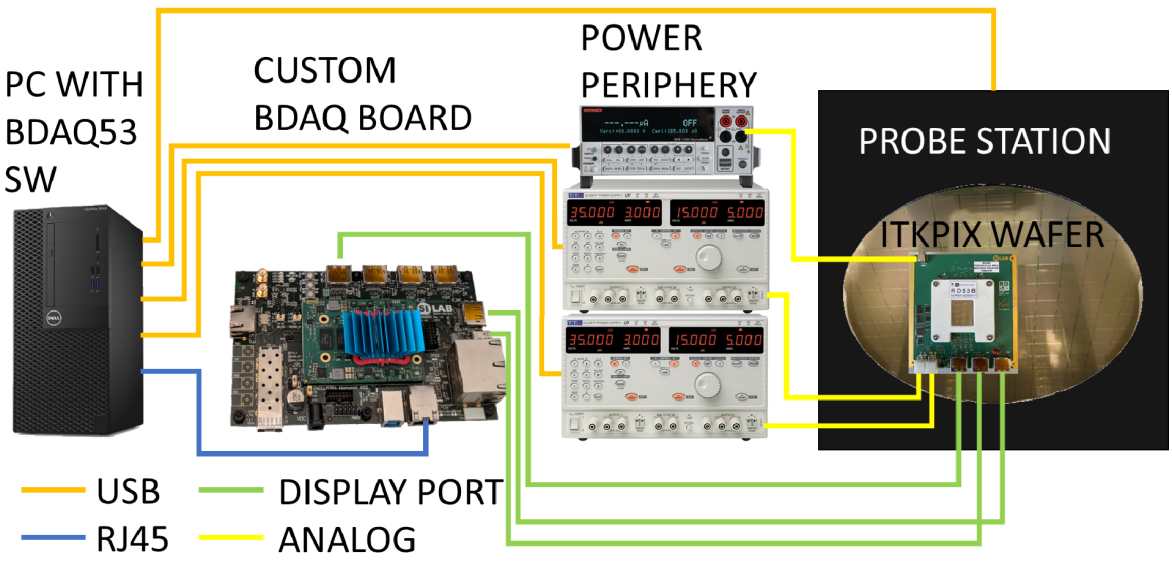


Figure 2: ITkPix-V1 wafer probing setup.

of its components. From left to right we find the data acquisition PC, which controls powering, measurement, and probe station periphery via a serial interface. Controls like this allow the setup to automatically power off and on while informing the probe station to disconnect from the chip and continue to the next one. Connection to the chip is established with a probe card, featuring approximately 200 tungsten probes, temporarily touching the wire bond pads on the chip. Chip functionality is then tested using BDAQ53, which connects to the probe card via display port, to forward the received chip data to the data acquisition PC via RJ45.

4. Test Routines

The functionality tests are oriented along the domains introduced in Section 2. Figure 3 shows the order of tests with a color reference for the given domain. The order of tests is picked after hierarchy. A chip, that is drawing too much current, e.g. due to an analog power rail shortage, is also not passing all following tests. Therefore if one test fails by a certain margin the other tests are skipped and the chip is marked red (non-functioning).

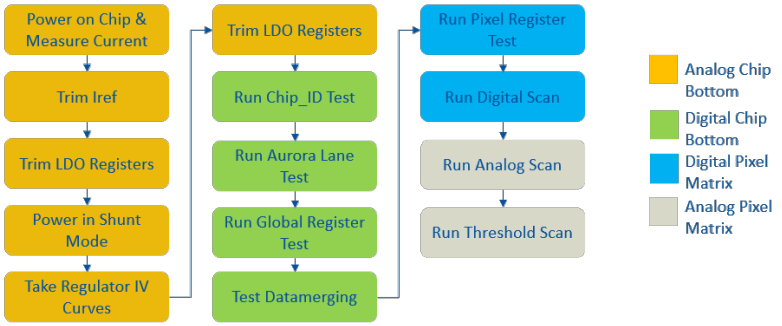
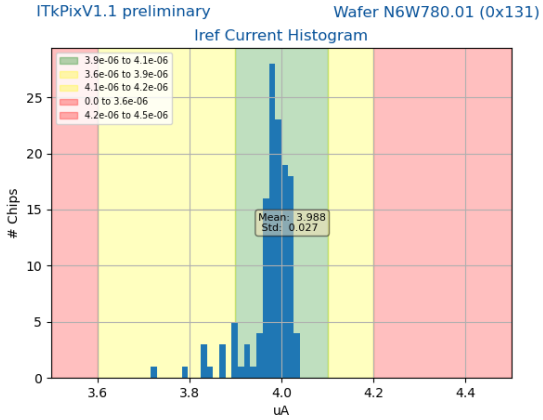


Figure 3: Order of tests conducted per chip.

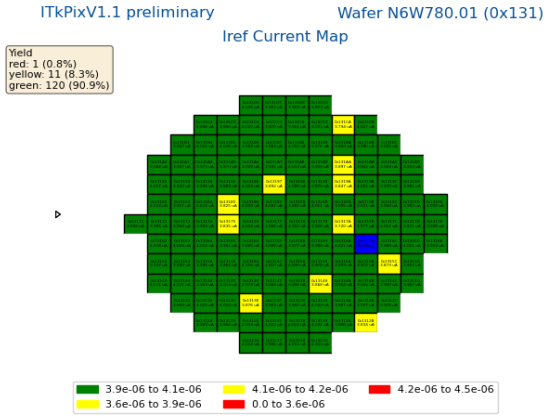
The yellow domain incorporates essentially four procedures, the first is powering and checking for short circuits by measuring the current after powering. The second is trimming the on-chip reference current to 4 µA "Trim Iref" and the third step is trimming the on-chip digital and analog power rails to 1.2 V. If this is successful, a second powering mode of ITkPix-V1, the so-called shunt mode is tested. This mode will be used to power multiple ITkPix-V1 in series. For this operating mode, it is crucial, that each chip draws the same current, regardless of the chips operating state. The excess current is burnt in the so-called shunt regulators, which mimic an ohmic resistance. [7] The linearity of this ohmic resistance is tested in the step "Take Regulator IV Curves" (See Figure 3. Afterward, again the supply power rails are trimmed to 1.2 V. In this powering mode, the chip's digital chip bottom domain is subject to further tests. The general idea behind these tests is that a predefined command pattern is sent to the chip. If the chip responds with the expected correct pattern it passes the test. Test patterns include testing if the chip is reachable under the correct chip ID if the chip can respond on all four data TX lanes "Aurora Lane Test" if all the bits in the chip's configuration registers work, and if a feature called data merging works. Data merging is a feature, where one chip X can forward its data output to another dedicated data merging input of chip Y. Chip Y then integrates the data of chip X in its own data output stream. For this purpose, BDAQ53 simulates a full ITkPix-V1 aurora core in its FPGA and can forward data to the device under test (chip Y) input. While BDAQ monitors the chip Y output for the data sent by the simulated chip X. The blue domain tests if the pixel configuration registers work and the digital hit processing of each pixel work. The grey domain focuses on the analog pixel matrix domain. Here the analog front end is checked and whether each of the pixels responds in a certain threshold region.

5. Test Routine Output

Each of the test routines mentioned in Section 4 produces a wafer level histogram and map, to get a statistical overview of chip variations over the same wafer and assign the measured properties of each chip to the correct position for future wafer processing. Figure 4a shows an exemplary histogram of the trimmed reference current (Iref). The plot is divided into three performance domains: red, yellow, and green. Chips, that have values in the red area, fail the test and the prober-software will immediately go to the next chip. Yellow chips are chips, which do not quite fulfill the requirements for the detector but can most likely still be used for bench testing and development. Green chips are chips, which pass the criterion for being assembled into modules. Based on this histogram the colors in Figure 4b, are assigned and form a so-called



(a) Reference current histogram after trimming for 132 chips



(b) Wafer map for reference current after trimming

wafer map. Blue chips in the wafer map are not represented in the histogram, due to an earlier measurement error. (e.g. shorted power rails). In the next step, wafers will be cut and green, yellow and red chips will be sorted and assigned for their future use.

6. Summary

This paper summarizes the automated process of wafer probing the ATLAS ITk Pixel chip RD53B/ITkPix-V1. During production, more than 80000 ITkPix-V1 will be tested in at least three sites in Glasgow, Paris, and Bonn, which should each probe three wafers per week. These sites will all run with hardware and software as presented in this paper, ensuring the readiness of 33092 ITkPix-V1 for the integration into the ATLAS Inner Tracker for the HL-LHC upgrade at CERN in 2025.

References

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