RD3 note 45
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ELECTRONIC NOISE in LAr CALORIMETRY

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1- Introduction

Due to the trade-off between pileup noise and electronics noise, the latter remains a limitation, even for the next high luminosity colliders. The electronic noise is widely known to depend on a large number of parameters, such as the detector capacitance, the shaping time, the power allocated or the technology used for the preamplifiers. Some of these parameters are frozen by the detector design (capacitance) or by external contraints (shaping time or power dissipated). The others (circuit architecture, technology or transistors size) are left free for optimization. We shall detail here the part that can be optimized, give numeric figures on the noise performance that can be aimed at and compare with experimental results recently achieved.

2- Signal

Before talking of the noise, we should always talk of the signal. The current waveform created by an ionizing particle in a sampling calorimeter has already been described many times. Here is a reminder of the most important formulas. The numeric figures given are issued from the RD3 ("accordion") electro magnetic calorimeter.

a) Charge deposited in the ionization medium

An incoming particle yields part of its energy in the absorber and part in ionizing the liquid noble gas, creating a 'straw' of electron-ion pairs that drift under the effect of the external electric field applied to the gap. The total charge Q deposited in the liquid is related to the sampling fraction η_s (ratio of the dE/dx of the different materials) multiplied by the suppression factor for electromagnetic showers[1] a_M.

$$Q = \frac{E}{W_i} \eta_s a_M \qquad (1)$$

in which
Q is the charge deposited (Q electrons and Q ions)
E is the particle energy
W_i = 26 eV is the energy necessary to create one pair electron-ion in the argon[2]

1 - The suppression factor corrects for the fact that em showers give less signal than the corresponding energy in MIPs : part of the shower is "suppressed". This is due to the low energy photons at the end of the shower process that lose their energy preferentially in the absorber through photoelectric effect (scaling as Z^5). [1].

2 - In fact the number of charges collectable depends on the electric field as a fraction of electrons and ions can recombine at low field. This is usually specified in terms of yield of free electrons for 100eV : $G_{fi}(E)$. The dependence of G_{fi} with the field is often described with Onsager's model [2]. For liquid argon, G_{fi} quickly saturates to its maximum value equal to $100/W_i$.

$\eta_s = 0.23$ is the sampling fraction[3]. It is directly proportionnal to the gap thickness.
$a_M = 0.7$ is calculated on the basis of Montecarlo simulations.
For RD3 geometry these figures lead to :

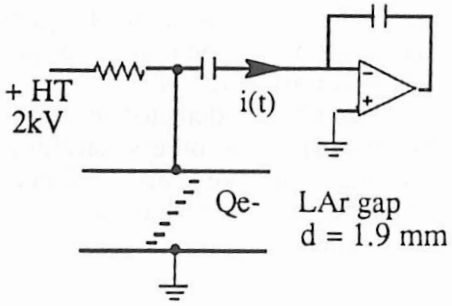
$$Q \approx 6000\ e^-/MeV \qquad (2)$$

b) Current waveform

The motion of the electrons[4] under an applied electric field creates a current in the external circuit. The current waveform is given by [3]:

$$i(t) = \frac{Q}{t_{dr}}\left(1 - \frac{t}{t_{dr}}\right) \qquad (3)$$

in which
Q is the number of ionisation electrons, given by eq (1)
$t_{dr} = d/v_e$ is the drift time that would take one electron to cross the gap.
For RD3 : d = 1.9 mm, t_{dr} = 400 ns



The initial current is then, using eq (2) :

$$I_0 = \frac{Q}{t_{dr}} = 2.5nA / MeV \qquad (4)$$

Integrating (4) during the drift time gives the collected charge, equal to

Q/2 = 3000 e-/MeV.

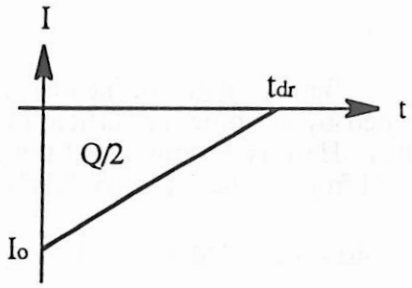


Fig. 1 : Current induced by an ionising particle in LAr

3 - Electronic chain

The front end electronic chain usually consists of a preamplifier and of a shaping amplifier. The preamplifier gives some gain so that the noise from the following stages and the pick-up on the output cables can be negligible.

[3] - Details of the calculation for RD3 geometry :

Materiel	dE/dx	*	density	*	thickness	=	total
1.8 mm lead	1.13		11.35		1.8		23.08
0.2 mm SS	1.48		7.80		0.2		2.31
0.6 mm Plastic	1.51		1.40		0.6		1.90
3.8 mm Argon	1.51		1.40		3.8		8.03
Total							35.32

Leads to a liquid argon fraction : ηs = 8.03/35.32 = 0.228

[4] - The ions also induce a current of the same sign (opposite charge and opposite drift direction), but their mobility being less than 1000 times that of the electrons, this current can be neglected. The space charge they constitute could, in principle, modify the electric field, but the effect has been shown negligible [4].

a) Charge preamps and Current preamps

Charge preamps have been used for decades on detectors where the total ionization charge was to be read. Their advantages are :
- to deliver an output voltage directly proportionnal to the input charge
- to be a very low noise configuration[5]
- to exhibit a low, real, input impedance that minimizes crosstalk problems.

However, for LHC-SSC experiments, the huge dynamic range (whereas only 10% of the charge is read cf § 3-c) combined with second stage noise emergence, seriously jeopardizes their use [5].

There now seems to be a consensus on the use of *current* preamps[6] for the electro-magnetic calorimeter as they overcome these problems [5, 6]. But they present some counterparts :
- the input impedance is partly inductive, which can lead to oscillations as the detector is capacitive. This requires a very large bandwidth or ellaborate circuit design.
- the feedback resistor introduces parallel noise, which can be significant at long shaping or small detector capacitance.

However, these little difficulties are negligable, compared to the benefits on the dynamic range, the second stage noise and the shaper realisation[7]. It should be pointed out that the series noise optimization carried out in §4 applies to both type of preamps (see note 10).

At this stage, any slackening of the signal before the fast shaping results in amplitude loss at the output, known as ballistic deficit. Thus inductive leads to the preamps introduce a time constant that decreases the signal amplitude resulting in an increased noise referred to the input. This is the reason why preamplifiers are usually located as close as possible to the detector, directly working at LAr temperature.

b) Zero transistor (0T)

The '0T' denomination comes from the absence of electronics inside the cryostat. The preamplifiers, working at room temperature, are connected to the detector through a simple cable. It has been shown [7] that at fast shaping, the transmission line should not be considered as a simple capacitance adding to C_d and spoiling the noise, but as its complex impedance. Under some restrictive conditions (met by the accordion), this impedance is not worse than the impedance formed by C_d which determines the series noise, and the noise is relatively independent of the line length[8]. Besides, the preamplifier location at room temperature allows the use of bipolar transistors which display superior noise performance at fast shaping. The weakness of this configuration is an increased sensitivity to pick-up noise, but which can be overcome by care given not to violate the good Faraday cage formed by the cryostat. This configuration has been tested in the frame of RD3 with comparable noise performance than the preamps described in § 5-c [8].

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[5] By careful design, the noise can be reduced to the series noise of the input transistor (cf §4) which is unseparable from the amplification process.

[6] - A current preamp (PAI) is similar to a charge preamp (PAC) but with a resistor R_f in the feedback instead of a capacitor C_f. The transfer function of an ideal PAI is simply $V_{out}/I_{in} = R_f$ (instead of $1/sC_f$). A real one includes at least one pole to take into account its finite rise time and often is after more complicated as the second order poles are seldom negligible.

[7] A current preamp with 1.5kΩ feedback resistor is linear on the whole dynamic range for LHC and as it is non integrating, some gain can be added at the shaper level before the first differentiation, so that the shaper noise requirement becomes less stringent [5].

[8] The cable length comes into consideration only due to skin effect as it will slacken the signal and generate thermal noise. These effects are considerably diminished when the cable is located at low temperature, as the skin effect resistance goes down by a factor of 3 at liquid argon temperature.

c) Pulse shaping

The shaper is used to optimize the signal to noise ratio, including the "physics" noise[9] due to the pileup of low energy events. For high luminosity hadron colliders, this pileup noise will necessitate the use of a very fast signal shaping such as represented on fig 2. To avoid baseline variation with the mean energy deposited, a bipolar waveform is necessary, so that the signal area is zero [9]. Practically, with a charge preamp[10], the shaper is a combination of 2 differentiations (high pass) and n integrations (low pass) often noted CR^2RC^n. It has been shown elesewhere [10] that the signal to noise ratio is very weakly dependent on the number of integrations, provided n>2. In that case, the electronic chain can be characterized by its response to a current impulse (δ response), and more precisely by the time between 5% and the peak noted $t_p(\delta)$.

When this peaking time is shorter than the drift time, only part of the input current contributes to the shaped output[11]; when it is much shorter than t_{dr}, the input current can be assimilated to a step and the amplitude is roughly[12] proportionnal to $t_p(\delta)$. Thus, the output signal is no longer sensitive to the *charge read* Q/2 but to the *initial current* I_0.

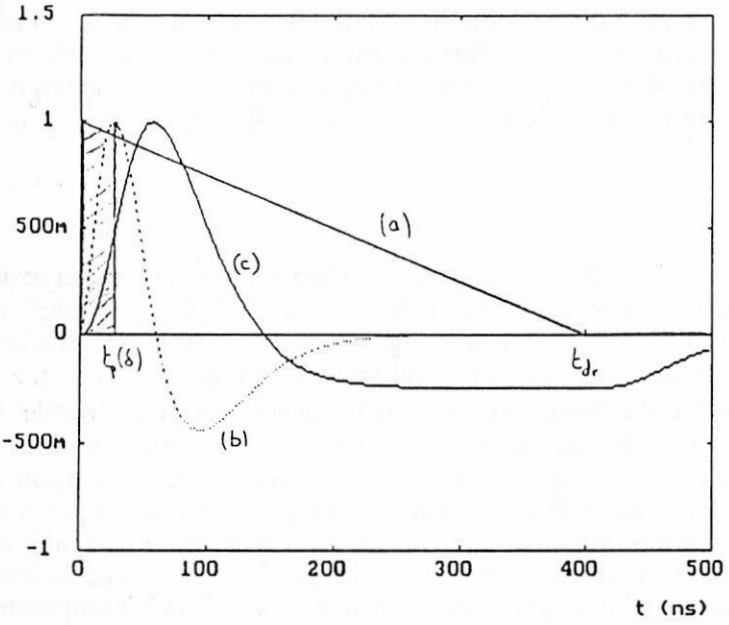

Fig. 2 : Signal shaping

a) Current waveform from the detector as given by eq (3).
b) Impulse response of the electronic chain (dashed) as anticipated for the barrel at maximum luminosity. It can be characterized by its peaking time $t_p(\delta)$
c) Response to the triangle = convolution of a) and b).
The hatched area represents the charge that contributes to the maximum amplitude of curve c) (see note 12).

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[9] - The enormous rate of uninteresting events that arise from hadronic collisions leads to consider them as a noise. They are mostly minimum bias events which present an energy spectrum exponentially decreasing, with a mean value of 350 MeV. The variance of the output voltage they induce is given by Campbell's theorem : $\sigma 2 = \iint n(E)E^2v^2_{out}dEdt$. As the variables are independent, the integrals can be separated in two terms : one from physics is $\sigma(E^2)$ and the other one from electronics is $\int v^2_{out}(t)dt$ known as *pileup integral*, is proportionnal to the shaper peaking time, thus the need for a fast shaping to minimize this noise contribution.

[10] - With a current preamp (PAI) which is a non integrating circuit, the shaper is unipolar as one less differentiation is needed. Besides, it can be shown that PAC + CR^2RC^n is equivalent to PAI + $CR\,RC^{(n+1)}$ as the global transfer functions are identical.

[11] - Analytical expressions for these signals in the time domain can be found in [10].

[12] - The charge Q_m that contributes to the output signal allows to define an 'effective integration time' : t_i as $Q_m=I_0t_i$ [9]. This effective integration time is analogous to the gate of a gated integrator. It is proportionnal to $t_p(\delta)$ although not very precisely (see Fig. 2). A better invariant is t_p(triangle) with $t_i=0.7*t_p$(triangle) [11].

4 - Electronic noise

The noise performance of the electronic chain is usually dominated by that of the preamplifier since the following stages contributions are referred to the input divided by the preamplifier gain. The widespread use of charge preamplifers has rendered the noise specification in terms of Equivalent Noise Charge (ENC) [12] very popular, so we shall give expressions stating ENC although they are not the most adapted to current sensitive electronics[13].

a) General expression

Any noisy electronic system can be represented by the same noiseless system and two noise generators on the input :
* a voltage one (e_n) in series with the input, hence the term of *series* noise
* a current one (i_n) in parallel with the input, known as *parallel* noise.

For a detector essentially capacitive, ENC is given by[14] [12] :

$$ENC^2 = e_n^2 \; C_t^2 \frac{I_a^2}{\tau} + i_n^2 \; I_b^2 \tau \qquad (5)$$

in which
* e_n is the spectral density (in V/√Hz) of the preamp series noise generator, the most fundamental as it is related to the amplification mechanism. It is related to the transconductance (g_m) of the preamp input transistor by $e_n^2 = 4kT \frac{\alpha}{g_m}$ where $\alpha \approx 0,7$ is the excess noise factor[15] and $4kT = 1.66\ 10^{-20}$ J at T = 300 K.

* C_t is the total capacitance at the preamp input, usually dominated by the detector capacitance C_d and the preamp input capacitance C_a.
* I_a is the series noise integral, related to the shaper architecture[16]. The use of the peaking time $t_p(\delta)$ instead of the shaper time constant τ renders $I_a / \sqrt{t_p(\delta)}$ fairly independent of the shaper design.
* i_n is the spectral density (in A/√Hz) of the parallel noise generator. It is usually due to the thermal noise of resistors on the input, such as feedback or calibration resistor : $i_n^2 = 4kT / R$. Benefit is obtained from the location of these resistors in the cold.
* I_b is the parallel noise integral also related to the shaper design. $I_b \sqrt{t_p(\delta)}$ is also roughly invariant (although a little less) than I_a to the shaper design.
* τ is the shaper time constant it is related to the peaking time $t_p(\delta)$.

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[13] - As the electronic chain is sensitive to the initial current (cf. § 3-c), the noise should be referred to the input in terms of Equivalent Noise Current (ENI) that can be easily converted in MeV with eq (3) : 100 nA rms -> 40 MeV.

[14] - A very similar formula holds for the noise in terms of equivalent noise current (ENI) :

$ENI = e_n C_t J_a \tau^{-3/2}$ (+) $i_n J_b \tau^{-1/2}$. With this formulation, there is no need to evaluate the effective integration time (cf. note 12) to know what fraction of the signal is read, and have the noise converted into energy resolution.

[15] - This excess noise factor should not to be mistaken with the 'excess noise' denomination for 1/f noise.

$\alpha = 1/2$ for bipolar transistors, $\alpha \approx 2/3$ for JFETS, $.7 < \alpha < 2$ for MOS transistors. It should be emphasized that α varies widely with the temperature, as for example JFETS exhibit more noise at T = 77K than at room temperature, although g_m is higher. This effect is usually attributed to hot electrons effects.

[16] - $I_a^2 = 1/2\pi h^2 \int_{max} H(j\omega\tau)^2 / (\omega\tau)^2 \, d\omega$ where $H(j\omega)$ is the filter transfer function. See ref. [10, 11, 12] for details.

Usually, the series noise is dominant and we saw that it is related to the g_m of the input trans. Therefore, rewriting (5) and neglecting the parallel noise term, leads to :

$$ENC = A \frac{C_d + C_a}{\sqrt{g_m}} \qquad (6)$$

in which $A^2 = 4kT\alpha\, I^2_a/\tau$

C_d is usually fixed by the detector design, although (6) shows that for a same signal, C_d should be minimized to reduce the electronic noise. The only parameters left free to the designer are g_m and C_a, and we shall examine how they can be optimized.

b) Optimum noise and "capacitive matching"

It is widely known that the preamp noise can be minimized by matching the preamp input capacitance to C_d or to $1/3C_d$! We shall detail here how to choose between these two 'optima' and how they can be conciliated. We suppose in this paragraph that the input device is a FET (Si, MOS or GaAs)[17], and try to determine the optimal transistor. A very good model of these transistors in the saturation region[18] is the square law approximation, relating the drain current to the input voltage [13] :

$$I_d = I_{dss}\left(1 - \frac{V_{gs}}{V_p}\right)^2 \qquad (7)$$

in which
I_d is the current flowing in the channel
I_{dss} is the saturation current obtained with $V_{gs} = 0$. This is the maximum current that can flow in the channel before turning into conduction the gate-source junction[19]
V_{gs} is the input voltage as the source is usually grounded to minimize the noise
V_p is the pinch-off voltage, for which the channel is cut off. ($V_p < 0$ for N channels)

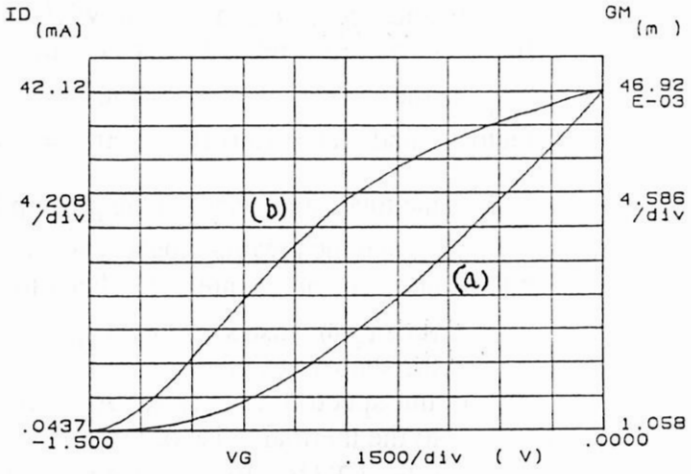

Fig. 3 : (a) I_d vs V_{gs} and (b) g_m vs V_{gs} for a Ga As MESFET 3SK166 (cf. § 5-b)

[17] - It is interesting to notice that the transistor size optimization done in the following applies to FETs, but not to bipolar transistors. In effect, their transconductance does not depend on their size, but only on the collector current : $g_m = qI_c/kT$. Therefore, for a given current, the series noise is minimized with the smallest transistor. In reality, limits on the current density set a minimum size for the transistor so that it does not melt ! A bigger transistor also allows to reduce the base spreading resistor $R_{bb'}$, the thermal noise of which is seldom negligible. When there is no constraint on power dissipation, the minimum noise is achieved by choosing a collector current such as the series noise and the parallel noise due to the base current be equal.

[18] - The region where the channel is pinched so that I_d varies marginally with V_{ds}. This is determined by $V_{ds} > V_p$ which sets a minimum voltage for the static polarization of the transistors.

[19] - In fact, the transistor could be operated at $I_d > I_{dss}$ provided the current flowing into the gate I_g remains reasonnable. This is determined by the amount of parallel noise $i^2_n = 2qI_g$ that can be accepted. This leakage current is very temperature dependent as $I_g = I_{gss} \exp(qV_{gs}/kT)$.

From which we can extract the transconductance g_m.

$$g_m = \frac{\partial I_d}{\partial V_{GS}} = -\frac{2I_{dss}}{V_p}\left(1 - \frac{V_{GS}}{V_p}\right) = -\frac{2}{V_p}\sqrt{I_{dss}\, I_d} \qquad (8)$$

g_m is maximum for $I_d=I_{dss}$, and this value is often noted $g_{m0} = -2I_{dss}/V_p$

(8) is valid only for $I_d \leq I_{dss}$. On the other side, at small currents the transconductance does not always scale with $\sqrt{I_d}$ as the ratio g_m/I_d cannot be better than q/kT.
The breakpoint is given by :

$$I_d = \left(\frac{2kT}{qV_p}\right)^2 I_{dss} \qquad (9)$$

Below this point, g_m scales linearly with I_d and the device is very similar to a bipolar transistor, which presents the best g_m/I_d ratio obtainable (q/kT). (See note 17).

In these expressions, most parameters are frozen by the technology used, and only the operating current (I_d) and the transistor width (W) can be varied.
V_p does not depend[20] on W
I_{dss} is directly proportionnal[21] to W.

$$I_{dss} = k_1 W \qquad (10)$$

and replacing (10) in (9) gives :

$$g_m = \sqrt{k_1' W I_d} \qquad \text{with } k_1' = \frac{4}{v_p^2} k_1 \qquad (11)$$

The amplifier input capacitance depends directly on the transistor size and very weakly on the operating current [22]

$$C_a = k_2 W \qquad (12)$$

At this moment, it can be noticed that the ratio g_{m0}/C_a does not depend on W or I_d but only on the technology. (This is however not the case for g_m/C_a that scales as $\sqrt{I_d}$ and $1/\sqrt{W}$). It is a factor of merit for the rapidity of the transistor : $F_t = \frac{g_{m0}}{2\pi C_a}$, but also for the noise as it can be seen from eq (6).

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[20] - V_p is relatively technology independent. It depends only on doping concentrations and on channel depth. It is not a very well stabilized quantity, usually specified within a factor of 2.

[21] - I_{dss} is proportionnal to the electron mobility and to the ratio W/L where L is the transistor length (a few microns) set by technological state of the art. As the capacitance is proportionnal to W*L, the speed (and the noise) of the technology benefits as L^2 of channel length improvements. However some parameters suffer with short channels such as 1/f noise, output conductance or excess noise factor. (See § 5-c).

[22] - The transistor capacitance is dominated by the gate-source junction capacitance, which varies with the gate voltage approximately as $C_{gs}=C_{gs0}/(1+V_{gs}/\phi_0)^{1/3}$. The gate voltage in turn varies with $\sqrt{I_d}$ cf eq (7).

Replacing (11) and (12) in (6) gives

$$ENC = A \frac{C_d + k_2 W}{\sqrt[4]{k'_1 W I_d}} \qquad (13)$$

For a given technology (k'_1 and k_2) we can optimize[23] this function of two variables W and I_d.

a) For a given transistor size, ENC scales as $I_d^{-1/4}$, and is then minimum when $I_d = I_{dss}$. Thus doubling the current decreases the noise by ≈ 20%.

b) For a given current I_d the optimum size is given by

$$\frac{\partial ENC}{\partial W} = 0 <=> k_2 W^{-1/4} - \frac{1}{4}(C_d + k_2 W) W^{-5/4} = 0$$

$$<=> W = C_d/3k_2 \qquad (14)$$

(14) can be rewritten as : $\underline{C_a = C_d/3}$ (independent of technology) (14 bis)

This optimization is valid for a drain current I_d smaller than the saturation current I_{dss} corresponding to the optimum transistor size $W=C_d/3k_2$. It is represented in fig 4 as the line (AB). At point B, the current cannot be further increased to reduce the noise, without also increasing the transistor size, as I_d would be greater than I_{dss}. The noise still goes down, but following the frontier $I_d = I_{dss}$ (line BC). It reaches an absolute minimum when $C_a = C_d$ (point C), known as 'capacitive matching', which can be attained only with small detectors or at high dissipation[24]. For liquid argon detectors, this is usually not the case, and the optimum matching is at $C_a = C_d/3$. It can be difficult to reach with transistors presenting a high g_m/C ratio (such as AsGa), as it requires very large transistors (cf § 5).

To summarize, the optimum matching is :

$C_a = 1/3\ C_d$ when the power is constrained
$C_a = C_d$ and $I_d = I_{dss}$ where there is no limit on power.

[23] - The optimization with respect to W is usually treated by paralleling n 'elementary' transistors. Although valid, this formulation is sometimes misleading on the concept of elementary transistor, on its operating point and whether this paralleling increases or not the total current. We prefer here to *separate completely the variables* : size and current.

[24] - Or with a transformer

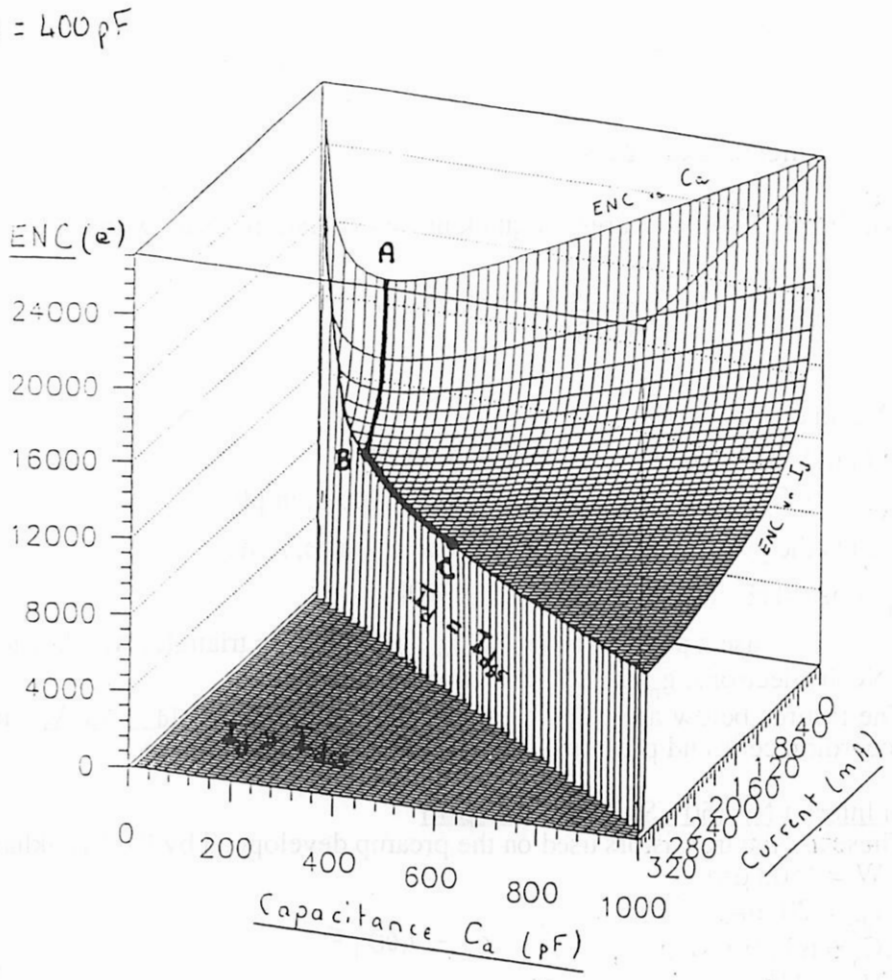

Fig. 4 : Noise versus drain current I_d and transistor capacitance C_a, as given by eq. (13). We take C_d = 400 pF and the Si JFET from § 5-a. The transistor size (proportionnal to C_a) determines the maximum allowable current I_{dss}, with eq (10). This delimits the frontier beyond which the noise is not defined.
We can see that at fixed current, the noise is minimal at $C_a = C_d/3$ and decreases as $I_d^{-1/4}$. When I_d reaches the frontier I_{dss} the noise still decreases by raising C_a (line BC). The absolute minimum is at $C_a = C_d$ (point C) and $I_d = I_{dss}$.

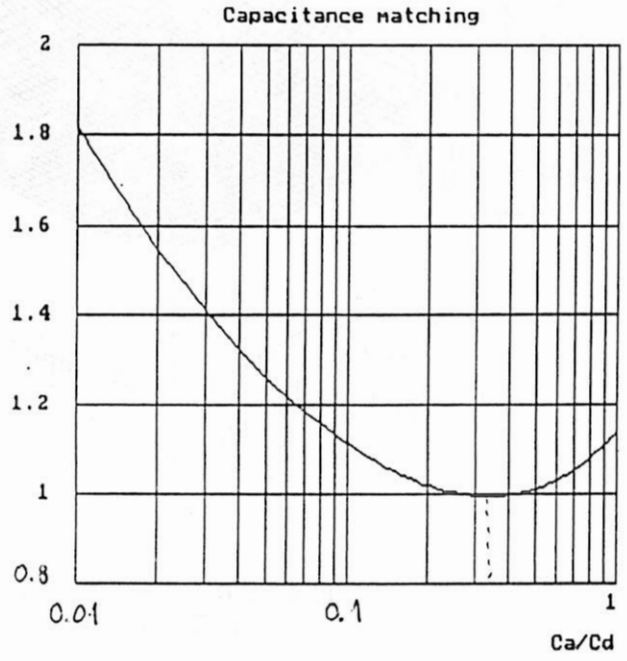

Fig. 5

Detail of the mismatch penalty at fixed current.

5 - Numeric examples

We first give some figures for quick noise evaluation (exact with a CR^2RC^2 filter) [10, 11]

$$ENC = 213 \frac{e_n C_t}{\sqrt{t_p(\delta)}} \oplus 168 i_n \sqrt{t_p(\delta)} \qquad (15)$$

ENC in electrons rms

e_n in nV/√Hz (60 Ω -> 1nV/√Hz at 300K)

$C_t = C_a + C_d$ is the total capacitance on the input, in pF

$t_p(\delta)$ is the peaking time (5-100%) to an impulse, in ns

i_n in pA/√Hz (1kΩ -> 4pA/√Hz at 300k)

We use a peaking time $t_p(\delta) = 20ns$ (40ns to triangle) which leads to A = 4.7 in (6) with ENC in electrons, g_m in A/V and capacitors in pF.
The figures below are calculated for $C_d = 400pF$ and $I_d = 5mA$, which correspond to the accordion cells and preamplifiers used in RD3 tests (cf.§ 5-c).

a) Interfet NJ 450 (Si JFET L=5 µm)
These are the transistors used on the preamp developped by the Brookhaven group for RD3.

$W = 4500\ \mu m$
$I_{dss} = 20$ mA
$C_a = 60$ pF
$V_p = -1V$
from which we deduce
$F_t = 100$ MHz
$k_1 = 4.44$ A/m
$k'_1 = 17.8\ AV^{-2}m^{-1}$
$k_2 = 13.3$ nF/m

i) one transistor
$W = 4500\ \mu m$
$C_a = 60$ pF
$g_m = 20$ mA/V
ENC = 4.7*415/√.02
= 15280 e-

ii) optimum matching
$C_a = 133$ pF
$W = 10\ 000\ \mu m$
$I_{dss} = 44$ mA
$g_m = 29.7$ mA/V
ENC = 14540 e-

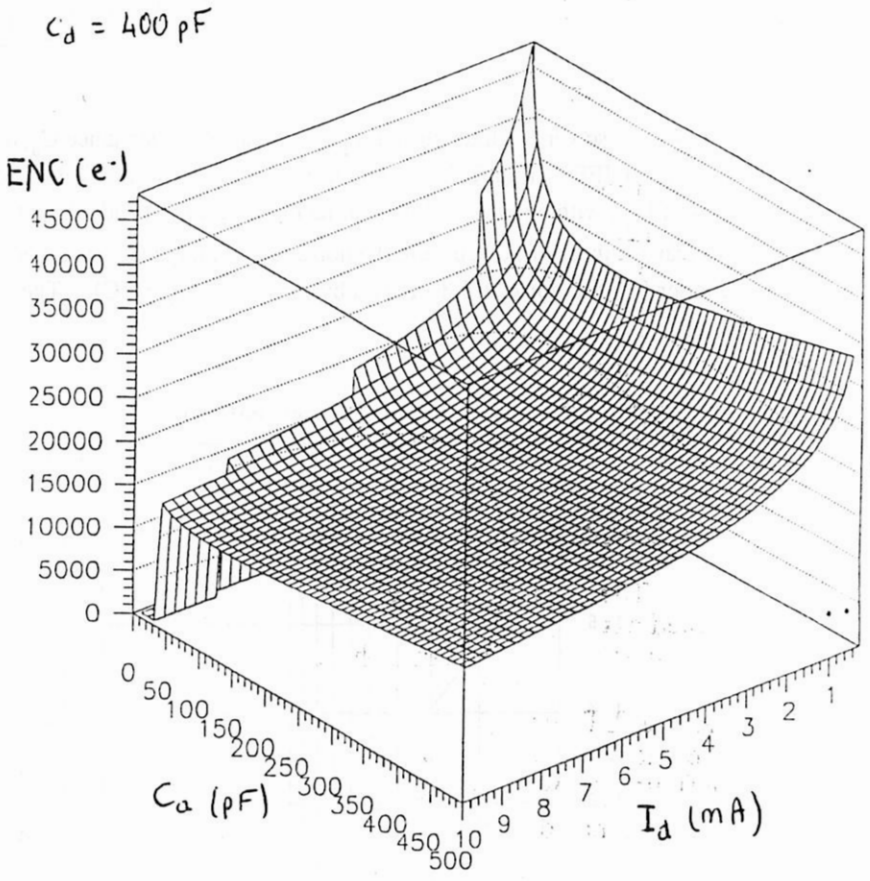

Fig. 6 : ENC (e-) vs Id (mA) and Ca (pF) of the Si JFET NJ5450

b) SONY 3SK166 (GaAs MESFET L=1.2 µm)

These transistors equipped the preamplifiers described in § 5-b,developped by the Milano group They are very similar to the Triquint process proposed by the Munich group.

W = 1200 µm
I_{dss} = 30 mA
C_a = 1.5 pF
V_p = -1.5 V
from which we deduce
F_t = 4.2 GHz
k_1 = 25 A/m
k'_1 = 44.4 $AV^{-2}m^{-1}$
k_2 = 1.25 nF/m

i) one transistor
W = 1200 µm
C_a = 1.5 pF
g_m = 16.3 mA/V
ENC = 14778 e-

ii) ten transistors in parallel
W=12000 µm =>
C_a = 15 pF
g_m = 53.3 mA/V
ENC = 9000 e-

iii) optimum matching
C_a = 133 pF =>
W = 106400 µm !
I_{dss} = 1.78 A !
g_m = 126m A/V
ENC = 7070 e-

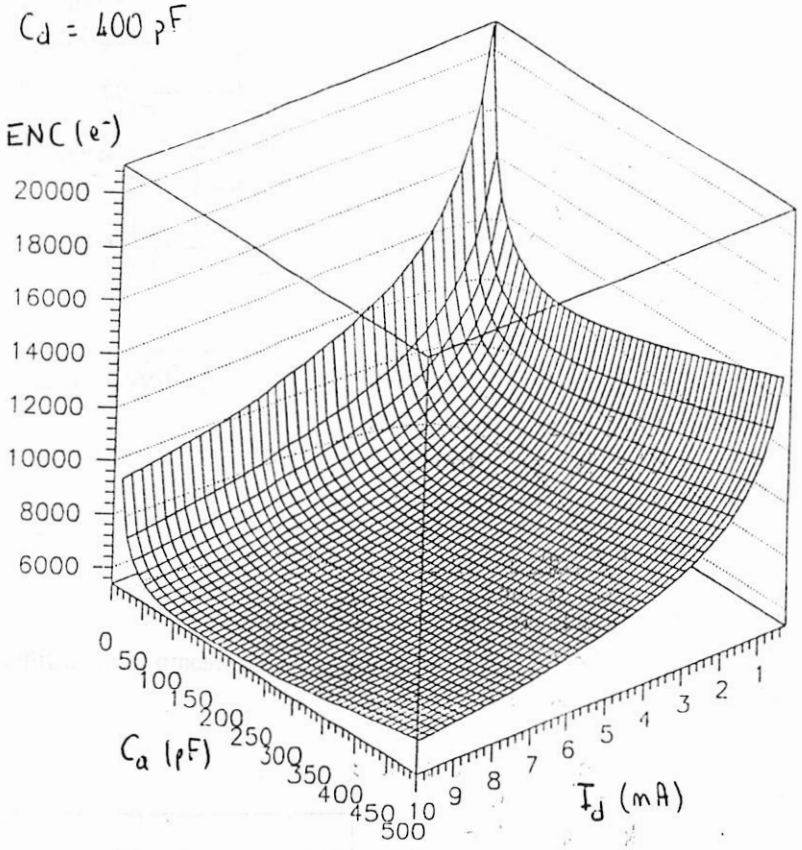

Fig. 7 : ENC (e-) vs Id (mA) and Ca (pF) of the GaAs MESFET 3SK166

From these figures, it can be seen that for the *same power*, a GaAs preamplifier should exhibit *half* the noise of its Si counterpart. Both technologies have been tested in the frame of RD3 collaboration but showed comparable noise levels with respect to the test beam energy [8].

c - Experimental results

The promising noise improvements that could be achieved with GaAs have long been pointed out by the Milano group, and charge preamps have been realized for RD3 tests.
Two types of charge preamps have been tested :

i) A Si JFET one developped by Brookhaven based on the transistors described in § 5-a. The schematic is given in fig 8. Q1 is the input transistor followed by the classical cascode configuration with Q2; Q3-R3 from a current source and Q4 the output follower, to drive a 50Ω terminated line. A level shifter (R9-R10) at the output allows the DC polarization in closed loop. The feedback network is F_c = 33 pF and F_r = 10 kΩ - Q5 acts as a protecting diode against discharges.

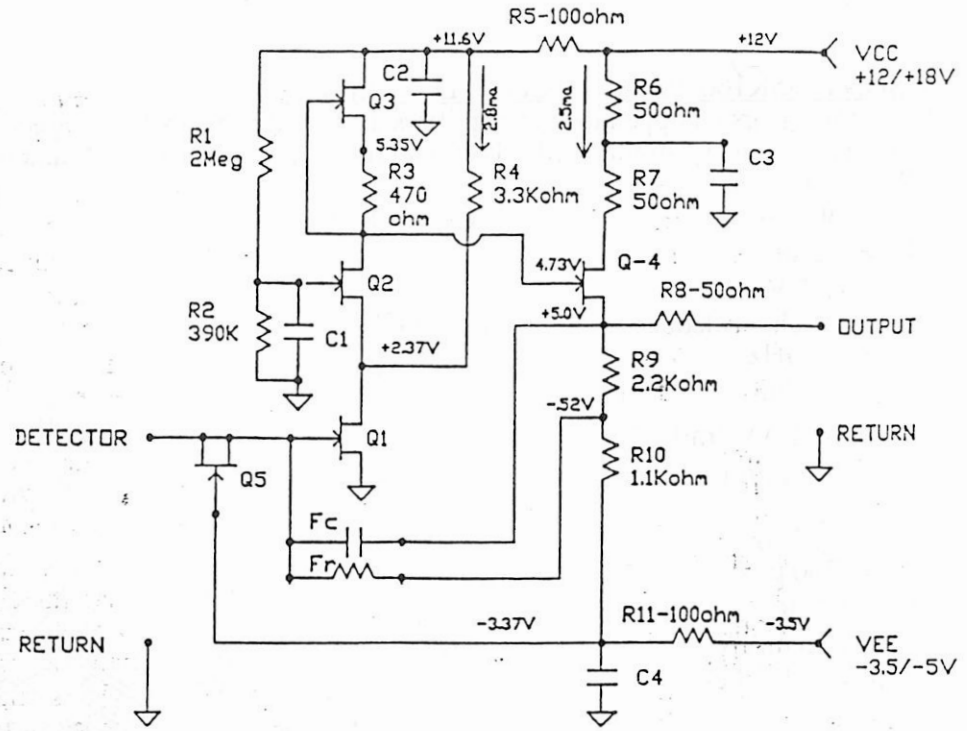

Fig. 8 : Charge preamp using Si JFETs developped by BNL [14]

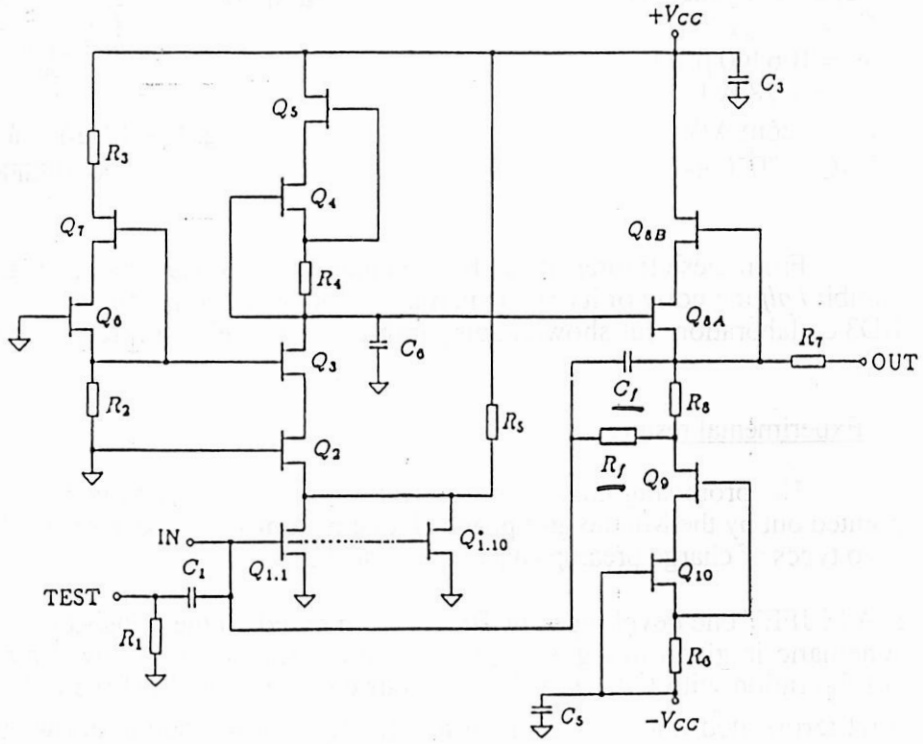

Fig. 9 : Charge preamp using GaAs MESFETs developped by Milano [15]

ii) a GaAs one, developped by Milano, using the transistors described in § 5-b. It follows the same global architecture (fig 9), although a little more complicated as each transistor is replaced by a bootstrapped pair (as Q4-Q5) to raise the output impedance, very low on GaAs. This is necessary to make an efficient charge preamp, as a high open loop gain G is necessary to transfer the charges from the detector into the feedback capacitor ($GC_f >> C_d$). The transistors are dual gate devices, in which the gates were shorted together to reduce the 1/f noise by a factor of 100 and raise the output impedance [14]. This results in a longer transistor (see note 21) which penalizes both g_m and C_a by a factor close to 2 , leading to a noise penalty from the figures given in § 5-b. 10 transistors were mounted in parallel to improve the capacitive matching - 100 would have been necessary ! - which gives a noise penalty of 40%.

Measurements on workbench at room temperatures, using the same variable filter, are plotted in fig 10. They display similar ENC values, not far from the calculation, especially for the Si preamp in which the series noise is really the dominant contributor. For GaAs, some $1/f^{\alpha}$ is visible at low frequency, but the series noise is dominant at fast shaping and similar to Si. At room temperature, the Silicium preamp is much slower than the GaAs, which renders the comparisons not so straightforward. This is even worse when measuring the noise in MeV (or in ENI) as the different preamp rise times lead to different effective integration time (see note 12). At liquid Argon temperature (87 K) the noise from GaAs improves by 30% (and more for 1/f), while the speed is merely affected. The silicon is much faster, comparable with GaAs, but the noise is similar to the levels at room temperature.

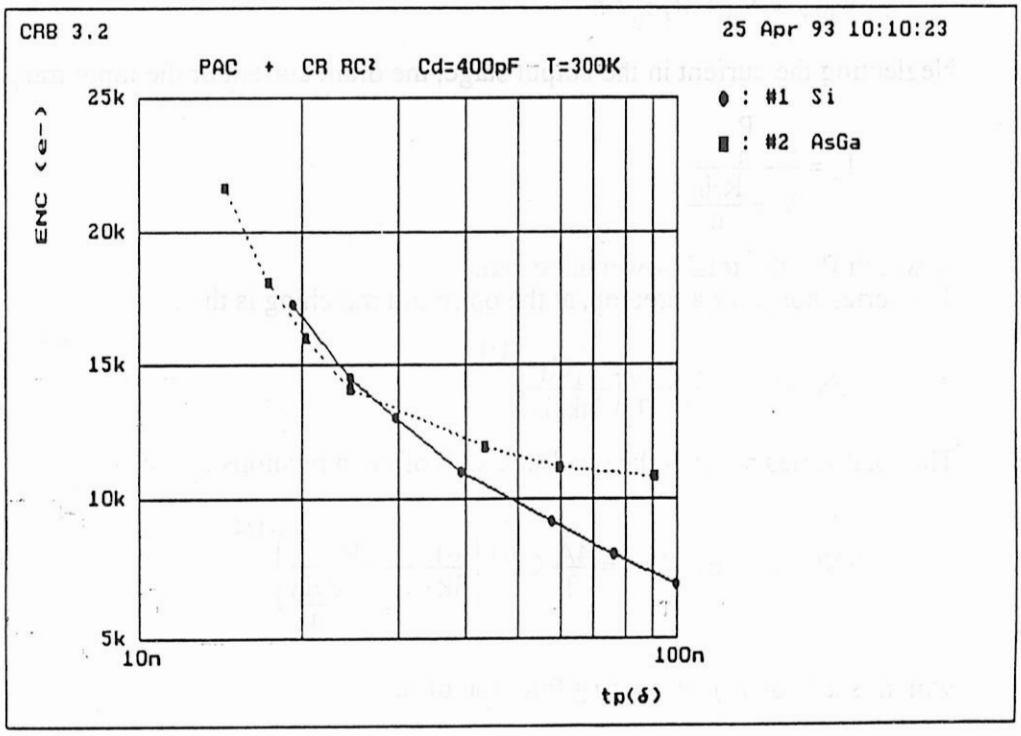

Fig. 10 : ENC vs $t_p(\delta)$ measurements of Si and AsGa charge preamps with C_d = 400 pF. At room temperature, the series noise are similar.

The noise penalty due to capacitive mismatch, unavoidable with discrete GaAs transistors (not at all designed for particle physics!) should be overcome by the realisation of a GaAs preamplifier in VLSI, presently under development by both the Milano and Munich groups (using Triquint Foundry). The noise deterioration due to short channels (such as 1/f noise, excess noise factor or output conductance) should be evaluated in details, especially in the current preamp configuration which is less demanding on open loop gain[25]. Besides, irradiation tests carried out at CERN showed higher noise deteriorations on GaAs preamps than on Silicium [16]. This might be worse with short channel transistors, as the 1/f noise is already higher and deserves further investigation.

6 - Detector segmentation

Subdivising the detector in depth looks attractive to reduce the noise at constant dissipation per tower ($d\eta\ d\phi\ dz$) [6]. In effect, the smaller dynamic range allows to reduce the supply voltage and operate preamplifiers at a relatively higher current.

We shall assume in the following calculation that a detector tower is subdivided in depth in n elements, each having a capacitance C_d/n. We make the simplist (and not very realistic) assumption that the total signal I_0 extends uniformly in depth, leading to I_0/n in each little preamp. The preamp output voltage, in the case of a current preamp, is simply :

$$V_s = R_f I_0 / n.$$

This determines the preamps supply voltage, taking into account a fix voltage for static polarization V_p : (see note 18)

$$V_{alim} = V_p + R_f I_0 / n \qquad (16)$$

Neglecting the current in the output stage, the drain current of the input transistor is :

$$I_d = \frac{\frac{P}{n}}{V + \frac{R_f I_0}{n}} \qquad (17)$$

in which P is the total power allocated.
The series noise for a preamp, at the optimum matching is then :

$$ENCs(n) = \frac{4A}{3}\frac{C_d}{n}\left(\frac{k_1' C_d}{3nk_2 I_d}\right)^{-1/4} \qquad (18)$$

The total series noise is the quadratic sum of the n preamps :

$$ENC = \sqrt{n}\ ENC(n) = \frac{4A}{3} C_d^{3/4}\left(\frac{k_1'}{3k_2}\frac{P}{V_p + \frac{R_f I_0}{n}}\right)^{-1/4} \qquad (19)$$

which is a (slowly) decreasing function of n.

---

[25] - The open loop gain G determines the low frequency input resistance $R_{in} = R_f/G$ which must be low enough so that the rise time $R_{in} C_{in}$ be small. However, the inductive part of the input impedance, set by the dominant pole, is usually the main limitation to the rise time.

A few figures to illustrate this point :

Subdivision	1	10
Detector capacitance	400 pF	40 pF
Power per preamp	60 mW	6 mW
Signal max per preamp	1.5 TeV	150 GeV
Signal input current I_o	4 mA	0.4 mA
Feedback value	1.5 kΩ	3 kΩ
Preamp output swing	6 V	1.2 V
Polarization voltage	5 V	5 V
Technology[26]	AsGa	AsGa
Current in input transistor[27]	5 mA	0.6 mA
Transistor width	106 mm	10.6 mm
Preamp capacitance	133 pF	13.3 pF
Transconductance	126 mA/V	16.8 mA/V
Series noise per preamp	7070 e-	1930 e-
Total series noise	7070 e-	6110 e-
Parallel noise per preamp[28]	1370 e-	970 e-
Total parallel noise	1370 e-	3060 e-
TOTAL NOISE	7200 e-	6830 e-

These figures show that the benefit on noise is very moderate, all the more since second stage noise will be more penalizing at small detector capacitance. Thus, concerning the electronic noise, detector subdivision seems rather irrelevant. The noise penalty of a larger detector capacitance (13) is therefore not significantly improved by detector segmentation.

7 - Conclusion

At limited power dissipation, the preamp series noise is minimal when the input capacitance is matched to one third of the detector capacitance.

GaAs transistors could in principle improve by a factor 2 or so the noise levels obtained so far by RD3. They will require specially designed transistors to achieve the precited capacitive matching, and the short channel effects should be carefully investigated including sensitivity to radiations.

Detector subdivision seems to have negligible effect on noise performance.

[26] - We use the parameters described in § 5-b.

[27] - $I_d = P/V_{alim}$; keeping O.3 mA for the output branch.

[28] - Noise due to the feedback resistor, which is at liquid argon temperature.

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