Global Trigger Technological Demonstrator for ATLAS Phase-II upgrade

Viacheslav Filimonov, Bruno Bauss, Volker Büscher, Ulrich Schäfer, Duc Bao Ta
on behalf of the ATLAS TDAQ Collaboration

Abstract—**ATLAS detector at the LHC will undergo a major Phase-II upgrade for the High Luminosity LHC. The upgrade affects all major ATLAS systems, including the Trigger and Data Acquisition systems.**

As part of the Level-0 Trigger System, the Global Trigger uses full-granularity calorimeter cells to perform algorithms, refines the trigger objects and applies topological requirements. The Global Trigger uses a Global Common Module as the building block of its design. To achieve a high input and output bandwidth and substantial processing power, the Global Common Module will host the most advanced FPGAs and optical modules.

In order to evaluate the new generation of optical modules and FPGAs running at high data rates (up to 28 Gb/s), a Global Trigger Technological Demonstrator board has been designed and tested.

The main hardware blocks of the board are the Xilinx Virtex Ultrascale+ 9P FPGA and a number of optical modules, including high-speed Finisar BOA and Samtec FireFly modules. Long-run link tests have been performed for the Finisar BOA and Samtec FireFly optical modules running at 25.65 and 27.58 Gb/s respectively. Successful results demonstrating a good performance of the optical modules when communicating with the FPGA have been obtained.

The paper provides a hardware overview and measurement results of the Technological Demonstrator.

Index Terms— **LHC, ATLAS, FPGA, Optical Modules**

I. INTRODUCTION

THE Global Trigger System is a part of the Phase-II upgrade of the ATLAS [1] Trigger and Data Acquisition (TDAQ) system [2]. The Global Trigger will replace the Phase-I Topological Processor [3] and extend its functions by using full-granularity calorimeter cells for refining the trigger objects calculated by the Level-0 Trigger System, performing offline-like algorithms, including iterative algorithms such as topoclustering, calculating event-level quantities and applying topological requirements (Fig. 1). The use of Higher Level Synthesis will be supported as well.
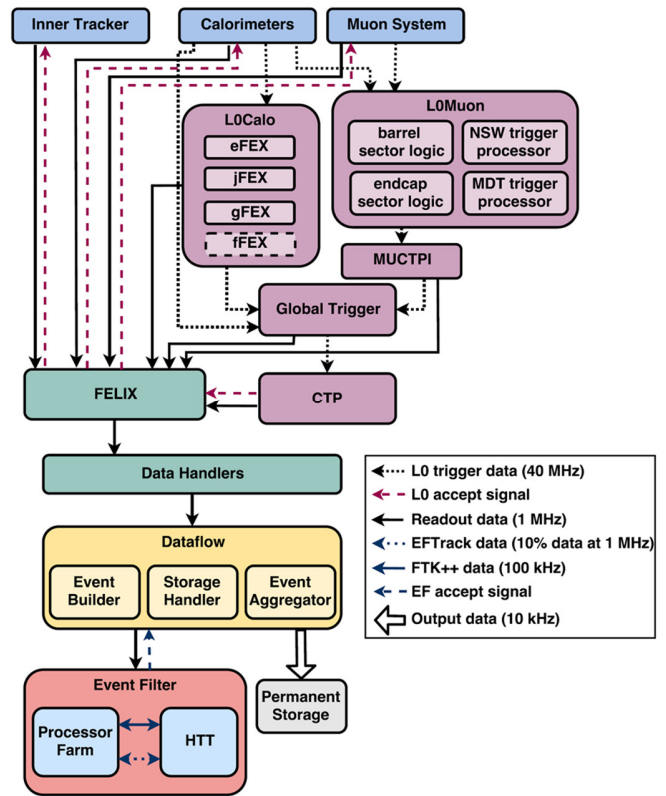
Fig. 1. TDAQ System after the Phase-II upgrade (baseline design) [2].

The Global Trigger is a time-multiplexed system, which concentrates data of full event into a single processor. The Global Trigger System is composed of three main layers: Multiplexing (MUX) layer, Global Event Processor (GEP) layer and Demultiplexing layer, which implements an interface to the Central Trigger Processor (CTP) (Fig. 2).
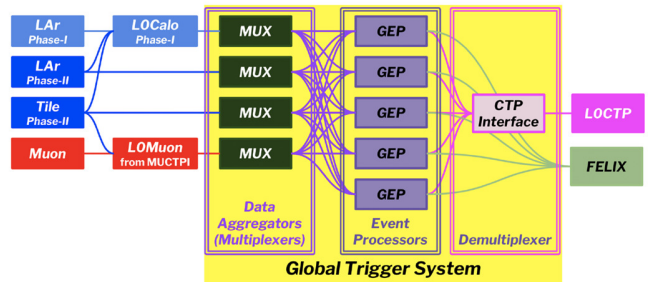

Fig. 2. Schematic view of the Global Trigger System [2].

The building block of the Global Trigger is the Global Common Module (GCM), which has to provide significant processing resources along with a high input and output bandwidth. This ATCA module is used in each layer of the Global Trigger System.

A block diagram for the GCM is shown in Fig. 3. The board hosts two large FPGAs (Xilinx Ultrascale+ VU13P [4]) with a sufficient number of multi-gigabit transceivers. A ZYNQ MPSoC is implemented for monitoring, control and readout functions. Random Access Memory (RAM) storage modules are used for long latency buffering of the input and output data. Each of the large FPGAs serves as a MUX or a GEP node, as shown in Fig. 2.
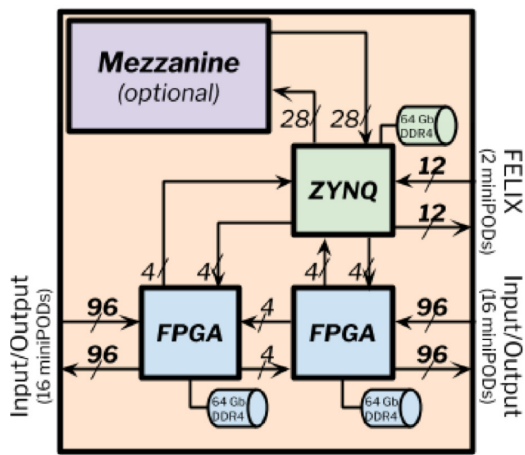

Fig. 3. GCM block diagram [2].

In order to provide a platform to evaluate various firmware blocks (MUX and GEP) of the Global Trigger System during the development of the GCM infrastructure and algorithm firmware, the Production Firmware Deployment Module (PFM) is used. This board represents a slice of the GCM, which includes a single processing unit (MUX or GEP), a control FPGA and a number of optical modules.

The PFM is designed in an ATCA form factor with the possibility of a standalone operation. The structure of the board can be seen in Fig. 4. The layout is well-matched to the ATCA airflow.

The main building blocks are the following: one MUX / GEP FPGA (Xilinx Ultrascale+ VU13P), up to eight Finisar BOA [5] modules for real-time data path, one Finisar BOA module for interface to Front-End Link eXchange (FELIX) system, one UltraZed [6] board with Zynq UltraScale+, one IPM Controller (IPMC), one FPGA power mezzanine and two DDR4 RAMs.

Such a configuration of the PFM allows testing and debugging algorithm and infrastructure firmware together with the corresponding software, thus minimizing the risk of firmware failures on the final system. In order to allow for early firmware development and evaluation, the PFM needs to be available well before the production GCM.

The design of the PFM is based on the R&D performed with the Technological Demonstrator, described below.
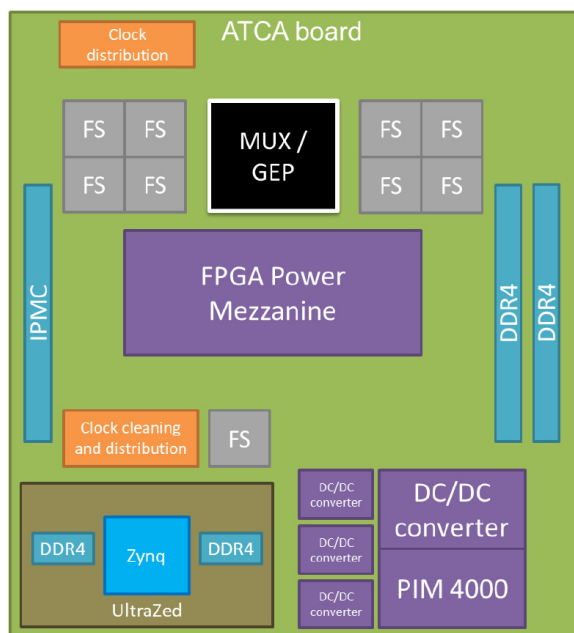

Fig. 4. PFM hardware structure.

Various link speeds, including high-speed links up to 28 Gb/s, should be supported on the GCM and the PFM. The high-speed link support is essential in order to cope with the transmission of high-granularity calorimeter data, which drives the bandwidth requirement for the upgraded TDAQ system. Since Avago MiniPOD [7] optical modules, widely used in the Phase-I Level-1 Trigger system, can only achieve data rates of 14 Gb/s, it is necessary to evaluate the new generation of optical modules running at high data rates (up to 28 Gb/s). The optical modules should be tested together with one of the most advanced FPGA supporting high-speed data transmission and having substantial processing power.

II. BOARD OVERVIEW

As part of the R&D for the Phase-II Global Trigger System, a Technological Demonstrator board has been designed with an FPGA and high-speed optical modules implemented on-board (Fig. 5). The board design is significantly closer to the final GCM and PFM designs in comparison with commercial evaluation boards and, therefore, can provide more reliable evaluation results.

The Demonstrator is designed in a custom ATCA form factor with a number of design blocks, which can be evaluated and reused for the GCM. The central part of the board is the Xilinx Virtex Ultrascale+ 9P FPGA [4], which is connected to two 28G 2x4-lane bidirectional Samtec FireFly [8] modules, one 28G 2x12-lane bidirectional Finisar BOA [5] module and six 14G 1x12-lane unidirectional MiniPODs (three receivers and three transmitters). The Demonstrator makes use of power and control mezzanines in order to provide the necessary voltages for the on-board components as well as to provide the essential control functionality. Dedicated clock distribution circuits are

implemented as well in order to provide reference clocks for the multi-gigabit transceivers of the FPGA. A slot for an IPMC module, a standard component in ATCA boards for hot-swap power management and sensor monitoring, is present on the board as well.
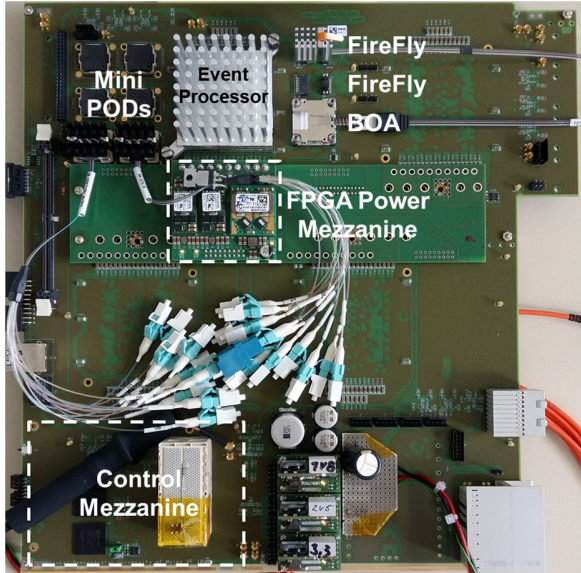

Fig. 5. Global Trigger Technological Demonstrator hardware overview.

The detailed block diagram in Fig. 6 shows the multi-gigabit transceiver connections of the FPGA on the Technological Demonstrator.
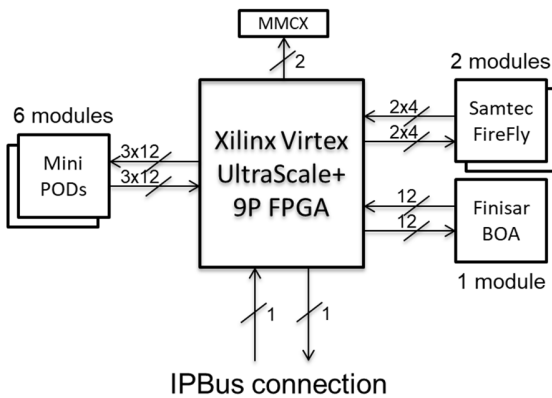

Fig. 6. Multi-gigabit transceiver connections of the FPGA on the Technological Demonstrator.

Such a custom design of the Demonstrator board allows evaluating the optical modules together with the FPGA operating on the same mainboard.

III. HIGH-SPEED PCB DESIGN CONSIDERATIONS

In order to optimize the signal integrity for the high-speed signals, dedicated high-speed PCB design techniques were used.

Thus, all the high-speed differential pairs adhere to strict physical and spacing constraints. Phase tuning is performed in order to stay within the phase tolerance limit. Appropriate in-pair spacing and trace width provide the 100 Ohm ± 10% differential impedance, while sufficient spacing across all pairs (4 times larger than the in-pair spacing) minimizes the crosstalk. Each high-speed signal trace is routed entirely on a single internal layer, apart from the transition areas between the outer and the inner layers, where ground vias are used in order to improve the signal integrity. The in-pair spacing is constant over the entire trace length.

Moreover, the stack-up (Fig. 7) is designed in such a way as to provide good signal integrity for high-speed signals. Signal planes are shielded by the ground planes, thus minimizing the crosstalk. High-speed signals occupy the top and bottom inner layers, and use microvias in order to avoid stubs on the signal lines. Buried vias are used as well in order to provide a better connection between the top and the bottom microvia layers.

Ultra-low transmission loss and highly heat resistant PCB material (MEGTRON6) is used for the PCB due to its good dielectric constant and dissipation factor for high frequencies.
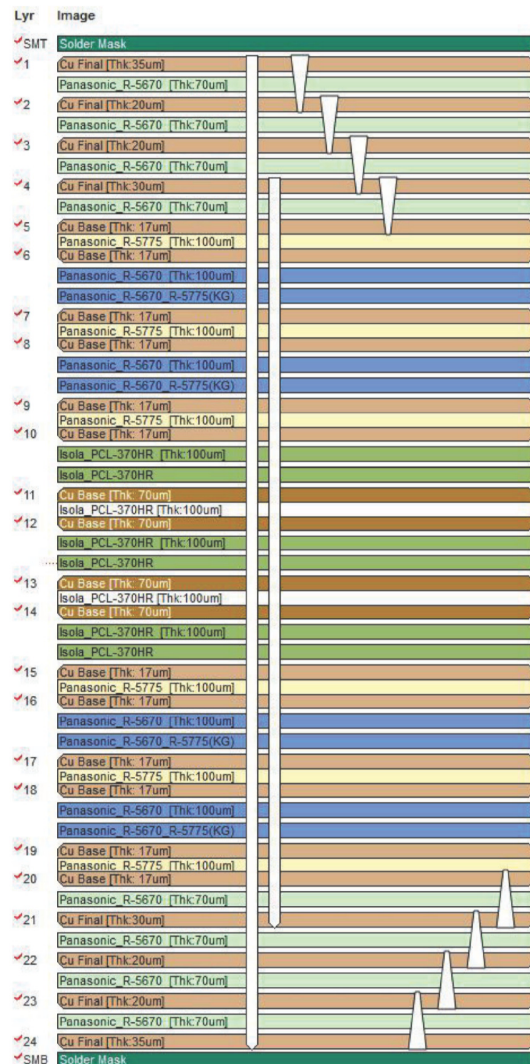

Fig. 7. Global Trigger Technological Demonstrator stack-up.

IV. PERFORMANCE EVALUATION

Performance of the high-speed optical modules and the FPGA has been evaluated with long-run link tests.

An Integrated Bit Error Ratio Test (IBERT) loopback test has been performed for the Finisar BOA optical module. In the test 12 transmitter links of the optical module were looped back to 12 receiver links of the same module with the help of a 24 to 2x12-fiber Y-cable and a 12-fiber trunk cable (Fig. 8).
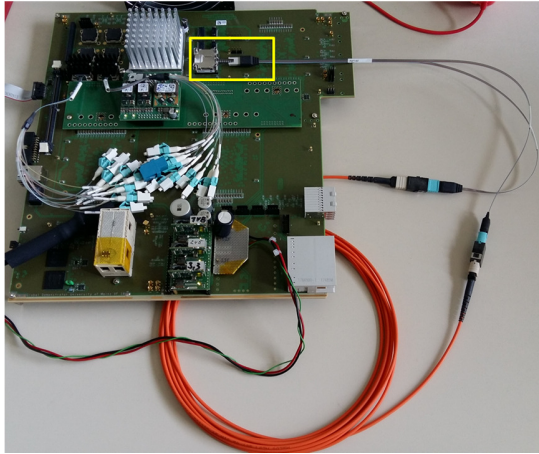

Fig. 8. Finisar BOA IBERT loopback test: test setup.

A day-long IBERT test run at 25.65 Gb/s, using a 31-bit PRBS pattern, has been performed. All 12 links are functional, and no bit errors have been detected (Fig. 9), measuring the BER down to $1.9 \cdot 10^{-15}$.

Fig. 9. Finisar BOA IBERT loopback test: links status.

A typical eye diagram, obtained using a low power mode of the GTY receiver, is shown in Fig. 10. With an open area and an open UI of 7608 and 57.58 % respectively, good performance of the Finisar BOA optical module is achieved.
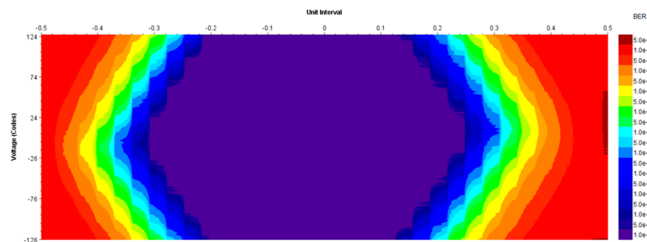

Fig. 10. Finisar BOA IBERT loopback test: a typical eye diagram.

Eye diagrams for other 11 optical links show a good eye-opening and overall good performance of the optical module (Fig. 11).
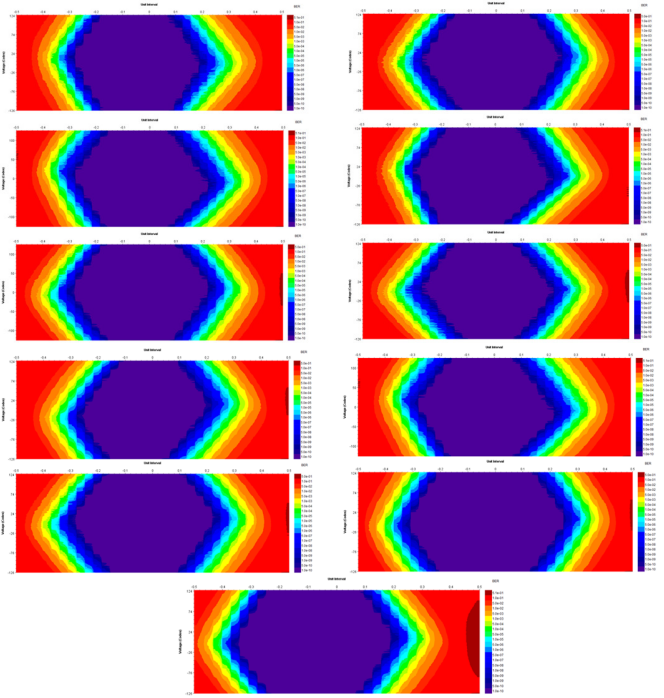

Fig. 11. Finisar BOA IBERT loopback test: eye diagrams for the rest of the optical links.

An IBERT loopback test has been performed for the Samtec FireFly optical module as well. In the test 4 transmitter links of the optical module were looped back to 4 receiver links of the same module with the help of a 12-fiber MTP to LC breakout cable (Fig. 12).
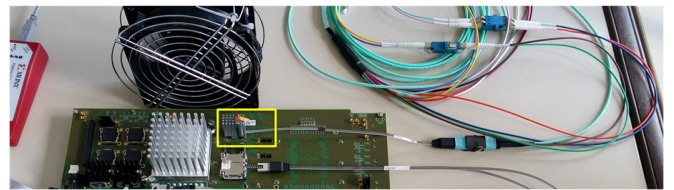

Fig. 12. Samtec FireFly IBERT loopback test: test setup.

A day-long IBERT test run at 27.58 Gb/s, using a 31-bit PRBS pattern, has been performed. All four links are functional, and no bit errors have been detected (Fig. 13), measuring the BER down to $1.7 \cdot 10^{-15}$.

Fig. 13. Samtec FireFly IBERT loopback test: links status.

A typical eye diagram, obtained using a low power mode of

the GTY receiver, is shown in Fig. 14. With an open area and an open UI of 8612 and 63.64 % respectively, good performance of the Samtec FireFly optical module is achieved.
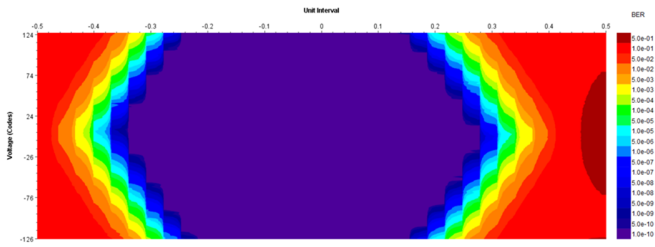

Fig. 14. Samtec FireFly IBERT loopback test: a typical eye diagram.

Eye diagrams for other three optical links show a good eye-opening and overall good performance of the optical module (Fig. 15).
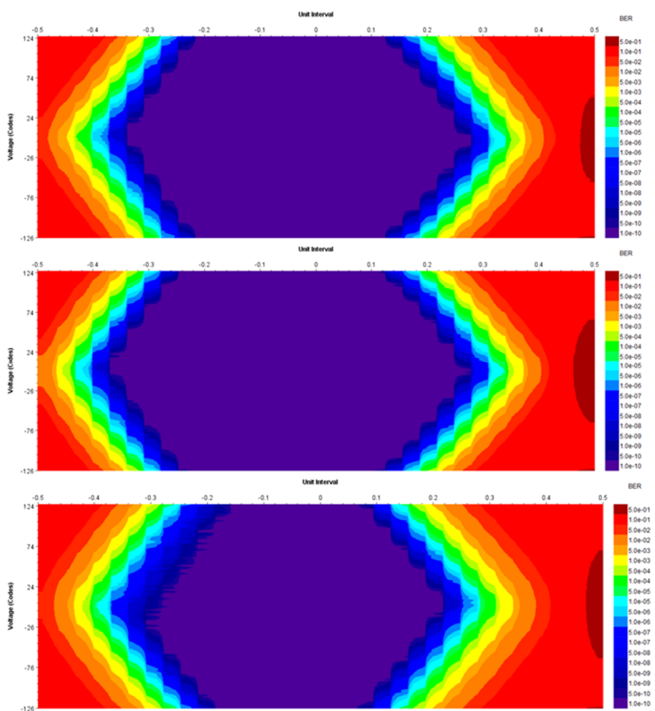

Fig. 15. Samtec FireFly IBERT loopback test: eye diagrams for the rest of the optical links.

V. CONCLUSION

The high-speed link support is essential for the Global Trigger system in order to cope with the transmission of high-granularity calorimeter data which drives the bandwidth requirements.

As a part of the R&D for the Phase-II Global Trigger System, a Technological Demonstrator has been designed and tested with a Xilinx Virtex UltraScale+ 9P FPGA and 28 Gb/s Samtec FireFly and Finisar BOA high-speed optical modules implemented on-board. A good performance and absence of bit errors during long runs have been demonstrated for both optical

modules. Due to a higher link density and a good performance, Finisar BOA is used for the PFM.

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