A new revision of the ATLAS Tile Calorimeter link Daughterboard for the HL-LHC.

Eduardo Valdes Santurio, Samuel Silverstein, Christian Bohm *Senior, IEEE*,
Katherine Dunne, Suhyun Lee, Holger Motzkau.

***Abstract*—The upgrade of ATLAS for the High Luminosity Large Hadron Collider (HL-LHC) has propelled gradual redesigns of the ATLAS Tile Calorimeter (TileCal) read-out link and control board (Daughterboard). The Daughterboard (DB) serves as a hub connecting the on- and off-detector electronics by means of two 4.6 Gbps downlinks and two redundant pairs of 9.6 Gbps uplinks. Two CERN radiation hard GBTx ASICs receive LHC timing and configuration commands through the downlinks, which are propagated to the front-end through Xilinx Kintex Ultrascale FPGAs. At the same time, the Kintex FPGAs continuously transmit redundant copies of high-speed read-out of digitized PMT samples, Detector Control System signals and monitoring data through the uplinks. The designs of the DB aim to reduce single points of failure and improve performance and reliability of the board. Mitigation of radiation damage and Single Event Upsets (SEUs) is done by employing a double-redundant scheme, using Xilinx Soft Error Mitigation (SEM) complemented by Triple Mode Redundancy (TMR) schemes in the FPGAs, adopting Forward Error Correction (FEC) in the downlinks and using Cyclic Redundancy Check (CRC) error verification in the redundant uplinks. With the revision 6 of the DB, we present a redesign that improves radiation tolerance by mitigating Single Event Latch-up (SEL) found in the Kintex Ultrascale+ architecture used in the previous board iteration, features a more robust power circuitry combined with a current monitoring scheme, enhances the performance of the ADC read-out, and improves the timing scheme of the design.**

***Index Terms*—HL-LHC, upgrade, radiation tolerant, SEL, SEE, NIEL, TMR, GBTx, TileCal, Daughterboard**

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I. Introduction

The Large Hadron Collider (LHC) is the most powerful particle accelerator to date consisting of a 27 kilometer tunnel that houses superconducting magnets and accelerating structures. Inside the LHC tunnel, two high-energy particle beams traveling at opposite directions are accelerated before they are made to collide in different points. At the collision points, experiments are placed to measure and characterize the particles produced in the collisions. The High-Luminosity LHC (HL-LHC) is the result of a series of upgrades to achieve up to five times the LHC nominal instantaneous luminosity, thereby allowing physicists to further study known mechanisms such as the Higgs boson, and potentially to observe rare new phenomena. Consequently, the data sample of the ATLAS experiment [1] will have to be enlarged by at least one order of magnitude compared with the LHC baseline. The increased luminosity will expose the on-detector read-out systems of ATLAS (Figure 1a) to higher radiation levels and increased rates of pileup. R&D work is ongoing to ensure that the read-out electronics of the upgraded ATLAS detector is capable of coping with the new HL-LHC requirements.

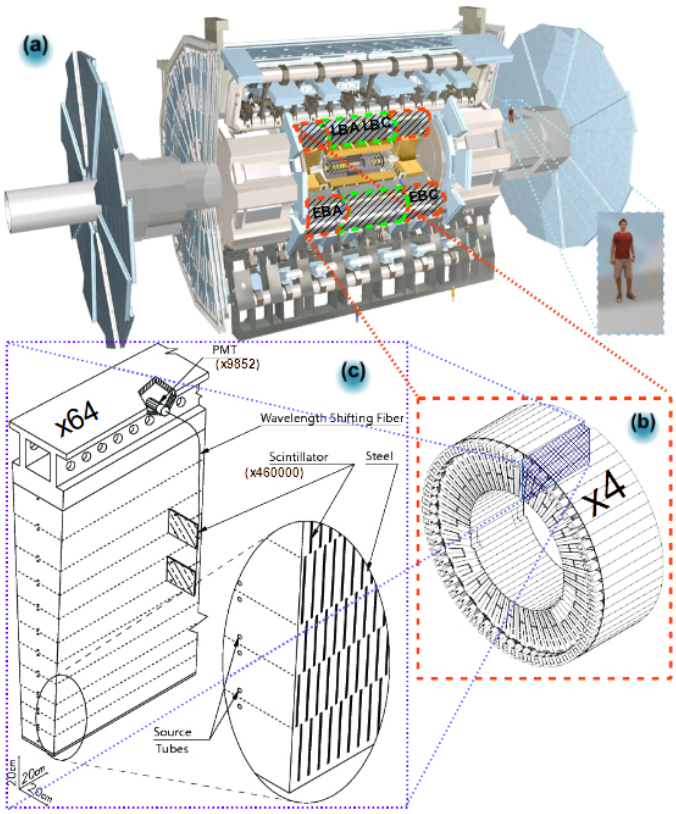

Fig. 1. (a) The ATLAS detector. (b) A TileCal barrel. (c) Depiction of a TileCal wedge-shaped module. [1]

II. ATLAS Tile Calorimeter

The ATLAS Hadronic Tile Calorimeter (TileCal) is a sampling calorimeter with plastic scintillator tiles and steel plates as active and absorber materials, respectively. TileCal is formed by three cylindrical barrels that altogether correspond to four partitions (Figure 1b). Each partition comprises 64

Eduardo Valdes Santurio, Fysikum, Stockholm University, email: eduardo.valdes@fysik.su.se, eduardo.valdes@cern.ch. Samuel Silverstein, Fysikum, Stockholm University, email: silver@fysik.su.se. Christian Bohm , Fysikum, Stockholm University, email: bohm@fysik.su.se. Katherine Dunne, Fysikum, Stockholm University, email: katherine.dunne@fysik.su.se. Suhyun Lee, Fysikum, Stockholm University, email: suhyun.lee@fysik.su.se. Holger Motzkau, Fysikum, Stockholm University, email: holger.motzkau@fysik.su.se.
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wedge-shaped modules (Figure 1c), each divided into cells that form pseudo-projective towers aimed at the interaction point. The light produced by the scintillating tiles in each cell is collected by wavelength shifting fibers and read out by a pair of PMTs.

All the current on- and off-detector electronics will be replaced in the HL-LHC upgrade to provide continuous digital read-out of all the calorimeter cells with lower electronic noise and better timing stability. The upgraded system will achieve less sensitivity to out-of-time pileup and better energy resolution [2]. The upgraded on-detector electronics will be tested for Total Ionizing Dose (TID), Non Ionizing Energy Loss (NIEL), and Single Event Effects (SEE), to prove its reliability when running in HL-LHC radiation environment conditions.

III. TileCal upgrade for the HL-LHC

The HL-LHC TileCal on-detector electronics are mechanically divided into 896 independent modules, so-called Minidrawers (MD, Figure 2a). Three or four MDs are inserted into the outer part of each wedge-shaped module to read out the scintillating fiber bunches, two bunches from each cell, one from each opposing side. Each MD consists of an aluminum mechanical structure that can house up to 12 PMT channels. A Front End board for the New Infrastructure with Calibration and signal Shaping (FENICS) card shapes, conditions and amplifies PMT analogue signals. A Mainboard (MB) receives and digitizes low- and high-gain amplified analogue signals corresponding to a 1:32 ratio from all the FENICs cards (Figure 2b).

A Daughterboard (DB), mounted onto the MB, serves as a hub between the on- and off detector systems (Figure 2b, c). The DB continuously reads, formats and transfers the data from 12 MB channels to the off-detector systems, while receiving and propagating LHC synchronized timing, control signals, and configuration commands to the front-end. In the off-detector systems, Tile PreProcessors (TilePPr) continuously receive and store PMT data in pipelines until reception of a trigger decision event, while providing processed and reconstructed data to the trigger system through the Trigger and Data Acquisition interface (TDAQi) and the Front-End Link eXchange (FELIX) system.

IV. The Daughterboard revision 5

The DB revision 5 (DB5, Figure 3) design follows a double redundant scheme where each half of the board is independently powered and can run the same functionalities as the other half separately. The two halves of the board, commonly referred to as side A and side B, share clock signals and communication buses with one another without interfering with each other's functionalities. Furthermore, four SFPs+ add an extra redundancy layer that allows nominal

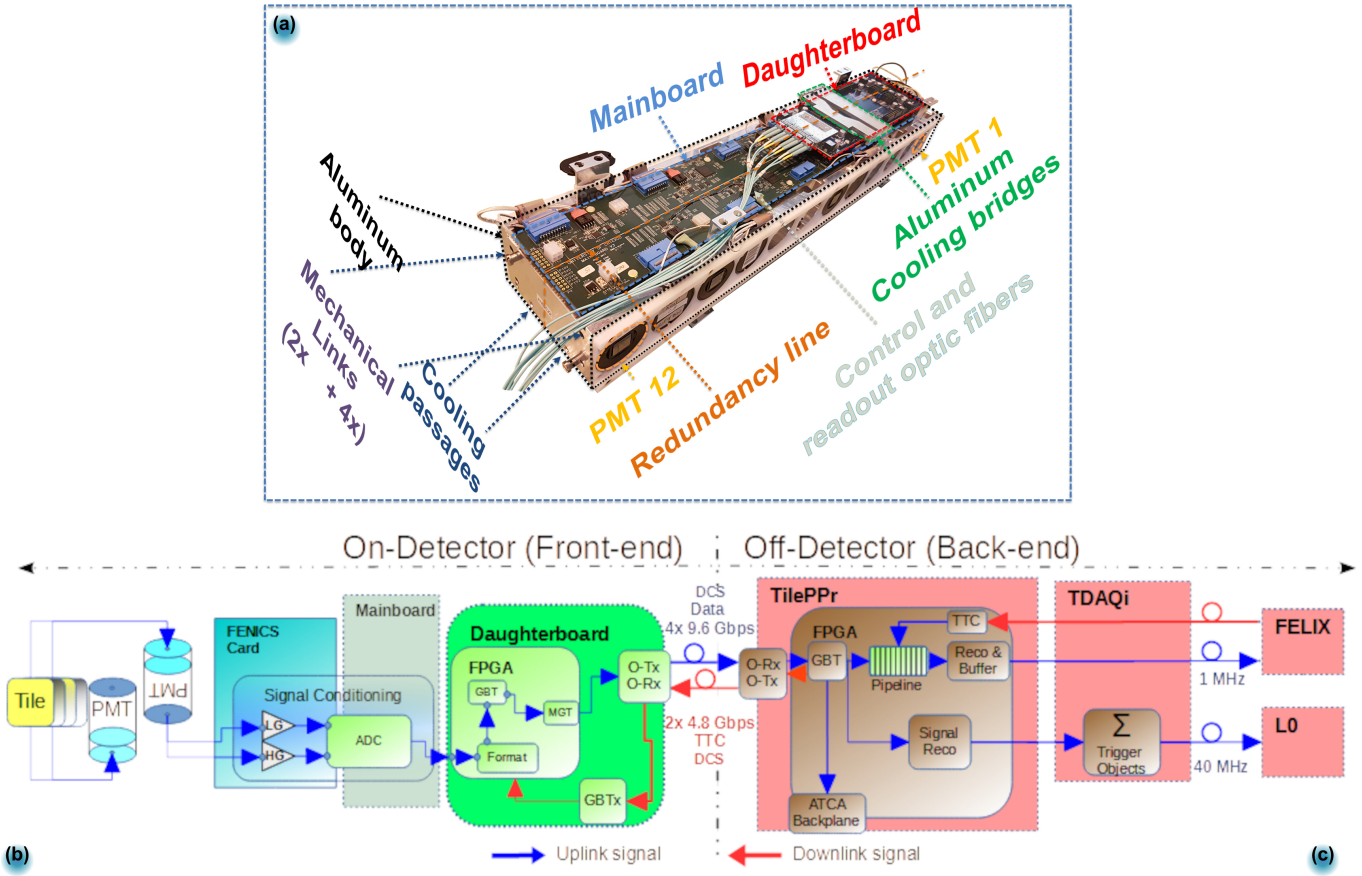

Fig. 2. TileCal HL-LHC Upgrade read-out system: (a) TileCal Phase-II Upgrade Minidrawer, (b) On-Detector electronics block diagram and (c) Off-Detector electronics block diagram.

running with two links, each sitting on opposite halves of the board can. Two SFP+ modules, each situated on different halves of the board, receive two redundant 4.8 Gbps links to a pair of CERN custom radiation tolerant ASICs (GBTx) [8]. Each GBTx ASIC recovers two 40 MHz Trigger, Timing and Control (TTC) synchronous clocks to drive the relevant logic of the Kintex Ultrascale+ (KU+) Field Programmable Gate Arrays (FPGAs), four 40 MHz TTC phase-configurable clocks to drive the digitizing blocks of each MB quadrant, and two 160 MHz (TTC) synchronous clocks to drive the GTY MGT (Multi-Gigabit transceiver) blocks of both KU+ FPGAs. Additionally, each GBTx ASIC decodes GBT-FEC protected words from off-detector to propagate configuration and control command signals, reset signals, and JTAG chain signals to both FPGAs through the dedicated GBTx ports (E-Ports). The GBTx propagated JTAG signals allow remote reconfiguration of the KU+ FPGAs and their attached PROMs. The KU+ FPGAs are powered by Triple Mode Redundancy (TMR) capable firmware that continuously transmits GBT-CRC protected words encoding the two gains of digitized data of all the MB PMT channels and Detector Control System (DCS) information to the back-end, by means of two pairs of redundant 9.6 Gbps read-out uplinks from each FPGA.

The earlier revisions featured Kintex-7 (K7) FPGAs powered by the older GTX MGT blocks, was found to be incompatible with the LHC timing [3]. The GTX MGTs are not specified for the interval from 9.4 to 9.8 Gbps, putting the bitrate of 9.6 Gbps outside of the specifications for the transceiver. Furthermore, the Quad-Phase-Locked-Loop (QPLL) modules of the GTX MGTs cannot deliver 9.6 Gbps with the clocks recovered in the DB without using a complex clocking scheme that introduces more noise and jitter to the GTX MGT reference clocks. This clocking scheme is not recommended by Xilinx and visibly impacts the stability and reliability of the links. Consequently, the DB5 design migrated to the Kintex Ultrascale+ FPGAs, powered by the newer GTY MGTs that allow 9.6 Gbps link communication. The KU+ architecture was chosen over the Kintex Ultrascale (KU) architecture to optimize the expected improvement on radiation tolerance, taking into consideration the lower cross-section for SEUs (Single Event Upsets) present in the KU+ with 16 nm FinFET technology compared to the K7 architecture with 28 nm TMSC process or even with the KU architecture featuring a 20 nm TMSC process [4].

The DB5 is backwards compatible with the interfaces of earlier revisions, such as the MB FPGA Mezzanine Card (FMC) docking connector, the Cesium calibration system connector (Cs Interface) and the on-detector high voltage interface (HV-OPTO). A custom connector routed to the Xilinx Analogue to Digital Converter (xADC) of each FPGAs was included for extra sensor signal monitoring, and new digital ID serial chips for unique digital identification of the MD.

V. TID, NIEL AND SEE RADIATION TESTS ON THE DAUGHTERBOARD 5

The DB5 TID test was performed with 9 MeV and 12 MeV electron beams, depositing a total of 20 kRad (Si) in the components of interest of the tested board. The design proved to withstand up to 20 kRad (Si), enough to be qualified for 10 years of HL-LHC radiation dose including safety factors. The test protocol followed the simulated radiation doses reported in the ATLAS Tile Calorimeter Phase-II Upgrade Technical Design Report [2]. Nonetheless, new simulations done with updated geometry showed new dose estimates that require TID testing up to either 72 kRad including safety factors or to 14.4 kRad if the test protocol includes annealing. The new simulated values were taken into consideration for the NIEL and SEE tests.

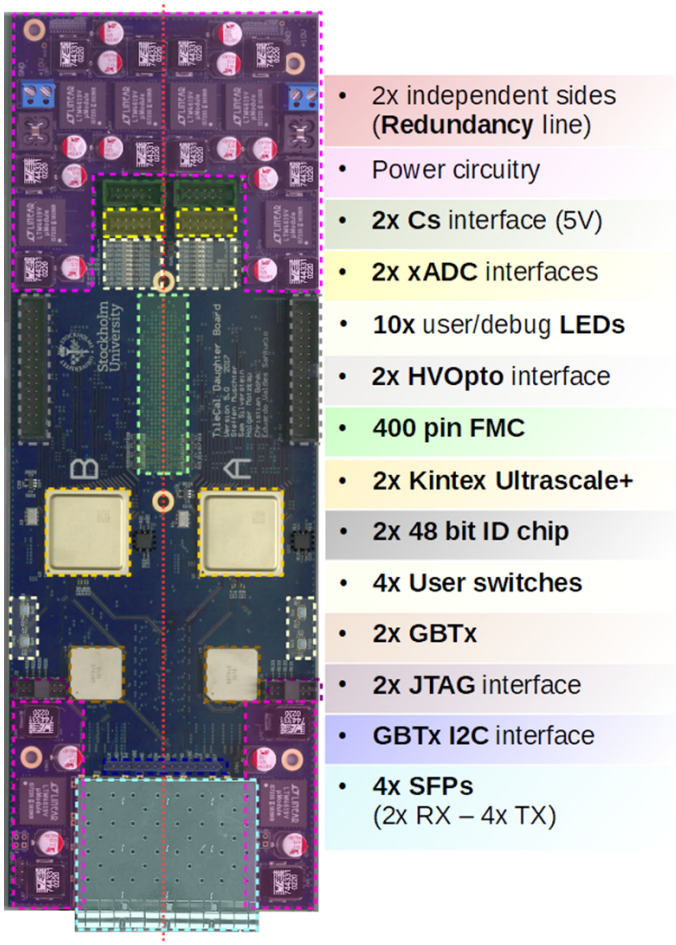

Fig. 3. The Daughterboard revision 5.

The NIEL test took place by achieving a total NIEL fluence corresponding to 9.00×10^{12} neutrons$\times$cm^{-2} (1 MeV equivalent neutron) by means of a 52 MeV proton beam. The test included two different SFP+ devices, AVAGO AFBR-709SMZ and the CORETEK CT-000NPP-SB1L-D. The irradiated AVAGO SFP+ micro-controller completely lost functionality, with no power consumption or signal detected when powered. On the other hand, the irradiated CORETEK SFP+ showed no detectable signal degradation. The DB5 irradiated GBTx ASICs and the FPGAs were severely damaged, showing electrical shorts on the various supply voltages. To reach the target fluence with a 52 MeV proton beam, the board was exposed to a TID of 768.2 kRad (Si) over a relatively small period of time of 84 minutes. In this case, the NIEL test was

considered inconclusive and a new test needs to be performed in a facility where the target fluence can be achieved with neutrons.

The SEE campaign comprised an SEU test performed with 58 MeV protons and an SEL test performed with 226 MeV protons. Both tests exhibited the SEL susceptibility of the KU+ 16 nm FinFET technology, with SEL-fluence rate increased from 2×10^{-11} at 58 MeV (Figure 4) to 2.36×10^{-10} at 226 MeV protons.

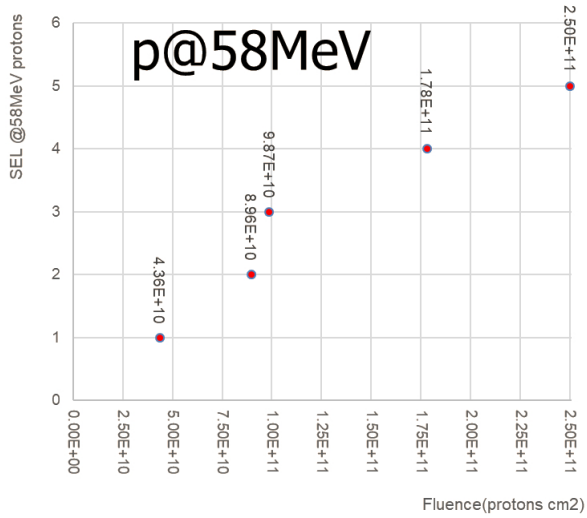

Fig. 4. Single Event Latchups test for the Daughterboard 5 seen during the SEU test performed with protons at 58 MeV.

A better characterization of the SEL events was performed during the SEL test with protons at 226 MeV protons (Figures 5 and 6). The exact mechanism for the over-currents induced by SEL is not well understood from the data. The SEL event starts with a drop of current followed by an over-current in the core voltage of the FPGA (VCORE). Afterwards, a slow and steady current rise leading to an over-current takes place in the 1.8 V powered banks. In the case of the DB5, these are the high-performance (HP) and configuration banks. Additionally, spontaneous drops in the currents for the 2.5 V and the 3.3 V of the high-range (HR) banks can be seen. The KU+ FPGA stopped functioning as soon as the VCORE over-current was triggered. Each over-current induced by SELs was mitigated with a quick power cycle.

Even though the KU+ FPGAs under test were exposed to over-currents for periods of time of around 60 s, the device functionalities were always recovered after a quick power cycle. Additionally, no detectable damage was seen in long runs performed with the irradiated board after the irradiation test was finished. Either way, hardware with the SEL rates measured is not acceptable for the HL-LHC ATLAS requirements. Therefore, solutions to mitigate SEL occurrence need to be included in the design.

The SEU tests were run up to a fluence of 2.50×10^{11} protons $\times$ cm^{-2} of which data for only a fluence of 2.05×10^{11} protons $\times$ cm^{-2} could be gathered due to the unexpected SEL over-currents interfering with the data taking process (Figure 7). The KU+ SEU rate calculated

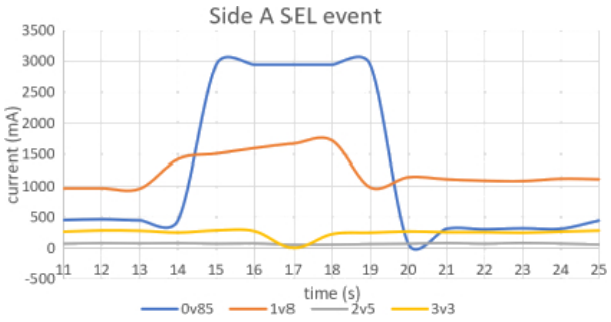

Fig. 5. Single Event Latchup over-current seen for side A of Daughterboard 5 during the SEU test performed with protons at 226 MeV. A quick power cycle was performed 5 s after the over-current appeared in the VCORE voltage.

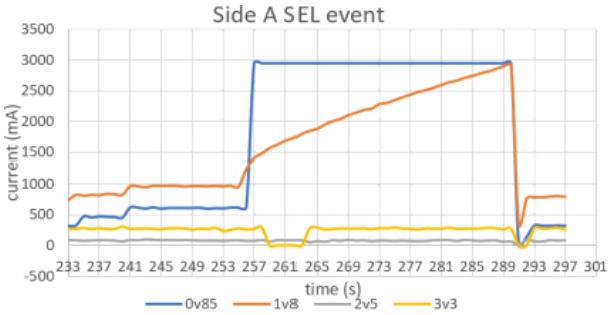

Fig. 6. Single Event Latchup over-current seen for side A of Daughterboard 5 during the SEU test performed with protons at 226 MeV. A quick power cycle was performed 40 s after the over-current appeared in the VCORE voltage to verify that the 1.8 V reached the 3 A maximum current measurable by the test.

from the data yields 24 SEUs per 10^9 proton $\times$ cm^{-2}. Out of a total of 4934 SEUs, 11 SEUs could not be corrected by the Xilinx SEM. The uncorrectable SEU rates measured mean that 1.4 $\pm$0.4 uncorrectable errors are expected per Daughterboard per year. The Xilinx SEM complemented with TMR strategies will assure that nominal runs will not be affected by uncorrectable SEUs.

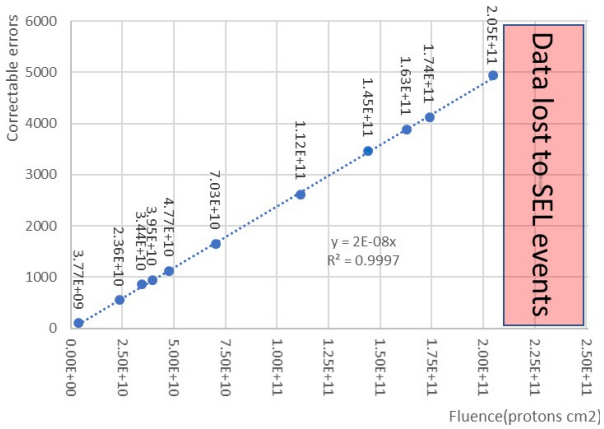

Fig. 7. Single Event Upsets for the KU+ FPGA in Daughterboard 5 performed with protons at 58 MeV. Each point represents the number of errors corrected by the Xilinx SEM before an uncorrectable error appeared. The firmware was re-loaded from the PROM after an uncorrectable error event. Data corresponding to a fluence of approximately 0.45 protons cm^{-2} was lost due to the SEL over-currents interfering with the data taking process.

VI. Motivations for Redesigning the Daughterboard Revision 5

The DB5 is a step forward when compared to the earlier revisions. The DB5 firmware has been under development and extensive testing has taken place in different testbenches connected to various prototype versions of the HL-LHC system. However, the design needs to move one step further by targeting some design flaws that interfere with the board robustness and reliability.

The DB5 power-on sequence was implemented by using an RC circuit, which can be sensitive to ageing, power ramping, or failure of one of the various LTM4619 DC-DC converters used in the board. Devices with multiple voltage inputs such as Xilinx FPGAs require a specific power-on sequence. A failure in one of the DC-DC converters can potentially cause further damage if not treated properly. A newer revision of the board should implement a power scheme with fail-safe power-up sequencing, while mitigating unexpected over-currents and any other power failures.

The interfaces between the GBTxs and the JTAG chains of both FPGAs malfunction upon instability or disconnection of the GBTx downlink. This malfunction is related to the instability of the RX_RDY signal and the DATA_VALID GBTx signals, used to enable the dedicated LVDS buffers in charge of translating the voltage standards between the GBTx E-Ports and JTAG chains of both FPGAs. The solution put into place is to use a small FPGA or Complex Programmable Logic Device (CPLD) to handle buffering, level translation and fan-out of signals between the GBTx signals and the main DB FPGA. This solution will allow TMR implementation in the selected device, more complex algorithms to enable or disable the interfaces and extra GBTx monitoring capabilities.

Full performance of the 9.6 Gbps uplinks was not achieved because of the jitter present in the GBTx de-skew clocks used to drive the GTY MGTs. To solve this problem, the reference clocks were routed to GBTx E-Link clocks, which have lower jitter than the GBTx de-skew clocks, by means of using the GTGREFCLK input of the GTY MGT. This scheme is not recommended by Xilinx. Therefore, further revisions of the DB need to use the GBTx E-Link clocks to drive the reference clocks of the MGTs. The DB5 was interfaced with various MB revisions, and the ADC read-out showed restricted performance due to non-optimal routing of the ADC clocks and data signals to the FPGA I/O banks at the board level. This issue needs to be addressed by optimizing the routing to assure that there are no timing violations during the implementation of the ADC readout firmware block. Additionally, the DB5 did not provide GBTx independent configurable de-skew clocks for both the ADC-readout and the charge injection calibration system. This scheme needs to be redesigned so that the eight de-skew channels of each GBTx can drive the ADC-readout and the charge injection calibration systems of the four quadrants of the MB.

The SEL rates measured during the SEE tests will be eliminated by migrating to an SEL-resistant FPGA. The Ultrascale family is powered by a 20 nm TSMC planar technology, where SELs have not been observed [5]. Migrating from the KU+ architecture to the KU architecture will increase the SEU rate by a factor of approximately 16 [4]. Regardless, a 16 times increase on the SEU rates is well within the mitigation capabilities of SEM and TMR.

VII. SEL Tests for the Daughterboard 6 Design

A KU FPGA, featuring a 20 nm TMSC process was chosen to execute the core functionalities of the DB6. This FPGA is powered by GTY MGTs that are compatible with the reference clocks recovered by the DB and is expected to provide manageable SEU rates. Two small FPGAs were chosen as candidates for buffering, voltage translation and fan-out between GBTx signals and the KU FPGA: a Microsemi ProASIC3 flash based FPGA and a Lattice ICE40LP FPGA based on Non-volatile Configuration Memory. Two Trenz TE0841

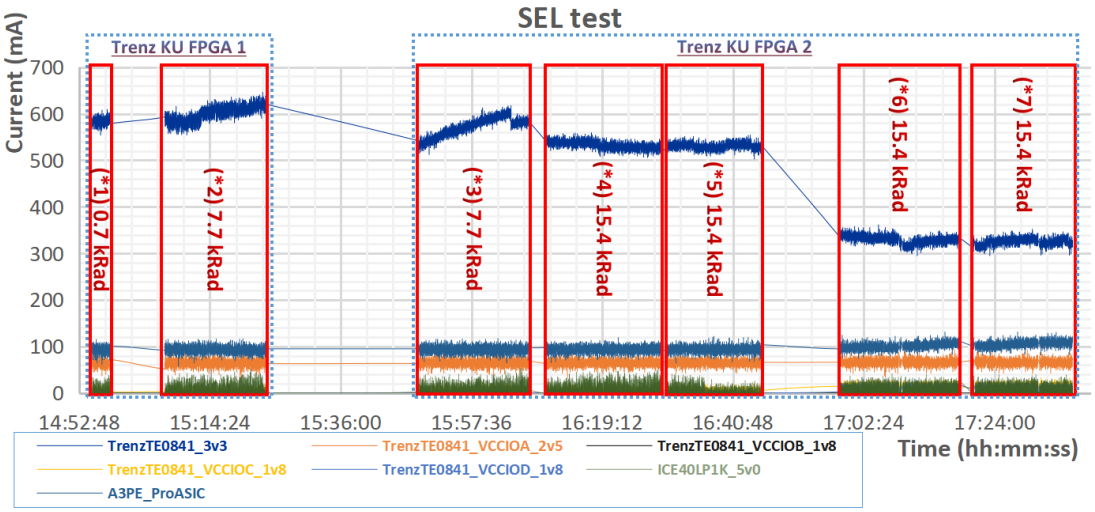

Fig. 8. Current monitoring data corresponding to SEL tests with protons at 226 MeV performed on two Trenz TE0841 micromodules (marked as Trenz KU FPGA 1 and Trenz KU FPGA 2), a Microsemi A3PE starter kit, and a Lattice ICEBLINK LP1K evaluation board. The irradiation took place over seven runs, each signalized in the red boxes with (*x) followed the corresponding deposited TID dose.

micromodules with a Xilinx KU035 FPGA each, a Microsemi A3PE starter kit, and a Lattice ICEBLINK LP1K evaluation board were exposed to a fluence of 1.2×10^{11}protons$\times$cm^{-2} delivered by a 226 MeV proton beam to cover 10 years of HL-LHC plus safety factors.

Figure 8 shows the evolution of the currents monitored for all the devices under test over the whole delivered dose. No SEL were detected over the whole delivered fluence for any of the devices. The test was divided in seven runs with runs 1 and 2 done with the first Trenz micromodule and runs 3 to 7 done with the second one. A firmware with Xilinx SEM was programmed on the KU FPGAs of the Trenz TE0841 micromodules to gather SEU rates for 226 MeV protons by means of a virtual input-output device though the JTAG chain. The Trenz micromodules FPGA JTAG chain is buffered by a LCMXO2 Lattice CPLD that was indirectly irradiated due to its proximity to the KU FPGA. The LCMXO2 CPLDs of the TE0841 boards 1 and 2 stopped functioning after 5.4 kRad and 6.9 of TID deposited respectively. For both CPLDs the current consumption steadily increased with the deposited dose until the device failed (Figure 8: runs 1 and 2 for TE0841 board 1 and run 3 for TE0841 board 2). The CPLD of the TE0841 board 2 was irradiated further, showing signals of functionality and stable power consumption up to 31.5 kRad (Figure 8: ending of run 3, plus runs 4 and 5). Afterwards the power consumption of the CPLD entirely dropped and no signs of any functionality were seen. It was verified that these two CPLDs failed by replacing them with new ones on the irradiated boards after the tests were done and the boards were cooled from the activation processes involved during the irradiation with high energy protons. As a consequence of the early failure of the CPLD, only rough SEU estimates could be determined. Around 166 SEUs per 10^9 proton$\times$cm^{-2} were measured for the KU tested at 226 MeV, accounting for approximately seven times more than the SEU rate of the KU+ tested at 58 MeV. Nonetheless, the test confirmed the use of the KU FPGA for the DB6, since it did not manifest SELs up to the delivered fluence and showed preliminary manageable SEU rates.

The ProASIC3 FPGA functionality was affected at approximately 58.3 kRad accounting for 75% of the total TID delivered. The functionality errors persisted after power cycling showing cumulative effects of the TID in flash based configuration memory. The Microsemi A3PE starter kit board was annealed after the irradiation test for a period of two months leading to full firmware functionalities being recovered. However, the re-configuration capabilities lost during the radiation test could not be recovered, seemingly because of the current pump mechanism being permanently damaged on the FPGA. The test outcome for the ProASIC3 matches the results reported by ACTEL in Ref. [9]. The FPGA of the Lattice ICEBLINK LP1K evaluation board functionality was affected after 10^9 proton$\times$cm^{-2}. However, the functionalities were recovered after a re-configuration of the device by means of a power-cycle. The ProASIC3 FPGA did not show SEL up to the delivered fluence, its 130 nm flash based configuration is preferable to the DB6 design and it is overall better supported by the manufacturer. Therefore, the ProASIC3 FPGA was chosen to handle buffering, level translation and fan-out of signals between the GBTx signals and the main DB FPGA.

VIII. Redesign of the Daughterboard

The redesign of the DB aims to eradicate SEL radiation issues detected in DB5, incorporate a more robust power circuitry that can manage over-currents of any origin, incorporate a more robust timing design, and further minimize single points of failure. The new design should meet all above mentioned goals while maintaining backwards compatibility with previous interfaces, ensuring tolerance to expected TID doses and NIEL fluences, and keeping SEU rates manageable by Xilinx SEM and TMR strategies. The DB6 uses conductive polymer capacitors to avoid radiation induced problems potentially caused by the use of large electrolytic capacitors with the DC-DC regulators. The conductive polymer capacitors have been reported to be more radiation tolerant with no visible performance effects up to 200 kRad at 500 rad per hour [6].

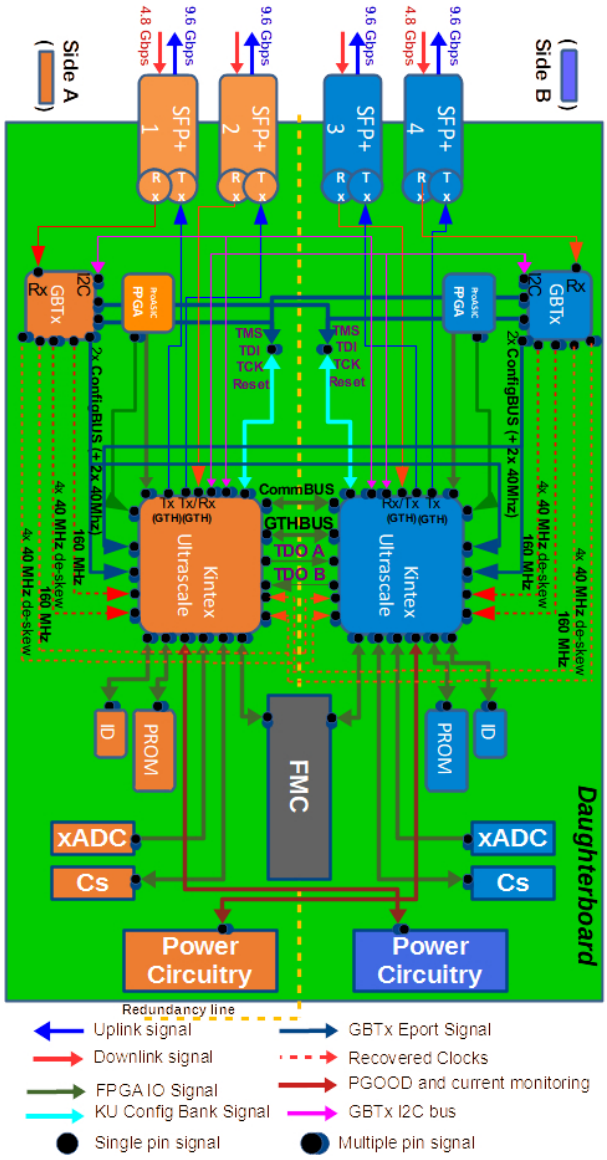

Fig. 9. The Daughterboard revision 6 block diagram.

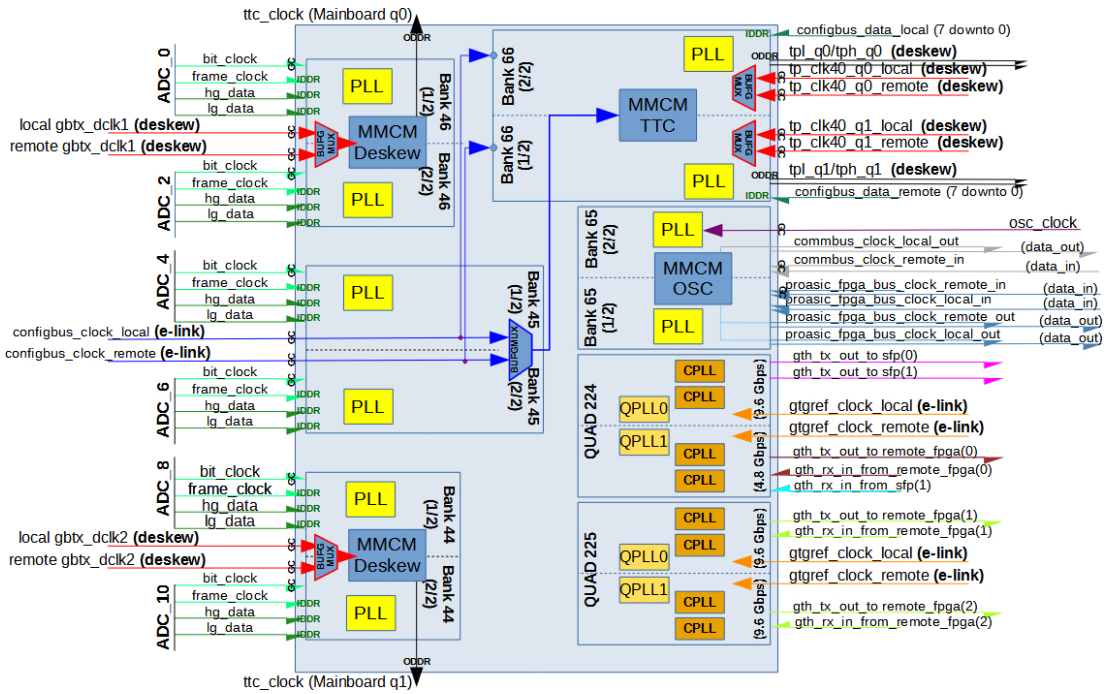

Fig. 10. Placement of clocks, ADC read-out pins, GTH signals, configbus interface and other clock dependent modules for XCKU035 FPGA to be used in DB6.

The DB6 features a power-up scheme that chains the DC-DC converters by means of the Power-Good (PGOOD) and RUN signals of the DC-DC converters, allowing to switch on each of the voltages in the order recommended by the various manufacturers of the different chips used in the board. Furthermore, the power circuitry is interfaced with a current limiting circuitry that powers-off the whole DC-DC converter chain if one of the voltages gets a current drain over a determined threshold. This scheme will effectively power-off the whole affected side in cases of failure of any of the voltages or over-current presence in any of the chain links. The DB6 will be more effective in preventing potential damages to the GBTx ASICs, the FPGAs or to any other components because of failures in the board power circuitry or unexpected over-currents. All the PGOOD signals and monitored currents are continuously sent to the off-detector system by the FPGA placed on the opposite side as part of DCS data. This extra layer of hardware control and monitoring contributes to minimize single points of failure and allows mitigation of any unexpected issues during nominal runs.

Figure 9 depicts a block diagram of the scheme followed for the DB6 design. The DB6 target FPGA chosen is the XCKU035 from the Ultrascale family, that features GTH transceivers fully compatible with the GBTx ASIC clocks and with the LHC timing. The DB6 will be capable of using the four downlinks, one on each side being connected to the corresponding GBTx ASIC, while each of the two remaining ones will be connected to the GTH MGT of the corresponding KU FPGA to test high-speed signal quality. CommBUS and GTHBUS are two multi-purpose independent buses that will handle communication between both KU FPGAs allowing signal monitoring, internal trigger commands, and data inter-change. CommBUS is a slow bus powered by IDDR/ODDR blocks situated on the KU GPIO banks, and GTHBUS is a 9.6 Gbps high speed bus powered by GTH transceivers.

The KU FPGAs read-out the dual-gain PMT digitized data and format them into GBT-CRC protected words. Figure 10 shows the routing scheme of the ADC signal groups and relevant time-dependent signals to the different banks for the DB6 KU FPGA. The DB6 optimizes the routing of the ADC signal groups to take advantage of the KU dedicated XYPHY BITSLICE byte groups architecture [7]. The bit-clock, the frame clock, the high-gain serial data, and the low-gain serial data signals coming from each ADC channel are connected to the same XYPHY BITSLICE byte group, to be read by means of the IDDR modules present on the IO blocks. Each ADC signal group corresponds to either byte group 1 or byte group 2, situated in the center of the FPGA bank used. This scheme allows access to the Phase Locked Loops (PLLs) and the Mixed-Mode Clock Manager (MMCM) of the bank by means of the dedicated Global Clock Capable IO pins (GCIO). Dedicating a byte group per channel mitigates unnecessary routing congestion to avoid more than six clocks driving IO loads on any half bank. BUFGMUX will multiplex the TTC LHC synchronized input clocks depending on which GBTx ASIC is selected to drive the FPGA logic and the ADC readout blocks.

Figure 11 show the scheme for the distribution of the DB6 de-skew clocks, including the maximum phase shifting value and the resolution per level. The fan-out process takes place by using the de-skew clocks to drive ODDR modules that serialize and output a standard logic vector shaped as a clock. The ODDR modules feature extra fine-tune phase shifting capabilities by means of ODELAY modules sitting on the IO

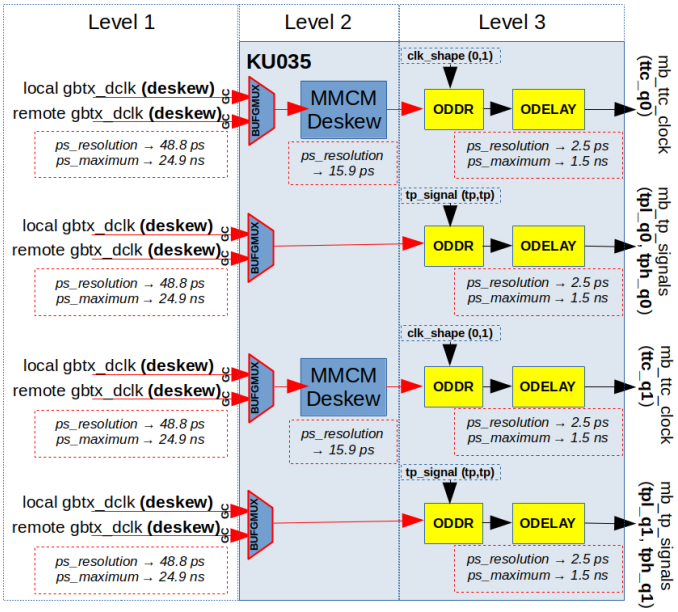

Fig. 11. De-skew clock path for one side of the Daughterboard revision 6. (ps_resolution: phase shift resolution, ps_maximum: phase shift maximum)

banks. Each KU FPGA will receive and fan-out eight 40 MHz de-skew clocks, four from the local GBTx ASIC and four from the remote GBTX ASIC. Four clocks out of those two groups are further de-skewed and fanned-out to the two MB quadrants sitting on the same FPGA side. Two clocks drive the ADC read-out and two clocks drive the charge injection calibration system. The de-skew clocks for the ADC read-out have three levels of phase shifting: starting in the GBTx ASIC, continuing with the MMCM and ending in the ODELAY modules. On the other hand, the charge injection calibration system only features two levels by not including the MMCM phase shifting capabilities to avoid unnecessary routing congestion.

IX. Conclusions

The DB is a read-out link and control board serving as a hub to interface the front-end electronics of a TileCal Minidrawer with the off-detector electronics. The DB6 migrated to a KU FPGA to avoid the SEL present on the KU+ FPGA. Further improvements on the DB radiation tolerance are achieved by using conductive polymer capacitors with the DC-DC regulators. The board components successfully passed the SEL test. TID, NIEL and SEU tests will take place during the first half of 2021 to qualify the board as required by ATLAS radiation policies. The DB6 features a new power circuitry with controlled power-up sequence interfaced with power monitoring that will power cycle the board side in the case of an over-current or a power failure. The design mitigates the previous problems related to the interface of the GBTx and the JTAG chain of the main FPGA by means of a ProASIC3 FPGA that controls, translates and fans-out the interface signals. Optimization of the ADC read-out modules and of the complex DB clocking scheme took place to improve the firmware timing closure and assure good performance during nominal runs. Dedicated phase configurable de-skew clock paths were included to drive the charge injection calibration system independently of the ADC-read-out block. The DB6 design was reviewed by the TileCal upgrade collaboration. Eight prototypes will be produced by the end of 2020. It is planned that 1085 DB6 will be produced as the contribution of Stockholm University to the ATLAS Upgrade for the HL-LHC era.

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