Inductive Adder for the FCC Injection Kicker System

Inductive Adder für das FCC Injektionskickersystem
Zur Erlangung des akademischen Grades Doktor-Ingenieur (Dr.-Ing.)
vorgelegte Dissertation von David Gerd Woog, geboren in Northeim, Deutschland
Fachbereich Elektrotechnik und Informationstechnik
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Zusammenfassung

Die vorliegende Dissertation beschreibt die Auslegung, Konstruktion, den Zusammenbau und die Ausmessung eines Inductive Adder (IA) Pulsgenerators. Der IA wurde für die Future Circular Collider (FCC) Studie ausgelegt, um die Möglichkeiten eines höchst zuverlässigen Pulsgenerators für Kickermagnetsysteme in Teilchenbeschleunigern zu erforschen.

Kickermagnete werden in Teilchenbeschleunigern verwendet, um den Teilchenstrahl abzulenken: z.B. bei der Injektion oder Extraktion des Teilchenstrahls in den oder aus dem Orbit eines Zirkularbeschleunigers. Aus verschiedenen Gründen können die Thyratrons, wie sie oft für die Pulsgeneratoren solcher Systeme eingesetzt werden, nicht für das FCC Kickersystem verwendet werden. Daher ist ein alternativer Pulsgenerator mit auf Halbleitern basierenden Schaltern (sog. solid-state Schalter) notwendig.

Halbleiter basierte Schalter sind eine vielversprechende Alternative, um Thyratrons in Pulsed-Power Anwendungen zu ersetzen. Dies wurde möglich, da durch die Weiterentwicklung halbleiterbasierter Bauelemente bezüglich Strom und Spannung in den vergangenen Jahren deutliche Fortschritte erzielt wurden. Die IA Technologie macht es möglich, mit mehreren Lagen und durch Parallelschaltung von solid-state Schaltern einen Pulsgenerator zu bauen, der Pulse mit hohen Spannungs- und Stromwerten erzeugen kann.

Ein IA, der die Injektionsparameter des FCC erfüllen kann, wurde bisher noch nicht gebaut. Daher wurde auf Basis dieser Parameter ein IA ausgelegt. Eine Herausforderung ist die Kombination aus 2.4 kA und 15 kV Ausgangspuls, 2.3 µs Pulslänge, 6.25 Ω Systemimpedanz und die kurze Anstiegszeit von etwa 75 ns (0.5 %-99.5 %) des Ausgangsstroms. Die Spezifikationen der Hauptkomponenten wurden definiert und Beispielkomponenten getestet. Neben Standardkomponenten für MOSFETs und Gatetreiber wurden z.B. für die Pulskondensatoren und Magnetkerne Maßanfertigungen benötigt.

Nach der Komponentenwahl wurden der magnetische Kreis ausgelegt, die Gehäuseteile produziert und der IA zusammengebaut. Um kurze Anstiegszeiten zu erreichen, musste das Design möglichst klein gehalten werden. Durch das Vormagnetisieren der Magnetkerne konnte das erforderliche Magnetmaterial nahezu halbiert und so auch die Höhe des IA verringert werden. Mit einer Ölisolierung konnte die Ausgangsspannung von 15 kV bei den durch die geringe Impedanz von 6.25 Ω bedingten Spaltmaßen realisiert werden und gleichzeitig die Durchmesser der Magnetkerne klein gehalten werden. Die Funktion von passiver, analoger Modulation konnte auch mit vormagnetisierten Magnetkernen gezeigt werden, was zur Reduzierung des Spannungsabfalls während des Impulses genutzt werden kann. Die geplante Ausgangsspannung von 15 kV konnte für einen Lastwiderstand von 50 Ω bei einer Impulslänge von 2.32 µs erfolgreich getestet werden. Auch der geplante Lagenausgangsstrom von 2.4 kA konnte bei der nominellen Lagenspannung von 1 kV erreicht werden.

Außerdem wurde ein Ansatz vorgestellt, der den Einsatz eines IA innerhalb eines Pulssystems mit Kurzschlussterminierung möglich macht. Dabei wurde mit Simulationen gezeigt, dass die Stromerhöhung

im Schaltelement vermieden werden kann, wenn durch das Schalten eines zweiten Schaltelements die Pulsimpedanz des IA verändert wird.

Die Herausforderungen des FCC Injektionssystems können mit den in dieser Dissertation gezeigten Methoden wie z.B. Siliziumkarbid MOSFETs, Ölisolierung, vormagnetisierten Magnetkernen und analoger Modulation bewältigt werden. Manche Verbesserungsmöglichkeiten des Designs, die sich im Laufe der Arbeit gezeigt haben, sind hervorgehoben und mögliche Lösungen werden diskutiert.

Diese Arbeit ermöglicht die Entwicklung eines IA für die Anforderungen des FCC Injektionskickersystems bei hohen Frequenzen, wie sie für einen so langen Zirkularbeschleuniger mit entsprechend vielen Vorbeschleunigern notwendig sind. Die Errungenschaften der Arbeit erlauben außerdem den Einsatz eines IA, um Pulsgeneratoren in bestehenden Teilchenbeschleunigern am CERN zu ersetzen. Hier hat der IA besonders durch den Einsatz von halbleiterbasierten Schaltern und sein kompaktes Design ohne SF6-Gas isolierte Komponenten oder Thyratrons Vorteile.

Abstract

This thesis presents the design, construction, assembly and measurements of an inductive adder (IA) type pulse generator. The IA was built for the future circular collider (FCC) study to investigate the possibility of a fast, high current, high voltage and reliable pulse generator for use in the injection kicker systems. In addition, the possibility of utilizing this technology as part of the injection system of an existing particle accelerator, with a generator voltage of up to 40 kV, is born in mind during the studies for the FCC injection IAs.

Kicker magnets are used in particle accelerators to deflect the beam for example during the injection process, to place the injected beam onto the central orbit of a circular accelerator. In order to achieve a high reliability for the FCC, it is necessary to replace the thyratrons presently used in the pulse generators of the kickers systems by pulse generators based on solid-state technology.

Solid-state switches are a promising alternative to thyratrons for pulsed power applications. Recent developments have increased the current and voltage ratings of power semiconductors and make it possible to use them for high current and voltage solid state pulse generators. The IA is a promising technology for generating high voltage and high current pulses: it consists of many ground-referenced layers, to achieve the high voltage, and many parallel connected solid state switches to achieve the high current capability.

An IA with demanding specifications as required for the FCC injection kicker system has never been built so far. The main challenge for such an IA is the combination of 2.4 kA and 15 kV output waveform, 2.3 µs flattop duration, 6.25 Ω system impedance and a short current rise time of approximately 75 ns (0.5 %-99.5 %). Based on these demanding requirements, an inductive adder was designed and simulated. The specifications for the main components of the IA were defined and sample components were ordered and tested. In addition to off-the-shelf components, such as SiC MOSFETs and gate drivers, some components required a custom made design e.g. pulse capacitors and magnetic cores.

After the components were selected, based on detailed analyses of tests and measurements, the hardware structure was designed and manufactured and a prototype IA was assembled. To obtain fast rise times, the height of the mechanical structure was reduced, by applying biasing to the magnetic cores, which made it possible to decrease the required volume of magnetic material in half. An oil insulation was selected to insulate the 15 kV output voltage and realise the low characteristic impedance of 6.25 Ω while keeping the diameter of the magnetic cores within an acceptable range. The principle of passive analogue modulation, together with biasing to reduce the flattop droop was proven. The required output voltage of 15 kV was achieved for a load impedance of 50 Ω with a pulse length of 2.32 µs. The specified layer output current of 2.4 kA was demonstrated with the nominal layer output voltage of 1 kV.

Furthermore, a theoretical approach to use the IA in a short-circuit terminated system is discussed. Simulations show that the increase of the current due to pulse reflection from a short-circuit can be prevented by adding a second switch in each branch of the IA to change the impedance of the stack.

The demanding requirements of the FCC injection system can be achieved by using the IA with presented technologies such as SiC MOSFETs, oil insulation, magnetic core biasing and passive analogue modulation. Some issues which require future work are discussed and possible improvements are proposed.

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List of Abbreviations

ALS-U	advanced light source upgrade
bd	breakdown
C	capacitor
CERN	European organization for nuclear research
CLIC	compact linear collider
CV	constant voltage
DARHT	dual-axis radiographic hydrodynamic test facility
DC	direct current
DNA	deoxyribonucleic acid
DR	damping ring
FCC	future circular collider
GaN	gallium nitride
GTO	gate turn-off thyristor
HEB	high energy booster
HEH	high energy hadron
hh	hadron-hadron
HV	high voltage
IA	inductive adder
ID	inner diameter
IVA	inductive voltage adder
IGBT	integrated gate bipolar transistor
KFA45	injection kicker system of the PS
L	inductor
LBNL	Lawrence Berkeley national laboratory
LHC	large hadron collider (particle accelerator at CERN)
LLNL	Lawrence Livermore national laboratory
LTD	linear transformer driver
LV	low voltage
MKI	injection kicker system of the LHC
MKP	injection kicker system of the SPS
MOD	modulation
MOSFET	metal oxide semiconducting field effect transistor
OD	outer diameter
PCB	printed circuit board
PFL	pulse forming line
PFN	pulse forming network
PS	proton synchrotron (particle accelerator at CERN)
R	resistor

RCPS	resonant charging power supply
rep	repetition
RF	radio frequency
RMS	root mean square
sc	semiconductor
SEB	single event burnout
SEE	single event effect
SF6	sulfur hexafluoride
SG	spark gap
Si	silicon
SiC	silicon carbide
SPS	super proton synchrotron (particle accelerator at CERN)
sw	switch
TDI	target dump injection
Trig	trigger

List of Symbols

A	m^2	area
A_c	m^2	actual cross section
A_{Fe}	m^2	effective cross section
B	T	magnetic flux density
B_r	T	remanence flux density
B_{sat}	T	saturation flux density
C	F	capacity
C_b	F	branch capacity
C_l	F	layer capacity
C_{layer}	F	parasitic capacitance of one layer
D	As/m^2	electric flux density
d	m	diameter
E	V/m	electric field strength
E_{max}	V/m	maximum electric field strength
f	Hz	frequency
H	A/m	magnetic field strength
h	m	height
I	A	electric current
i	-	index of summation
I_{out}	A	output current
I_{prim}	A	primary current
I_{sec}	A	secondary current
J	A/m^2	electric current density
l	m	length
L	H	inductance
L_{bias}	H	biasing inductance
L_{layer}	H	parasitic inductance of one layer
l_m	m	magnetic path length
L_m	m	mutual inductance
L_p	H	primary inductance of one layer
N	-	total number of layers
n_{branch}	-	number of branche
n_{layer}	-	number of layer
Q	C	electric charge
r	m	radius
R	Ω	resistance
R_{mod}	Ω	modulation resistance
S	-	scattering parameter

t	s	time
t_{prop}	s	porpagation time
V	V	voltage
V_{out}	V	output voltage
w	m	width
Z	Ω	impedance
Z_{IA}	Ω	characteristic impedance of the IA
δ	m	insulation gap
ε	As/Vm	permittivity
ε_0	As/Vm	permittivity of vacuum
ε_{r}	-	relative permittivity
η_{Fe}	-	fill factor
μ	Vs/Am	permeability
μ_0	Vs/Am	permeability of vacuum
μ_{r}	-	relative permeability
Ψ	Wb	magnetic flux

List of Subscripts

b	bias
bd	break down
bias	biasing
branch	parallel branch
c	magnetic core
cap	capacitor
ch	charging
coax	coaxial
CVlayer	constant voltage layer
f	fall
i	inner
ins	insulation
int	integrator
IA	inductive adder
l	load
layer	stacked layer
m	magnetizing
max	maximum value
MODlayer	modulation layer
o	outer
out	output
p	primary, pulse
prop	propagation
r	rise
s	stage
ss	secondary stray
tor	toroidal
tot	total
z	in axial direction
σ	stray parameter

1 Introduction and Motivation

In 1954 the European Organization for Nuclear Research (CERN) was founded and located in the area of Geneva. Scientists and researchers from the 22 member states and from all over the world are pushing the limits of physics to improve our understanding of the world we live in. Important and powerful tools for this research are particle accelerators and colliders which can accelerate particles to nearly the speed of light and collide them. Over the years of CERN's existence several particle accelerators have been built and used. The Large Hadron Collider (LHC), currently the biggest and most powerful particle accelerator in the world, was finished in 2008. Even if the LHC is the largest accelerator it is anyway only the last piece of a long acceleration chain consisting of many particle accelerators. Since a circular accelerator can only accelerate particles within a certain range of energy, pre-accelerators are needed. In Fig. 1.1 the CERN accelerator complex is shown. It can be seen that many machines of different sizes are accelerating different particle types for a diverse range of experiments.

The LHC with a nominal centre of mass energy of 14 TeV (7 TeV for each of the counter rotating beams) has a planned operation time span until 2035. Design, component construction, final assembly and startup of the LHC took around 30 years [20]. With this background it is obvious that the planning of an accelerator for the post LHC time should already start shortly after the LHC commissioning. For this reason a design study for a future circular collider (FCC) with a centre of mass energy of 100 TeV started in 2013. The FCC study investigates the challenges of a 100 TeV centre-of-mass energy hadron-hadron (hh) collider in the Geneva region. The proposed location of the FCC accelerator is shown in Fig. 1.2.

A big challenge from the technological point of view will be the injection of the particle beams from the pre-accelerator, also called high energy booster (HEB), into the FCC. Different HEB options are studied: The LHC can be used as pre-accelerator with a reduced beam energy of 3.3 TeV, the super proton synchrotron (SPS) could be upgraded with superconducting magnets to reach an energy of up to 3.3 TeV or a pre-accelerator could be placed in the same tunnel as the FCC. All options have advantages and disadvantages. The baseline is an injection energy of 3.3 TeV provided from the LHC [13, 85]. Due to machine protection reasons a fast and reliable injection system is required in any case. To provide a high reliability of the kicker system, the pulse generator design needs to be fundamentally different from existing former designs. Conventional pulse generator concepts at CERN (Pulse Forming Line (PFL) and Pulse Forming Network (PFN), described in section 2.4) use thyratrons to switch the high voltage and high current pulses which, under certain circumstances, can lead to issues concerning machine safety, reliability and availability [9]. Thyratrons are plasma switching devices which can pre-trigger and may lead to a mis-kick of the beam. Especially for the FCC, a high energy accelerator, a mis-kick of the beam must be avoided to prevent damage of the downstream accelerator equipment due to loss of the beam. To avoid this problem a new pulse generator design based on semiconductor switches instead of thyratrons is required.

First investigations for the FCC injection system showed that a field rise time of 430 ns and a field flat-top length of 2 µs, with a maximum ripple of ± 0.5 %, are required for injection at 3.3 TeV [68, 85]. Transmission

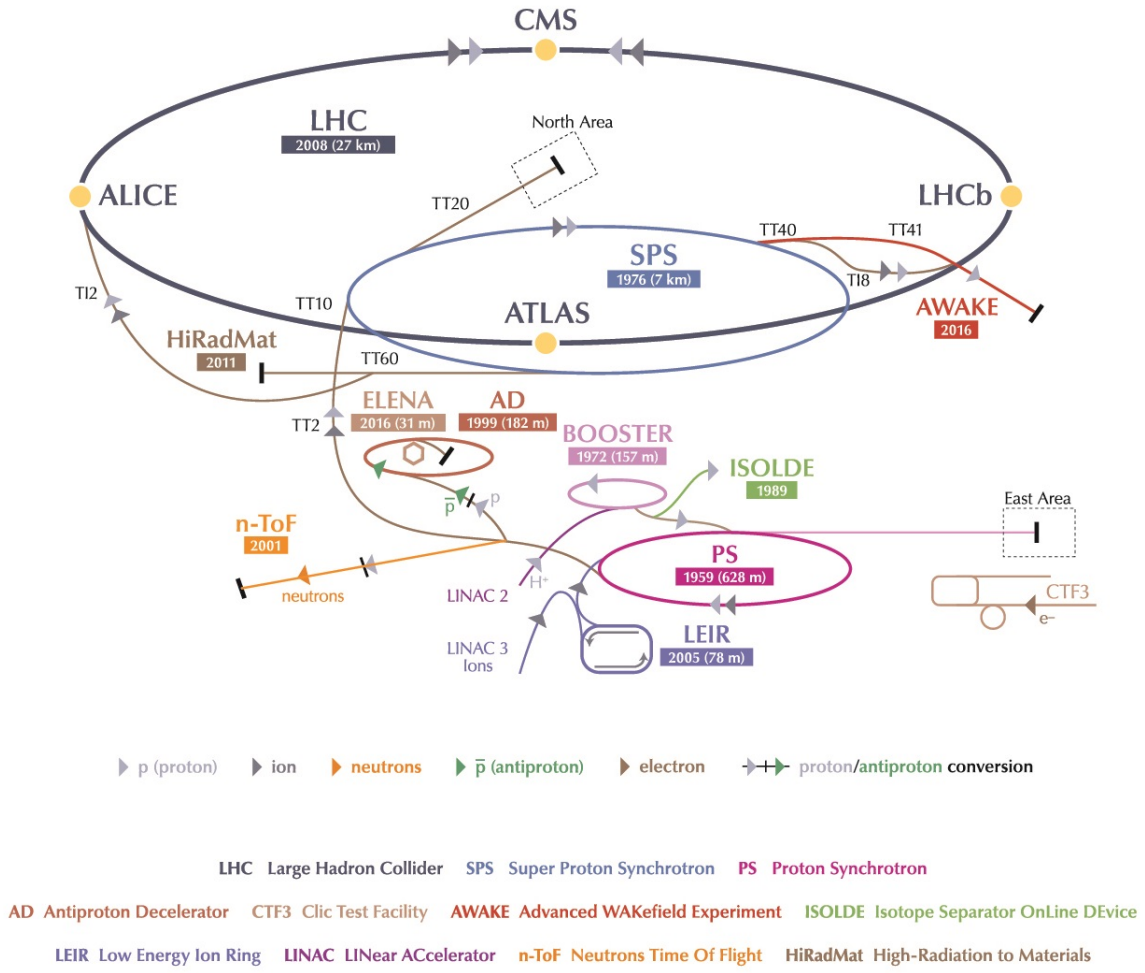

Figure 1.1: The CERN accelerator complex [40]

line kicker magnets, similar to the Large Hadron Collider (LHC) injection kicker design, will be used to achieve the fast rise time [29, 31]. The magnet delay time will be in the range of 355 ns hence the pulse generator is required to deliver a pulse rise time of below 75 ns [108]. A summary table of all requirements is given in chapter 4.1. The rather short pulse length allows the consideration of an inductive adder (IA) as a promising option. A major advantage of the IA is its modular design and all control electronics for the solid state switches are referenced to ground potential. The pulse requirements and the low system impedance, chosen for the transmission line kicker magnets [31], create several challenges. An IA as it is required for the FCC injection system has not been built yet.

The IA uses semiconductor based switching devices, instead of thyratrons. Semiconductor based devices, if properly designed and used, are more reliable than plasma switches such as thyratrons. Recent development in the semiconductor market, especially on wide band-gap devices for high power applications, made this technology available for this application. Further improvements in wide band-gap technology can be expected enlarging the design parameter space and facilitating future developments. Besides the switches the IA also brings other advantages compared to traditional pulse generator designs:
For the IA a PFL or PFN is not necessary. The components of the IA are common off-the-shelve components which makes it easy to source and replace them. It is possible to use components from different suppliers in

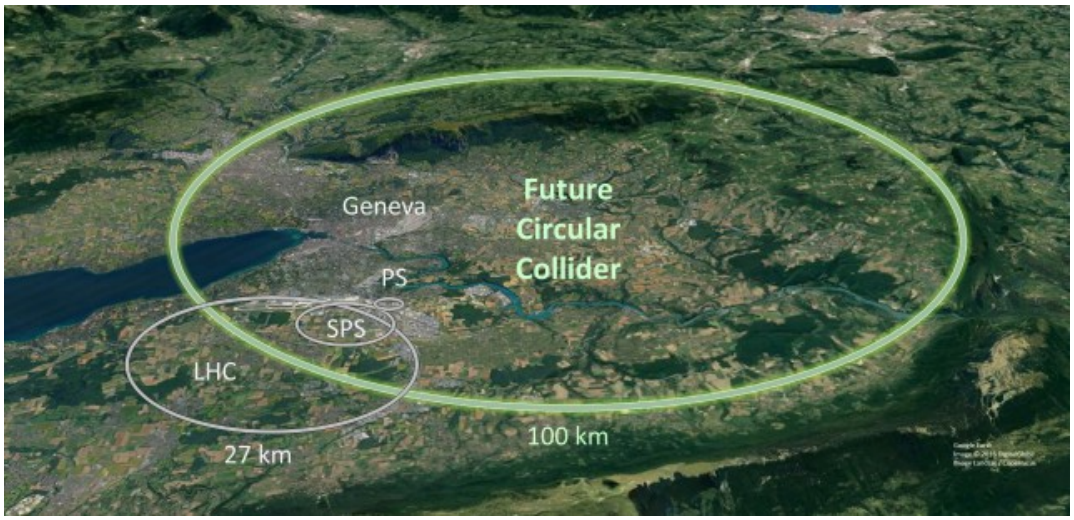

Figure 1.2: Schematic map of the proposed location of the future circular collider (FCC) [25]

one IA what gives more freedom in component selection and maintenance.

All the mentioned advantages of this new design make the IA not only interesting for kicker systems in future accelerators but also gives the opportunity to replace old generators in existing systems to reduce maintenance costs and profit from further advantages. This dissertation documents the design process, construction and measurements on an IA prototype that has been built for the FCC injection kicker system, reports the results and gives an overview of the challenges and possible improvements.

2 Fast pulsed systems

Pulsed systems are used in a wide range of applications in different fields. The focus of this thesis is on applications in experimental physics where pulsed systems are for example used for kicker systems in circular particle accelerators. Other applications where pulsed systems can be found are:

- Radar devices for the generation of radar waves [86]
- Test equipment for high voltage tests conducted on high voltage components [15, 18, 70]
- Electroporation in biotechnology or medicine where cell membranes are made porous to introduce DNA or other material inside the cell or to destroy the cell [17, 47, 78].
- Food processing applications where fruits or vegetables are exposed to high electric fields to improve further treatment [90, 91, 92]
- Research equipment for particle fusion, plasma or laser experiments to provide high power for a short time [18, 66, 104]
- Military applications, e.g. railguns [61, 72, 73]

The references show the big variety of requirements on the pulse systems depending on the application. Pulse lengths of tenth of ns for lasers and up to several ms for railguns, current values from several A up to several kA and voltages up to hundreds of kV are required for the different applications. Since the application of the pulse generator designed and built during this work is a power supply for a kicker magnet the following chapters are focused on pulsed power systems in particle accelerators and specifically kicker systems. Many examples of kicker systems will be related to CERN.

2.1 Injection and extraction systems

For circular particle accelerators the injection and extraction systems are of fundamental importance. Injection systems are injecting the beam from the transfer line from the pre-accelerator to the destination accelerator, onto the circular orbit of the destination accelerator. Extraction systems instead extract the beam from the orbit to the beam transfer line to an experiment, the next accelerator or the beam dump. These beam transitions are fundamental to reach high energy particle beams in a cascaded accelerator complex. Fast extraction and injection are realized with kicker magnets and septum magnets. In the following an injection system is described:

A septum magnet is a magnet with a constant field region and a field free region. The circular orbit of the accelerator is going through the field free region while the constant field region is part of the beam transfer line [8]. Since the two regions of the septum magnet are only separated by a very thin septum it is possible to bring the injected beam very close to the trajectory of the circular orbit. The last kick of the

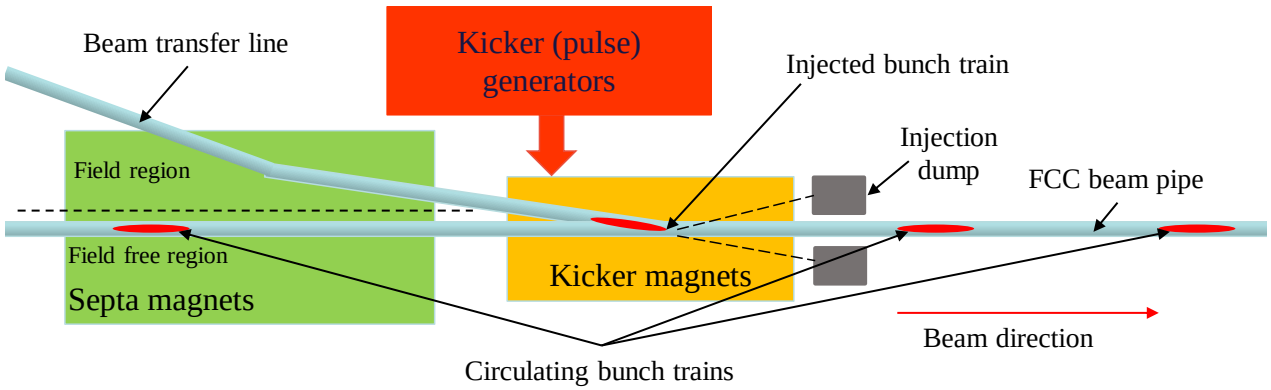

Figure 2.1: Schematic of an injection system with kicker magnet and septum magnet

injected particle beam that deflects the beam on the circular orbit is generated by a kicker magnet that is placed in the circular beam line of the accelerator. Figure 2.1 shows a schematic of an injection system with septum and kicker magnet.

A fast rising magnetic field of the kicker magnet is necessary to ensure only the injected beam is deflected and a fast fall time is required to not disturb the circulating beam [10]. Therefore the kicker magnet should generate a pulsed magnetic field with a smooth flat-top. To generate the pulsed field a pulse generator is required that serves as power supply for the kicker magnet and fulfills the pulse requirements in terms of voltage, current, rise and fall time, flat-top stability, flat-top length and repetition rate [5, 8, 10]. The different pulse parameters are explained in Figure 2.2.

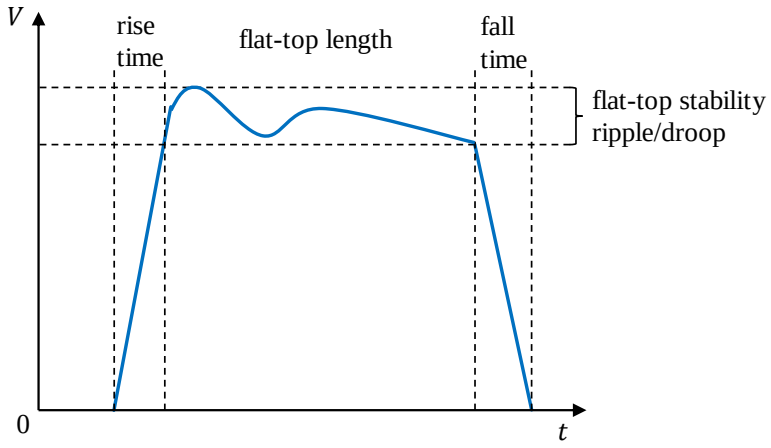

Figure 2.2: Definition of pulse parameters

Extraction systems work with the same principle as injection systems in reverse order and therefore contain the same components. The injection and extraction process is of high importance for an accelerator complex regarding the beam quality. If the pulse quality and subsequently the field quality of the kicker magnet are not within the tight limits the emittance of the injected beam may grow resulting in a poor beam quality.

2.2 Kicker systems at CERN

The first kicker systems at CERN during the 1960s were moved hydraulically into the beam line. They belonged to the Proton Synchrotron (PS) which started operation on the 24th of November in 1959 [26]. These so called plunging kickers were limited in rise time and aperture. In the 1970s with increasing beam intensity new kicker systems were developed to handle the more challenging requirements on aperture and rise time [45]. The new systems were designed as transmission line type kicker magnets with SF6-gas insulated pulse forming lines. Thyratrons were used as switching elements even though problems such as spontaneous triggering were well known. The relatively low beam energy and some technical improvements to reduce spontaneous triggering made it possible to use this technology in the PS until today [44].

The injection kicker system of the Super Proton Synchrotron (SPS), which was operating from 1976 on [27], contained twelve travelling wave magnets connected in pairs to six pulse generators [69]. The pulse generators were realised as thyratron based pulse forming networks (PFNs) with a maximum operation voltage of 60 kV and a maximum pulse duration of 12 μs. For the use of the SPS as injector for the LHC the injection system was modified to achieve faster rise times. The magnet length was reduced and the characteristic impedance increased. To compensate the missing kick strength four additional magnets and two pulse generators had been installed. To fulfill the requirements for proton and ion injection some modifications were carried out resulting in different injection systems depending on the particles [42].

In the LHC hadron injection kicker system (MKI) 4 kicker magnets of the transmission line type design are installed. Each magnet is supplied by one pulse generator realised as a PFN with thyratron switches [22, 41]. With increasing beam energy the effect of a mis-kicked beam and the protection of the machine against damage became more important [21]. Therefore the LHC is equipped with an injection dump (TDI) that absorbs beam losses caused by injection kicker failure [12]. Table 2.1 shows an overview of the injection kicker systems at CERN from the PS to the LHC.

Table 2.1: Comparison of injection kicker systems of the CERN accelerator complex

System	Unit	PS KFA45	SPS MKP	LHC MKI	FCC
Magnet design		transm. line	transm. line	transm. line	transm. line
Generator design		PFL	PFN	PFN	IA
Operation mode		short-circuit	terminated	terminated	terminated
Magnet impedance	Ω	26.3	12.5-16.67	5	6.25
Generator impedance	Ω	26.3	6.25-8.33	5	6.25
Magnet voltage	kV	40	50	25	15
Magnet current	kA	3.04	6-8	5	2.4
Rise time definition	%	5-95	0.5-99.5	0.5-99.5	0.5-99.5
Field rise time	ns	80	115-220	900	75
Field flat-top	μs	2.6	0.5-2.1	7.86	2.3
Flat-top ripple	%	±2	±0.5	±0.5	±0.5
Fall time	μs	0.104		3	1
Injection energy	GeV	1.4	14-26	450	3300

The beam dump system of an accelerator is used to safely dispose of the beam in case of any problem with

the machine or if the beam quality is not good enough for experiments. Even though the beam dump system is a pulsed system, the requirements on the kicker pulse quality are different to injection kicker systems - often flat-top ripple or a decaying sinusoid is required. Nevertheless the kick strength of the dump kicker system needs to follow the beam energy hence the generator of the system is always charged. The extraction kicker systems of a pre-accelerator are often of a similar design as the injection systems of the bigger accelerator since the beam energy is identical. Therefore the extraction kicker systems are not further described here.

2.3 Kicker magnets

The kicker magnet generates the pulsed magnetic field to deflect single particles, a bunch train or a particle beam of an accelerator. Kicker magnets can be designed to be inside or outside the machine vacuum. Both versions have advantages and disadvantages: in case the magnet is built outside the vacuum chamber it can have an easier design but requires a complex vacuum chamber e.g. made of metallized alumina that requires additional aperture. On the other hand, a kicker magnet inside the vacuum tank needs to be designed out of vacuum compatible materials and requires feedthroughs for all services but the vacuum can also improve the high voltage insulation [6, 10, 67]. Figure 2.3 shows an example for a kicker magnet inside and outside the vacuum chamber. Typical magnet designs are lumped inductance kickers or transmission

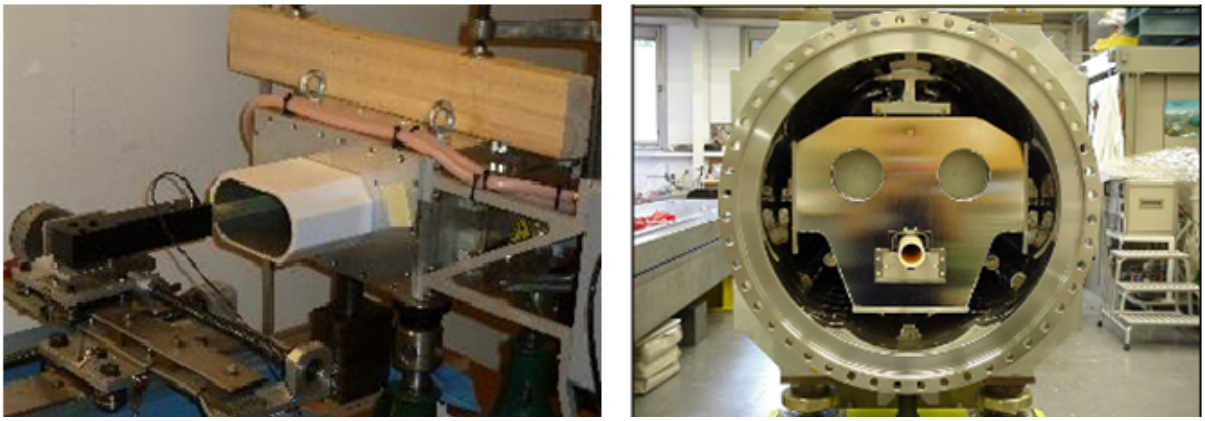

Figure 2.3: Left: Example for a kicker magnet outside vacuum. Right: Injection kicker magnet of the LHC inside the vacuum tank as an example for a kicker magnet inside vacuum [6].

line kickers. Lumped inductance kickers are used if fast rise times are not an important aspect. The magnet has a simple design and the generator should be located close to the magnet to reduce inductance [67]. For fast systems the transmission line kicker type is used. To achieve the fast rise time a transmission line kicker is manufactured with a single winding and consists of several cells. The cells contain of c-shaped ferrite cores in between HV plates and ground plates. In this way a broadband coaxial cable is approximated to realize a wide frequency range and therefore fast rise times. The fast rise time magnet design requires a matched impedance in the system to avoid reflections [5, 7, 10].

A different concept of kicker magnet is the stripline kicker magnet where the magnetic and electric field are both used to deflect the beam. It comprises two parallel conductors charged to a positive and negative voltage and a current flowing through the conductors in opposite directions. In the area between the

conductors the electric field, caused by the voltage difference and the magnetic field, caused by the current are overlaying and deflect particles in one direction [7].

Any type of kicker magnet can be operated in terminated and short-circuit mode. If a matched resistor is connected to the kicker magnet the system is terminated and after the pulse traveled through the magnet the current and voltage values are constant inside the magnet during the pulse. In case of a short-circuit at the output end of the kicker magnet the pulse is reflected and travels back, doubling the current and cancelling the voltage to zero resulting in a higher kick strength, for a given system impedance, PFN/PFL voltage and magnetic length, but also a longer field rise time. A more detailed description of pulsed systems with matched or short-circuit termination can be found in [54].

2.4 Pulse generators

A pulse generator is needed to supply the kicker magnet with the required power to generate the field. The pulse generator provides a certain current and voltage output to match the requirements for the needed magnet field magnitude, duration, rise time, fall time and ripple. Critical parameters are: current and voltage values, system impedance, pulse rise time, pulse fall time, droop, flat-top stability, pulse-to-pulse stability and repetition rate. Various pulse generator concepts, based on different technologies, can be used to match the requirements of different kicker systems. Some examples for pulse generator designs are explained in the following:

2.4.1 Thyratron switched pulse forming network or line

A common way to generate a pulse is to charge an energy storage network of capacitors and inductors and discharge it via a switch. The network can be realized with lumped elements and is then called a pulse forming network (PFN), or as a coaxial cable then it is called a pulse forming line (PFL). The single-way electrical length of the PFN/PFL should be at least half as long as the required pulse length. After the energy storage is charged with a resonant charging power supply (RCPS) to a voltage V the main switch connects it via a transmission line to a kicker magnet. During that process a negative voltage wave of $V/2$ is discharging the PFN/PFL and, if the dump switch remains off, it is reflected at the second end. Therefore the total length of the output pulse is twice the electric length of the storage network and the amplitude of the output pulse is half of the charging voltage. A basic component of a PFN/PFL pulse generator is the switching element that discharges the PFN/PFL into the load. In many designs a thyratron is used as switching device. Thyratrons are reliable plasma switching tubes that are able to withstand high overcurrents and can switch very fast. Disadvantages of a thyratron are e.g. high maintenance efforts, possibly required oil cooling and the risk of erratic triggering [9]. An example for a thyratron based PFL is the proton injection kicker system in the PS at CERN (Table 2.1). The simplified schematic of this system is shown in Fig. 2.4.

The described basic version of a pulse generator in a PFN/PFL design can be extended to a system with flexible flat-top length if a second thyratron is connected as a dump switch to the other end of the PFN/PFL. By triggering the dump thyratron before the discharge pulse has reached the end of the storage network, it is discharged from both ends and the pulse length is therefore shortened. If the kicker magnet is terminated the generated pulse is not reflected after travelling through the magnet. A schematic of such a system

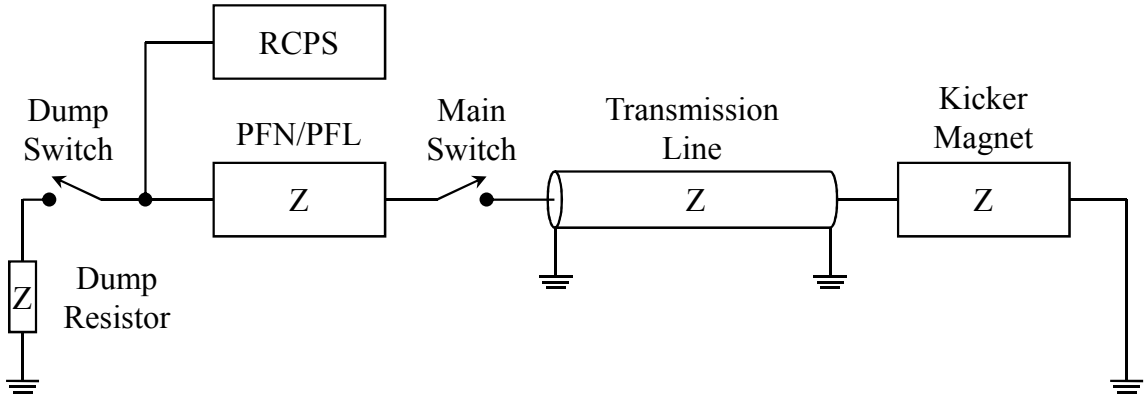

Figure 2.4: Schematic drawing of a kicker system with PFN or PFL in short-circuit operation with dump switch and dump resistor [7]

can be found in Fig. 2.4. If the kicker magnet is in short-circuit mode the generated pulse is reflected, cancelling out the voltage and doubling the current in the magnet.

Figure 2.5 shows the reel of PFLs for the KFA45 kicker system, which is used for proton injection in the proton synchrotron (PS) at CERN, and a high voltage thyratron. More detailed information and applications about PFN and PFL based pulse generators can be found in [15, 18, 34].

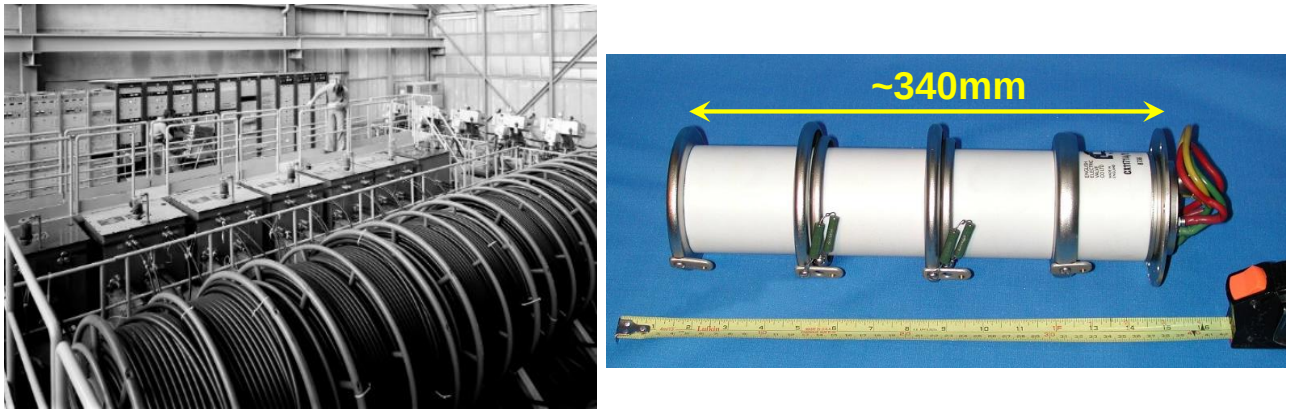

Figure 2.5: Left: Reels of PFL of the KFA45 pulse generator for the PS proton injection. Right: High voltage thyratron used for pulse generators at CERN [6].

2.4.2 Marx generator

The Marx generator is a standard equipment to generate high pulse voltages and was invented in 1923 by Erwin Marx and is still state of the art for many applications e.g. in high voltage test facilities. Fig. 2.6 shows the schematic of a multi stage Marx generator. The stage capacitors C_s can be charged in parallel

via the resistors R_l and R_e as shown in Fig. 2.6. If the spark gaps (SG) are triggered all capacitors are connected in series through the damping resistors R_d and the capacitor voltages of all n stages add up at the output voltage of the Marx generator. By changing the resistor values of the schematic the rise and fall times of the Marx generator can be adapted e.g. to generate a standardized lightning pulse wave form on a given load. In high voltage laboratories and test facilities normalized switching impulse voltages and lightning impulse voltages are generated by Marx generators. With well manufactured and adjusted spark gaps a very smooth operation can be obtained [86]. More detailed information, also about solid-state Marx generators, can be found in [14, 15, 18, 34, 52, 70].

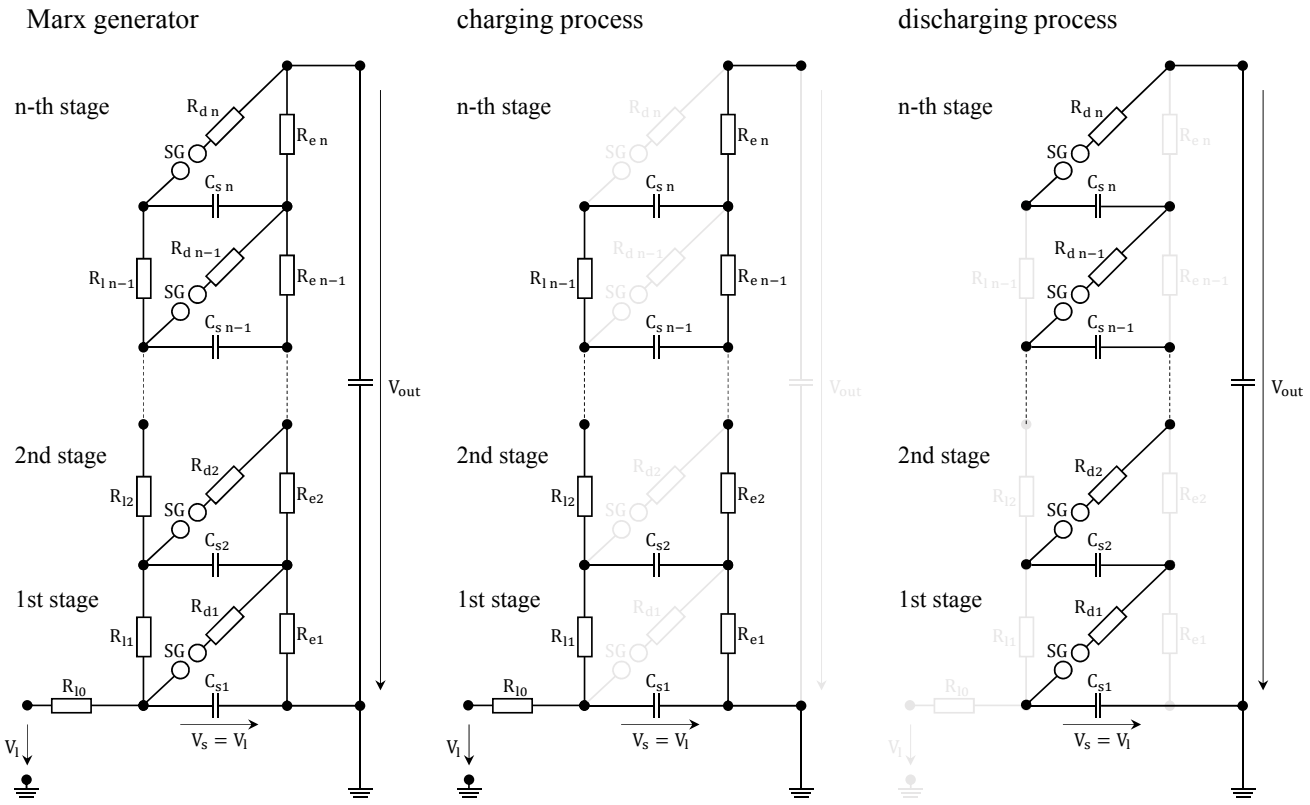

Figure 2.6: Schematic of a Marx generator after [15]. Left: full schematic, Center: active components during charging, Right: active components during discharging

2.4.3 Blumlein generator

Blumlein generators are often used in physics research experiments to generate electric pulses. The general principle is, as already described for the Marx generator, to charge two networks in parallel and discharge them in series. Two coaxial cables of single-way delay τ and with the same pulse impedance Z are connected via a high impedance load $R_\mathrm{l} = 2 \cdot Z$. If both cables are charged to the same voltage V and one end of the cables is switched to short-circuit, the load will see a voltage of V after τ that lasts for $2 \cdot \tau$. Further information regarding the Blumlein generator can be found in [15, 18].

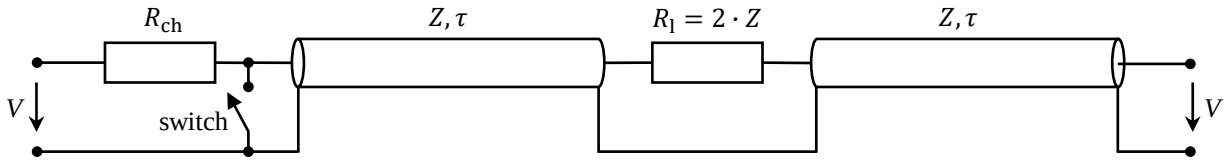

Figure 2.7: Schematic of a Blumlein generator according to [15]

2.4.4 Transmission line adder

The transmission line adder is a voltage adder that consists of several transmission lines connected in such a way that the pulses at the ends are adding up to a high output voltage. A capacitor serves as energy storage and can be discharged via a semiconductor switch into a coaxial cable. The inner conductor on the end of the cable is then connected to the outer conductor on the end of the next stage and so on as shown in Fig. 2.8. By putting correctly dimensioned ferrite cores around the end of the coaxial

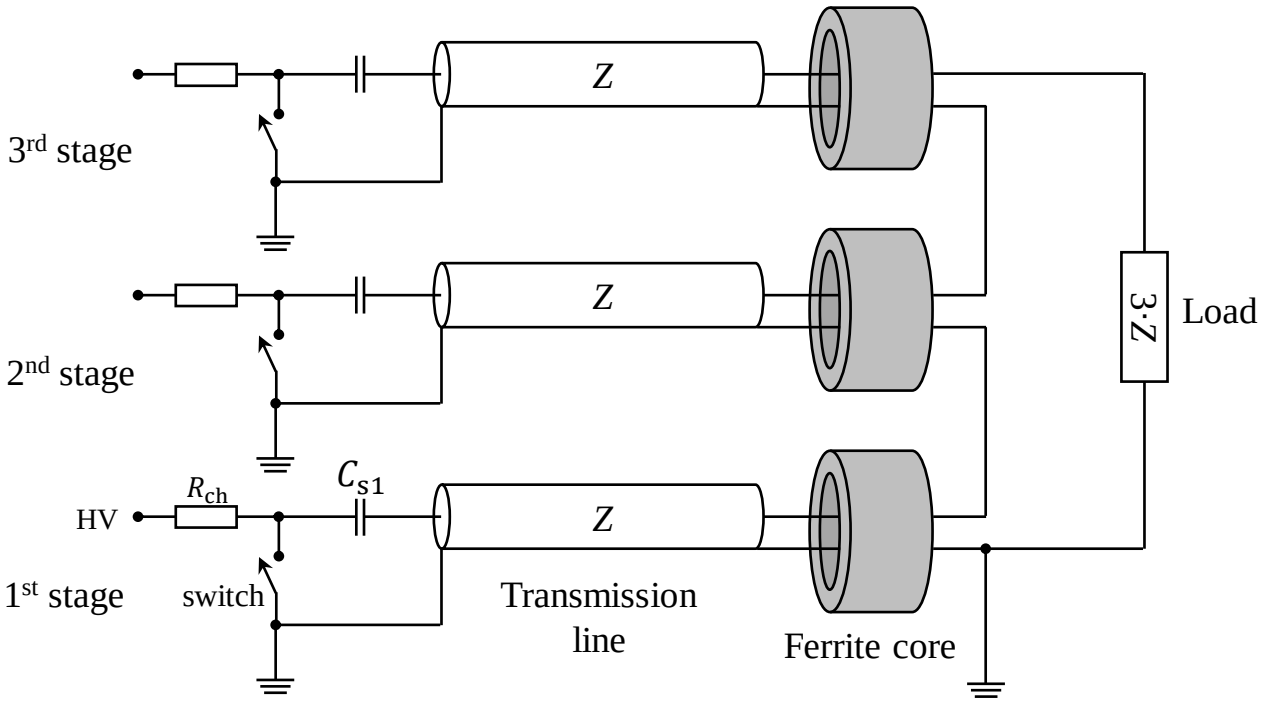

Figure 2.8: Schematic of a three stage transmission line adder according to [101]

cable of each stage a magnetic insulation is realised. The length of the cables needs to be long enough to avoid reflections of the pulse during flat-top. Therefore the transmission line adder is only used for short pulses since the cable length should be at least half the physical length of the output pulse flat-top. If the timing of the switches and the travelling time of the pulses is optimised, a very fast pulse rise time in ns range can be accieved [100, 101, 103]. Also the switching performance of the switch needs to be optimised for such short rise times [102]. For applications with several kV and higher load impedance, where very fast rise times and short pulses are required, the transmission line adder is an interesting option [23, 80, 82].

2.4.5 Other pulse generator designs

Marx generator, Blumlein generator and transmission line adder are just a brief overview of possible pulse generator designs. As it can be seen, many designs are taking advantage of the concept of charging capacitors in parallel and discharging them in series. Cascading a circuit with several stages to generate a higher output voltage is another common method and can be found in various applications to generate high AC voltages (cascading transformers [15, 70]) or DC voltages (Greinacher circuit [15, 70]). A different way to generate high voltage pulses is the pulse transformer. The pulse duration is limited by the saturation of the transformer core and a free wheeling current path needs to be added on the primary side of the transformer to avoid a negative backswing. Due to the high inductance of the windings of the transformer the rise time of the pulse is limited but can be optimised [15, 52].

2.4.6 Semiconductor based designs

All mentioned pulse generators are highly relying on the used switch in terms of performance and capabilities. Commonly used switches are spark gaps and thyratrons but also thyristors, which are semiconductor (sc) based closing switches and are only able to switch on. More advanced semiconductor switches such as MOSFETs and IGBTs have the ability to turn on and off. This improvement offers a wider range of options in the pulse generators. Nevertheless, semiconducting switches are not as capable in terms of current and voltage rating as gas switching devices. To reach comparable current and voltage values with semiconducting devices, components need to be switched in series and/or parallel. In case of parallel and series switching the thyratron can be replaced by many sc-switches and the PFN or PFL can still be used as the energy storing component. A problem of series connected sc-switches is the trigger system for the devices that are not grounded on the source pin. As an alternative design the solid state Marx generator can be mentioned. Important is the triggering of the switches in all stages. The trigger system of each stage needs to be galvanically insulated. As switching elements traditionally spark gaps are used but they can also be realised with sc-switches, which make the Marx generator more flexible [84, 89]. The galvanic insulated trigger system of each stage remains a challenge also for the solid state Marx generator. An example for an entirely new pulse generator design which can be realised with sc-switches is the inductive adder, which is described in section 3: the inductive adder does not require galvanically isolated trigger systems.

The used sc-components are usually silicon (Si) based metal oxide semiconductor field effect transistors (MOSFET) or integrated gate bipolar transistors (IGBT). During the last decades the silicon carbide (SiC) technology increased the performance of MOSFETs steadily. Components of several hundred A of pulse current and of up to 1.7 kV rated voltage are available on the market. Compared to Si based MOSFETs and IGBTs the switching time of SiC components is clearly improved and the on-state resistance of the device is reduced, which is important for pulse generators used in kicker systems with low characteristic impedance. This development encourages to think about a pulse generator design based on SiC MOSFETs as switching components.

2.4.7 Limitations of pulse generator designs

Currently used pulse generators in PFN/PFL design were very reliable during the past decades at CERN. During the last years maintenance efforts and the increased difficulties to source various components have become a major concern [112]. The cost of thyratrons recently increased significantly (≈ 20000 CHF): this

is due to the pricing policy of the manufacturer and the very limited number of manufacturers. Additionally, for environmental reasons, the use of sulfur hexafluoride gas (SF6) as part of the insulation medium in the PFL cables in several pulse generators should be reduced or avoided. The replacement of these 40 year old cables has become a big challenge [96].

Besides the maintenance and replacement problems also the erratic triggering is a limitation of a thyratron based pulse generator design. An erratic trigger is the ignition of the thyratron and therefore the generation of a pulse without a trigger signal [9, 60]. Thyratrons are plasma switches and therefore have a certain probability to ignite even if not triggered. The probability for this fault can be reduced by charging the PFN/PFL only a short time before the generator is triggered but can never be eliminated. Consequently accelerators at higher energies need to be equipped with collimation systems that protect the accelerator components downstream of the kicker magnet against the mis-kicked beam or particle showers. In case of higher energy, such as 3.3 TeV, a mis-kick can not be accepted anymore since machine protection efforts and the risk of a quenching superconducting magnet, resulting in downtime for quench recovery, are too high [9, 68].

A new, innovative, reliable and semiconductor based pulse generator would be a big advantage compared to traditional designs. A scalable and modular design that can be readily adapted to various kinds of systems and therefore easily maintained is another strong argument to look into new solutions. During the recent years semiconductor switch capabilities improved significantly in voltage and current capabilities and switching times have been gradually reduced. The mentioned disadvantages of traditional pulse generators and the technological achievements of the last years make it possible to look into a pulse generator design that can offer a highly reliable system, excellent pulse quality and low maintenance. Such a design would strongly improve the operation efforts of an accelerator complex like CERN.

This thesis shows how a semiconductor-based pulse generator, in this cse an inductive adder (IA), can be built for high current (2.4 kA), high voltage (15 kV), fast rise time (75 ns$, 0.5 - 99.5$ %) and relatively long pulse length (2.3 µs) to fulfill the pulse requirements for the FCC injection. The design and construction of the prototype is publised by the author in [108, 109, 110, 111, 112]. Investigations on the diode current peak after turn-off of an IA with low characteristic impedance were conducted by the author. The results are presented in chapter 4.3.2 and will be published. First investigations on the operation of an IA in a short circuited system are presented in chapter 9.

3 Inductive adder principle

Voltage adding is a common way to generate high voltage output pulses as described in section 2.4. In case of an inductive adder (IA) the voltages of the different stages are not added by directly switching them in series, as is the case for the Marx generator (section 2.4.2), but by connecting the output of many transformers in series and applying a pulse at the primary of all transformers at the same time. The principle of the inductive adder (IA) is also called inductive voltage adder (IVA) or linear transformer driver (LTD). As for many high voltage pulse generator designs, the IA also consists of several stages. Each stage consists of the primary circuit of a transformer, the transformer core and a secondary. The stages are built in such a way that the secondary winding passes through all transformer cores if the stages are stacked upon each other. In this way a stack of transformers is formed where the secondary windings are connected in series. Each stage has one or more primary circuits, consisting of a capacitor that can be discharged into the primary winding of the transformer through a switch. To reach short pulse rise

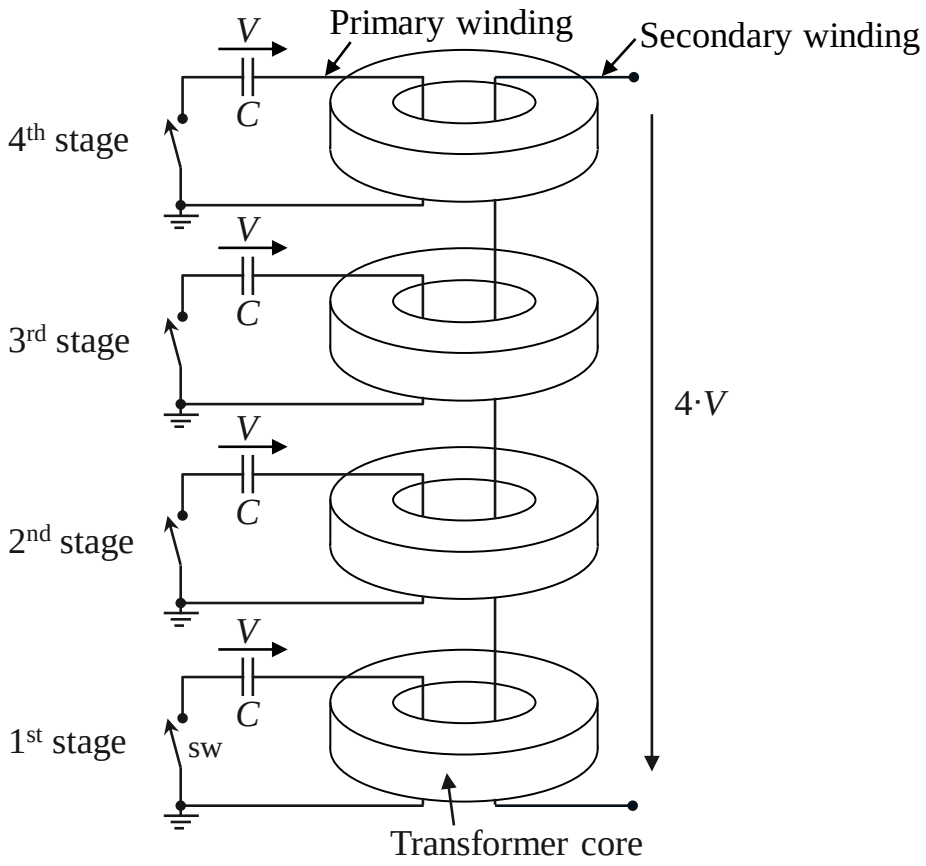

Figure 3.1: Simplified drawing of a 4-stage inductive adder

times the inductance of the primary and secondary circuit should be as small as possible. Therefore the primary winding has only one turn and fully encloses the toroidal magnetic core to minimize leakage inductance. The inductance of the secondary circuit needs to be low and is hence typically realised with only one turn that is passing through all toroidal transformer cores. A simplified schematic of the IA is shown in Fig. 3.1.

The coaxial structure formed by the primary winding, that is enclosing the magnetic core, and the secondary winding (also called stalk) defines the impedance of the generator. Parameters influencing the impedance are the ratio of the stalk diameter to the inner diameter of the primary winding. Further factors that influence the impedance are the insulating material between primary and secondary and the parasitic inductance of the primary circuit. In parallel to the transformer core a free wheeling diode is needed to provide a current path for the inductive current after switch off. The output voltage V_{out} of the IA is defined approximately by the capacitor charging voltage V_{c} of each layer and the number of layers n_{layer}: $V_{\text{out}} \approx V_{\text{C}} \cdot n_{\text{layer}}$. In this way the output voltage can be increased by adding more layers to the stack. Figure 3.2 shows the arrangement of the components for a 5 layer inductive adder. The coaxial structure formed by the primary winding, insulation and stalk can be seen. Important to note is that each layer is connected to ground potential on the primary side. In this way it is possible to have each switch connected to ground, which avoids problems with potential definition of gate drivers and makes a galvanic insulation unnecessary. The ground connection of each stage in the IA is a big advantage compared to the Marx generator.

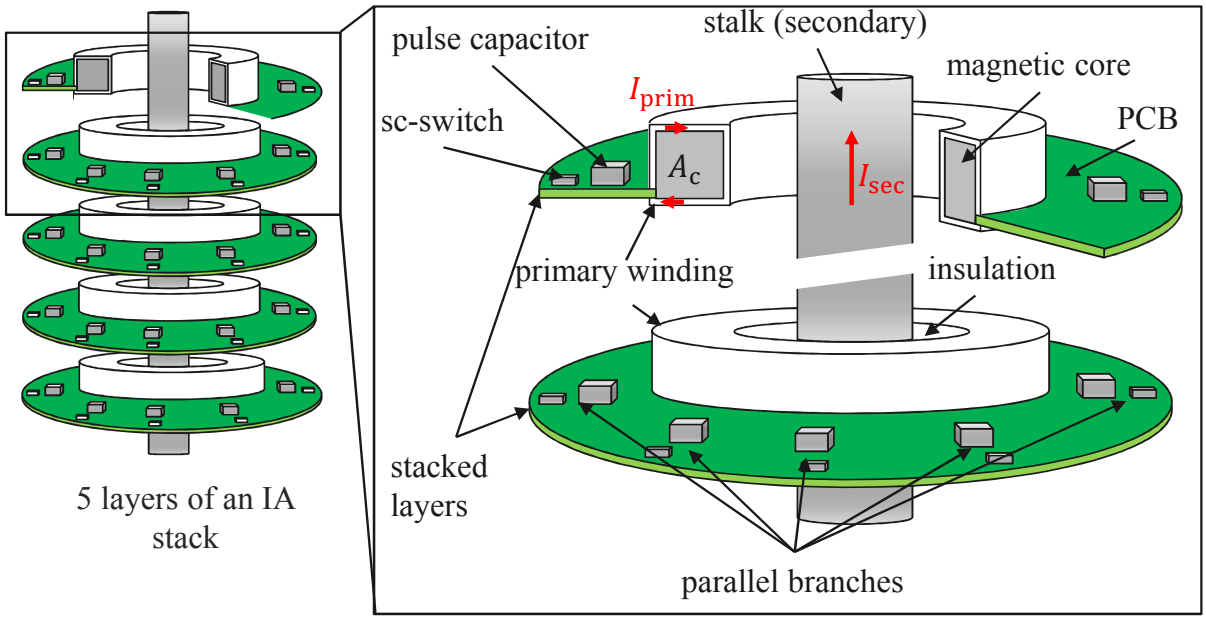

Figure 3.2: Schematic drawing of an inductive adder [112]. The primary circuit consists of: a printed circuit board (green) mounted around the magnetic core, the pulse capacitors, sc-switches and primary windings. The magnetic core is fully enclosed by the primary winding. Primary winding, insulation and stalk form a coaxial structure.

Whilst the voltage of each layer is just a fraction of the total output voltage, the output current in each layer is equal to the total output current. To increase the current capability of the primary circuit several branches, each consisting of capacitor and switch, are connected in parallel. For fast rise time of the output

pulse, simultaneous triggering of all parallel branches in one layer and of all stages needs to be ensured. A more detailed description of the functionality is given in chapter 3.4.

The principle functionality of the IA is based on induction accelerator cells [99]. If the secondary winding (stalk) of the IA is replaced by a ceramic beam pipe, a particle beam passing through the core is seeing the voltage applied at the primary circuit of the core. In such way particles can be accelerated or decelerated. Historically the induction accelerator was first developed and then the secondary circuit was added to build a high voltage pulse generator [32, 65].

3.1 Advantages and disadvantages

The IA can be used as a pulse generator with advantages compared to other designs [33]. In the following, a list of advantages is given:

- All major components of the design are exposed to a relatively low capacitor charging voltage. A high voltage only appears at the secondary winding (stalk).
- The IA consists of a modular design that can be easily scaled to various applications of different requirements.
- The components in the inductive adder are off-the-shelve components and can, under certain circumstances, easily be replaced by components with similar or better performance.
- Semiconductor switches like MOSFETs and IGBTs can be used, which provides higher dynamics than closing switches.
- Active ripple reduction and actively controlled output waveform shaping can be implemented in the design by using modulation layers (see section 3.5).
- Faulty single components or faulty modular elements in the design do not necessarily cause a total breakdown of the output waveform. Instead operation of the IA at a significant portion of its rated output voltage is still possible.
- All switching components can be directly referenced to ground.

Many advantages make the IA principle suitable for a pulse generator design with high reliability. Especially the advantage of a modular design where the fault of single modular elements does not cause the total fail of the generator is of paramount importance. This enables to further use the IA while minimizing unwanted beam losses. Nevertheless, the design of the inductive adder has some disadvantages which are listed below:

- The transformer is a fundamental part of the design and limits the possible output frequency range.
- The output pulse length is limited by the transformer core and its saturation properties.
- The IA has little over-current capability of semiconductor switches in case of fault conditions compared to plasma switch based designs.
- Using the inductive adder in systems with short-circuit termination is presently not feasible.

Hence, IA systems still require considerable research efforts.

3.2 Existing inductive adders

Several IAs exist in operation or as prototypes. This chapter will give an overview on the specifications of these devices. In Tab. 3.1 an overview of different IA type pulse generators is given. All listed IAs use MOSFETs as semiconductor switches. From Tab. 3.1 it can be concluded that several IA type pulse generators have been realized in a wide range of different pulse performance parameters. Output voltages of some kV up to tens of kV and current values up to 400 A have been reported. The load impedance (Z_{pulse}) is in the range of 25 up to $120\ \Omega$, whilst rise and fall times reach from less than 10 ns up to 100 ns. For a comparison of rise and fall times (t_{r}, t_{f}) their definition ($t_{\text{r,f}}$ def.) is an important factor e.g. 1 % to 99 %, 2 % to 98 %, 10 % to 90 %. Also in terms of IA size big differences of the compared IAs are observed, ranging from 8 layers and 8 branches up to 31 layers and 24 branches. Repetition rates of up to 100 Hz in continuous operation and even 1.6 MHz of burst operation have been reported. The max. pulse flat-top ripple of the compared IAs are in the low percentage range: generally less than 4 %. Impressive is the flat-top stability of the IA for the CLIC project of ± 0.02 % which has been optimised for very low flat-top ripples.

Table 3.1: Selection of existing inductive adder pulse generators in various laboratories worldwide

	Unit	LBNL ALS-U [105]	LLNL DARHT-2 [3, 35]	Nagaoka University [64]	CERN CLIC DR [59]	Pockels cell driver [1, 3]
V_{out}	kV	4.55	20	29	12.5	10
I_{out}	A	182	400	240	309	200
Z_{IA}	Ω	25	50	120	40.5	50
t_{p}	ns	50	16-200	50-170	900	86
t_{r}	ns	10-15	12	30-40	100	8.8
t_{f}	ns	10-15	10	30-40	100	12.8
$t_{\text{r,f}}$ def.	%	1-99	10-90	10-90	0.1-99.9	10-90
max. ripple	±%	1	<4	-	0.02	3
rep. rate	Hz	0.1	1.6M (burst)	100	50	10
Layers	-	8	31	30	20	15
Branches	-	8	24	24	8	12

3.2.1 Difference to transmission line adder

In [49, 50] the concept and prototype of an „inductive voltage adder“ is presented. The name suggests that the applied technology is similar to the inductive adder as described above. Moreover the prototype looks similar to some inductive adder prototypes. Nevertheless the setup is actually designed as a transmission line adder consisting of radial and coaxial transmission lines. Even if both, the inductive adder and the transmission line adder, are using magnetic material the application of this material is different: In the IA design the magnetic material serves as transformer core whereas in the transmission line adder the magnetic material is used as a transient inductive (magnetic) insulation between two potentials. Therefore the fundamental functionality of the inductive adder compared to the transmission line adder is different.

3.3 Equivalent circuit of the inductive adder

An equivalent circuit of the IA is important for assisting in the design of an indctive adder and other calculations or simulations. Based on the equivalent circuit presented in [55] and [114], an equivalent circuit of one IA layer was developed which is presented in Fig. 3.3.

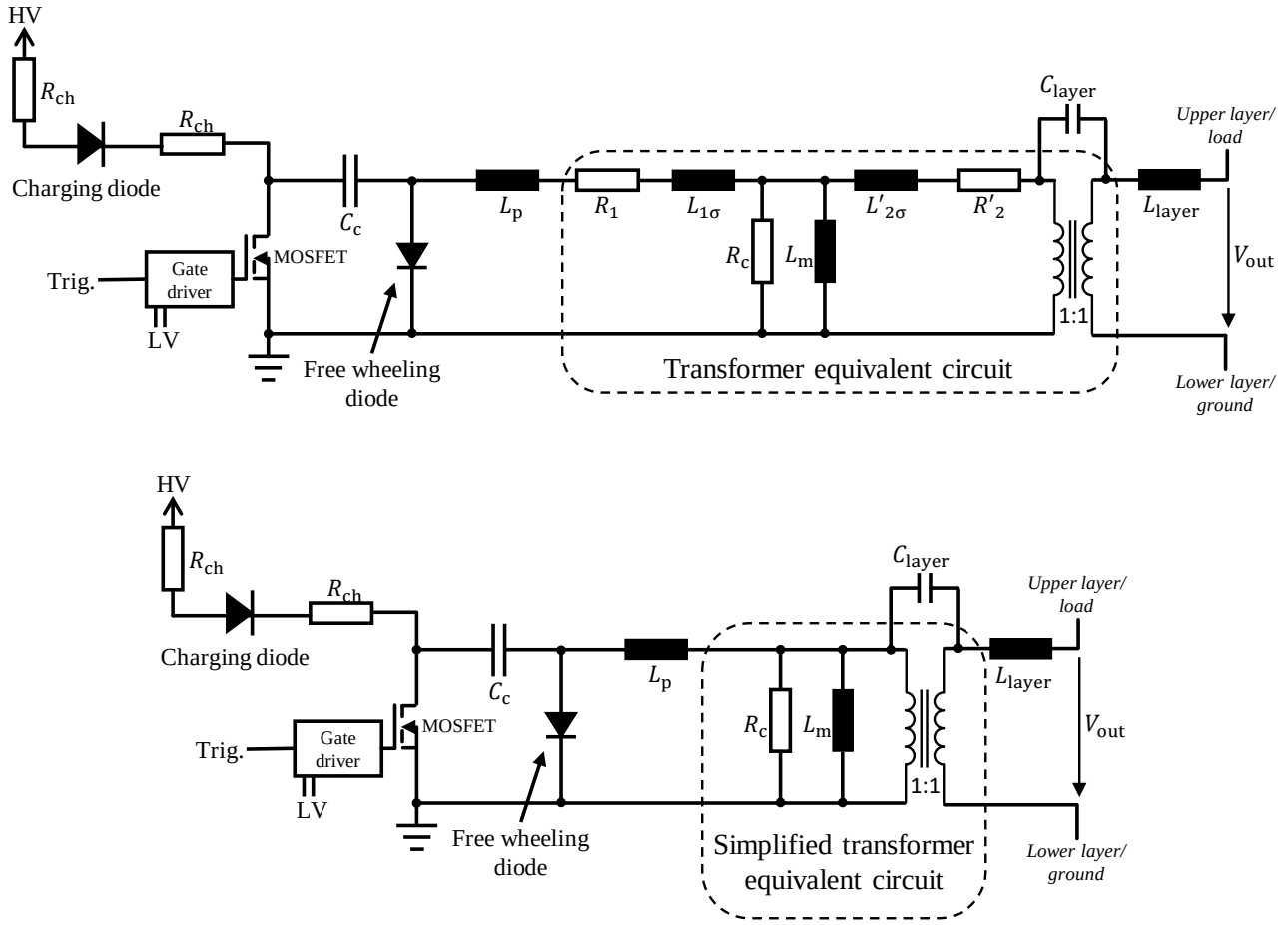

Figure 3.3: Simplification of the equivalent circuit of one layer. The transformer equivalent circuit in the upper schematic according to [16] can be reduced to simplify the equivalent circuit.

In Fig. 3.3 the pulse capacitor, charged by a high voltage power supply via charging resistors and a charging diode, is connected to the drain of the MOSFET. The MOSFET is grounded on the source side and driven by a gate driver which is connected to the trigger signal and a low voltage power supply. On the other side the capacitor is connected to the transformer, which is represented by a T-equivalent circuit according to [16]. On the primary side the free wheeling diode is connected in parallel to the transformer with the cathode at ground potential. L_p is representing the parasitic inductane of the primary circuit and is added between the capacitor and the transformer. On the secondary side of the transformer the secondary parasitic inductance of the stalk L_{layer} and the parasitic capacitance C_{layer} between the primary and secondary are added. The equivalent circuit of the transformer consits of the resistance and parasitic inductance of the primary winding, R_1 and $L_{1\sigma}$ respectively. The resistance and parasitic inductance of the secondary winding are

transformed to the primary side of the ideal 1:1 transformer in the equivalent circuit and represented by R'_2 and $L'_{2\sigma}$ respectively. The losses of the magnetic core are represented by the resistor R_c. L_m is the magnetizing inductance of the transformer.

Thanks to the high conductivity metal housing which encloses the magnetic core, as shown in Fig. 3.2, with only one turn, R_1 and $L_{1\sigma}$ can be neglected in the equivalent circuit since other parameters such as the primary inductance and the on-state resistance of the switch can be considered significantly larger. The secondary winding is also realised as a single turn and consists of a short conductor. Therefore the resistance R'_2 and the inductance $L'_{2\sigma}$ can be neglected as well. After the simplifications the transformer equivalent circuit only consits of the magnetizing inductance L_m, the resistor to represent core losses Rc and the ideal transformer, as shown in the lower schematic of Fig. 3.3. With the resulting equivalent circuit for one IA layer an IA stack can be constructed to calculate or simulate the behaviour of the device for design optimisation.

3.4 Design optimisation of the key components

Designing an IA is an iterative process which requires consideration of multiple parameters. A guideline of the design process is given in [55]. Some components of the IA influence the performance stronger than others. These key components are fundamental elements which should be chosen regarding the requirements. The key components are:

- Insulation material parameters between the stalk and the primary winding: dimension and dielectric material parameters.
- Transformer core: dimensions and magnetic material of the transformer core in each layer
- Semiconductor switch and gate driver in each branch of the primary circuits
- Pulse capacitor: energy storage in each branch of the primary winding

In the following, the key components and important factors influencing their design are further described.

3.4.1 Insulation

The central structure of the IA can be considered as a coaxial cable with an inner conductor (stalk), insulation/dielectric material and outer conductor (primary winding/core housing). As in a coaxial cable the characteristic impedance and the propagation time of the IA can be calculated. In the following the formulae for the characteristic impedance and the propagation time of a coaxial cable are derived. More detailed information can be found in references [15, 51, 106].

Like in a cylindrical capacitor, the electric field strength of the insulation in the IA occurs at the smallest radius of the insulation. The electric field in a cylindrical layout is [51]:

$$E(r) = \frac{V}{r \cdot \ln\left(\frac{r_o}{r_i}\right)}, \tag{3.1}$$

where $E(r)$ is the radial component of the electric field depending on the radial coordinate r, r_o the outer radius of the insulation (inner radius of the core housing), r_i the inner radius of the insulation (outer radius of the stalk) and V the voltage between the inner and outer conductors at r_i and r_o. The maximum electric field strength E_max in the insulation occurs at the innermost radius and can be calculated, if the variable r is set to r_i. The minimum required outer radius can be derived not to exceed E_max for a given r_i and voltage.

$$E_\mathrm{max} = \frac{V}{r_\mathrm{i} \cdot \ln\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right)} \rightarrow r_\mathrm{o} = r_\mathrm{i} \cdot e^{\frac{V}{E_\mathrm{max} \cdot r_\mathrm{i}}} \tag{3.2}$$

The capacitance of a cylindrical capacitor is

$$C = \frac{2\pi\varepsilon l}{\ln\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right)} \,, \tag{3.3}$$

where l is the length of the layer in the axial direction and $\varepsilon = \varepsilon_0 \cdot \varepsilon_\mathrm{r}$ the permittivity of the insulation material. With the known charge, the capacitance of one layer C_layer can be calculated.

$$C_\mathrm{layer} = \frac{Q}{V} = \frac{2\pi\varepsilon l}{\ln\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right)} \tag{3.4}$$

The inductance of one layer can be calculated from the equation:

$$L' \cdot C' = \mu \cdot \varepsilon \rightarrow L' = \frac{\mu\varepsilon}{C'} = \frac{\mu \ln\frac{r_\mathrm{o}}{r_\mathrm{i}}}{2\pi} \rightarrow L_\mathrm{layer} = \frac{\mu \cdot l \cdot \ln\frac{r_\mathrm{o}}{r_\mathrm{i}}}{2\pi} \,, \tag{3.5}$$

where L' and C' are the inductance and capacitance per unit length, respectively. Knowing the inductance and capacitance of an IA layer, the characteristic impedance of an IA layer Z_layer can be calculated. With some simplifications, presented by Zhang in [114], the characteristic impedance can be calculated:

$$Z_\mathrm{layer} = Z_\mathrm{IA} = \sqrt{\frac{L_\mathrm{layer} + L_\mathrm{p}}{C_\mathrm{layer}}} = \sqrt{\frac{L_\mathrm{p}}{2\pi\varepsilon l} \ln\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right) + \frac{\mu}{4\pi^2\varepsilon} \ln^2\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right)} \,, \tag{3.6}$$

where L_p is the inductance of the primary winding. The characteristic impedance of an IA layer is equivalent to the characteristic impedance of an IA that consists of multiple identical layers ($Z_\mathrm{layer} = Z_\mathrm{IA}$). The impedance should be matched with the impedance of the system the IA is operated in to avoid reflections. For a given inner insulation radius r_i and characteristic impedance the outer insulation radius r_o can be calculated by rearrangeing equation 3.6.

$$\rightarrow r_\mathrm{o}(r_\mathrm{i}) = r_\mathrm{i} \cdot e^{-\frac{L_\mathrm{p} \cdot \pi}{l\mu} + \sqrt{\left(\frac{L_\mathrm{p} \cdot \pi}{l\mu}\right)^2 + Z_\mathrm{layer}^2 \frac{4\pi^2\varepsilon}{\mu}}} \tag{3.7}$$

It can be seen that the formula presented by Zhang [114] is very similar to the formula for the characteristic impedance of a coaxial cable $Z_\mathrm{coax} = \sqrt{\frac{L'}{C'}}$, only the parasitic stray inductance of the primary circuit L_p is further increasing the pulse impedance of the inductive adder. The insulation gap between primary and secondary conductor δ is:

$$\delta = r_\mathrm{o} - r_\mathrm{i}. \tag{3.8}$$

The propagation time of an IA, as the system impedance, depends on the inductance and capacitance of the layers. To calculate the single way propagation time of one layer the same simplified equivalent circuit as for the system impedance can be used [114]. Hence:

$$t_\mathrm{prop,layer} = \sqrt{\left(L_\mathrm{p} + L_\mathrm{layer}\right) \cdot C_\mathrm{layer}} \,. \tag{3.9}$$

Compared with the propagation time of a coaxial cable $t_{\text{prop,coax}} = \sqrt{L_{\text{coax}} \cdot C_{\text{coax}}}$ it can be seen that the primary stray inductance L_{p} is added. The single way propagation time of the entire stack $t_{\text{prop,stack}}$ can be calculated by multiplying the single layer propagation time $t_{\text{prop,layer}}$ by the number of layers in the stack.

$$t_{\text{prop,stack}} = n_{\text{layer}} \cdot \sqrt{\left(L_{\text{p}} + L_{\text{layer}}\right) \cdot C_{\text{layer}}} \tag{3.10}$$

A pulse generated by the IA is generated simultaneously in all layers and adds up at the output. One layer generates a voltage pulse of half the charging voltage propagating in each direction of the IA. Generally the IA is operated with one end in short-circuit. In case of the layer closest to the output, half the pulse has to propagate through the stack towards the short-circuit end, is reflected, and propagates back to the output end. Therefore, the minimum rise time of the pulse at the output end of the IA is $2 \cdot t_{\text{prop,stack}}$. To minimize the propagation time the number of layers n_{layer}, the inductances L_{p} and L_{layer}, and the capacitance C_{layer} should be kept as small as possible. At the same time the required system impedance and output voltage have to be considered. For a given output current I_{out} of the IA, the required voltage scales linearly with the system impedance and hence the number of required layers n_{layer}, each of a given voltage V_{layer}, increases. The minimum number of required layers in an IA stack for a given characteristic impedance and output current can be calculated with:

$$n_{\text{layer}} = \frac{V_{\text{out}}}{V_{\text{layer}}} = \frac{I_{\text{out}} \cdot Z_{\text{IA}}}{V_{\text{layer}}} \tag{3.11}$$

With the equations presented above the electrical field stress, insulation gap size and propagation times of an IA with different characteristic impedance values for a given output current and layer voltage can be calculated.

Figure 3.4 shows in the upper graph the calculated hyperbolic curve of the layer propagation time $t_{\text{prop,layer}}$ together with the approximately linear curve of the stack propagation time $t_{\text{prop,stack}}$ of the IA. In the lower graph the limit of the electric field strength $E_{\text{limit}} = 0.4 \cdot E_{\text{max}}$ and insulation gap size δ versus the system impedance is shown. The limit of the electric field strength was chosen with 60 % of margin to stay comfortably below the breakdown field strength. The plots were calculated based on formulae 3.9, 3.10, 3.8 and 3.2 for a given layer voltage of 960 V, output current of 2.5 kA and layer height of 4 cm. As insulation material oil ($\varepsilon_{\text{r}} = 2.7$) was considered. A value of 5 nH was assumed for the primary inductance, per layer. The possible design points are impedance values that can be reached as fractions of $50\ \Omega$ like $50\ \Omega$, $25\ \Omega$, $16.67\ \Omega$, etc. The design points are emphasized in the graphs. For values of more than $15\ \Omega$ the relation between impedance and propagation time is approximately linear, for values below $15\ \Omega$ the fact that the number of layers can only be an integer influences the graph and leads to the effect that the propagation time is not increasing much until a system impedance of $10\ \Omega$ before the linear trend is becoming visible.

As already mentioned before, the insulation material between the primaries and secondary winding serves at the same time as dielectric material in the internal coaxial design of the IA. The structure of the IA can be considered as a coaxial cable with inner conductor (stalk), insulation/dielectric material and outer conductor (primary winding/core housing). Therefore the material properties of the insulation material influence the design dimensions and the impedance. The dimensions of the IA are limited in two directions: reducing the diameters increases the electrical field in the insulation material and for big diameters production limitations of the transformer core will be exceeded. The electric field strength should not exceed the maximum field strength of the insulation material at any point. Hence the required material should have a high electric strength and at the same time a low relative permittivity for good insulation and propagation time properties. The minimum stalk radius can be calculated when the electric field at the stalk is set to the maximum design value. For good reliability this value should be comfortably

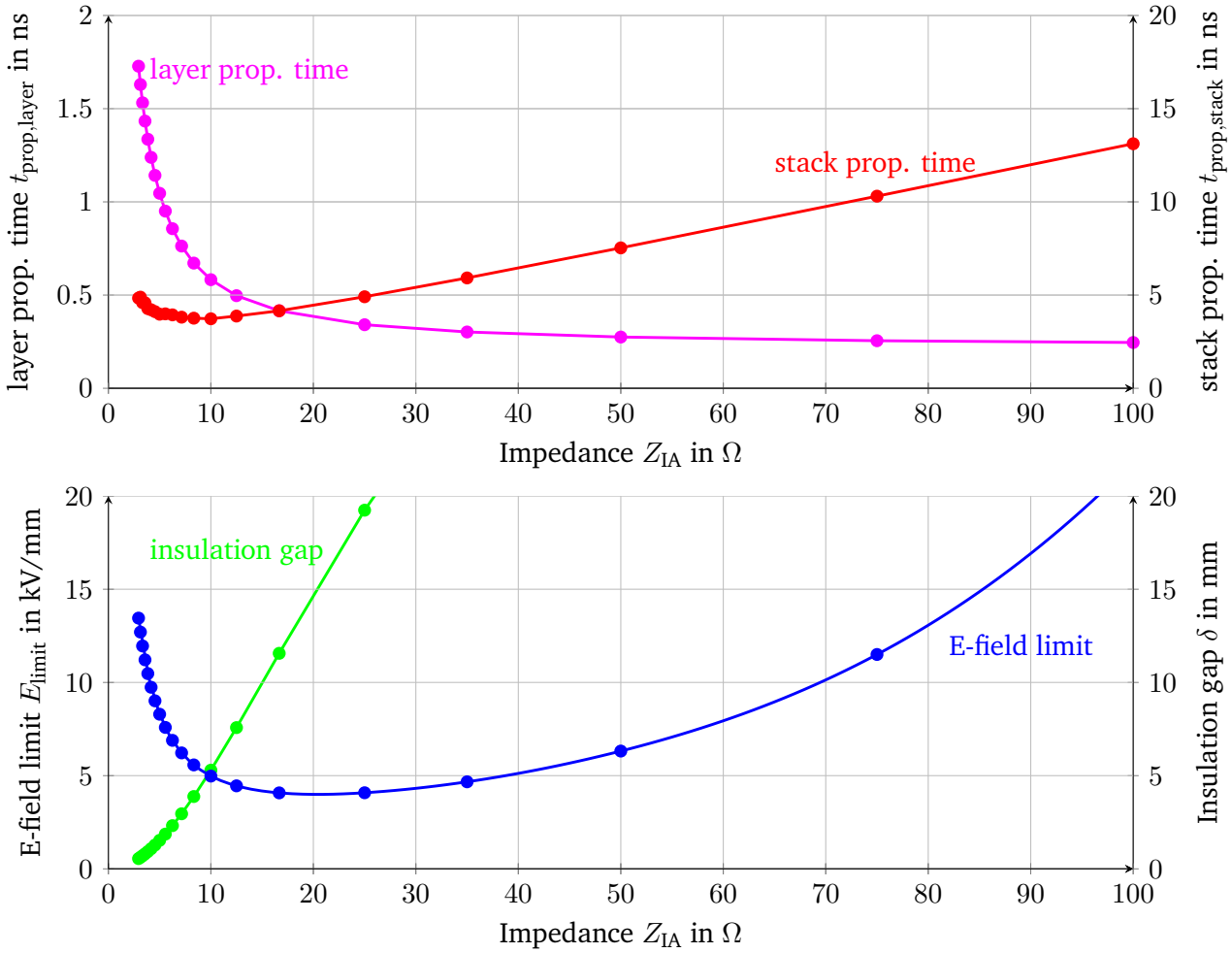

Figure 3.4: Calculated propagation time of the IA, maximum electric field and insulation gap size over system impedance for a given layer voltage and output current. The points mark design values for Z_{IA} which are rational fraction of $50\ \Omega$.

below the breakdown strength. Influencing factors are the insulation material, system impedance and primary inductance.

$$r_{\text{i,min}} = \frac{V_{\text{out}}}{E_{\text{ins,max}} \cdot \ln\left(\frac{r_{\text{o}}}{r_{\text{i}}}\right)} \tag{3.12}$$

With:

$$\ln\left(\frac{r_{\text{o}}}{r_{\text{i}}}\right) = -\frac{L_{\text{p}} \cdot \pi}{l\mu} + \sqrt{\left(\frac{L_{\text{p}} \cdot \pi}{l\mu}\right)^2 + Z_{\text{IA}}^2 \cdot \frac{4\pi^2 \varepsilon_0 \varepsilon_{\text{r}}}{\mu}} \tag{3.13}$$

Optimal insulation design: The optimum insulation would be dimensioned such that the maximum electric field is minimized. It can be calculated by finding the minimum value of the function $E_{\text{max}}\left(\frac{r_{\text{o}}}{r_{\text{i}}}\right)$, as shown in [51]. The minimum is reached if the ratio of inner to outer insulation radius is e:

$$\frac{r_{\text{o}}}{r_{\text{i}}} = e = 2.718 \tag{3.14}$$

If the ratio is chosen as e, the parameters to adapt the impedance of the IA reduce significantly since the radii ratio is the main method to adapt the impedance. Equation 3.15 shows the formula for the system impedance of an IA with $\frac{r_\mathrm{o}}{r_\mathrm{i}} = e$.

$$Z_\mathrm{IA}\left(\frac{r_\mathrm{o}}{r_\mathrm{i}} = e\right) = \sqrt{\frac{L_\mathrm{p}}{2\pi\varepsilon l}\ln\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right) + \frac{\mu}{4\pi^2\varepsilon}\ln^2\left(\frac{r_\mathrm{o}}{r_\mathrm{i}}\right)} = \sqrt{\frac{L_\mathrm{p}}{2\pi\varepsilon l} + \frac{\mu}{4\pi^2\varepsilon}} \tag{3.15}$$

It can be seen that the only remaining variables in equation 3.15 are the primary inductance L_p, the layer length l and the insulation parameters ε and μ. Considering a primary inductance of $L_\mathrm{p} = 5 - 20$ nH, layer length of $5 - 2$ cm and air as an insulation material, then a system impedances of $Z_\mathrm{IA} \approx 70 - 150\ \Omega$ can be realised. In case of oil with $\varepsilon_\mathrm{r} = 2.7$ as insulation material, a system impedances of $Z_\mathrm{IA} \approx 40 - 85\ \Omega$ can be reached. Hence for IAs with an impedance $\geq 40\ \Omega$ the design can be focused on the minimum electric stress in the insulation. However, for IAs with an impedance $< 40\ \Omega$ the design can not be realised with the ideal radii ratio. Any action to keep the radii ratio ideal such as increasing the layer height or choosing an insulation material with a very high permittivity brings up other disadvantages, for example an increased propagation time. During the design of an IA the best set of values needs to be chosen.

3.4.2 Transformer core

The transformer core of an inductive adder layer requires a design that matches the pulse requirements. Due to the saturation of the transformer core the maximum pulse length of the IA is limited which makes a careful design of the core essential. The required cross sectional area of the core is proportional to the voltage-time-integral of the pulse and the properties of the core material:

$$A_\mathrm{Fe} = \frac{\int V dt}{\Delta B}\ , \tag{3.16}$$

where A_Fe is the effective core cross section, V the layer voltage and ΔB the flux density swing of the magnetic core. The effective core cross section A_Fe is the actual cross section A_c multiplied by a fill factor $0 < \eta_\mathrm{Fe} < 1$ and describes the iron cross section in the core: $A_\mathrm{Fe} = \eta_\mathrm{Fe} \cdot A_\mathrm{c}$. Since the core is of toroidal shape, the magnetic path length on the inner diameter of the core is shorter than on the outer diameter of the core. The magnetic material is a cost intense part of the IA, hence the diameter ratio and core height should be chosen in such way that the volume of the core is reduced to minimize costs.

Figure 3.5 shows an example for a BH-characteristic of a magnetic material. The characteristics of the material should be chosen to fit the device requirements. High permeability material such as ferrite or iron is required for the core (steepness of the BH-curve). To reduce heating up of the material, the hysteresis losses should be low (area inside the BH-curve) as should the eddy current losses. Low losses and high permeabilities can be reached e.g. with tape wound nanocrystalline cores. However different materials and manufacturing techniques, depending on the manufacturer of the core, might be considered regarding core dimensions and insulation. The linear region of the core, marked in Fig. 3.5, should be sufficiently large for the pulse as described in formula 3.16. Besides the diameter also the core height needs to be chosen with care to fulfill the pulse requirements e.g. limit the height of the stack to achieve a fast rise time of the output pulse. Biasing of the core can be applied to reduce the required cross sectional area.

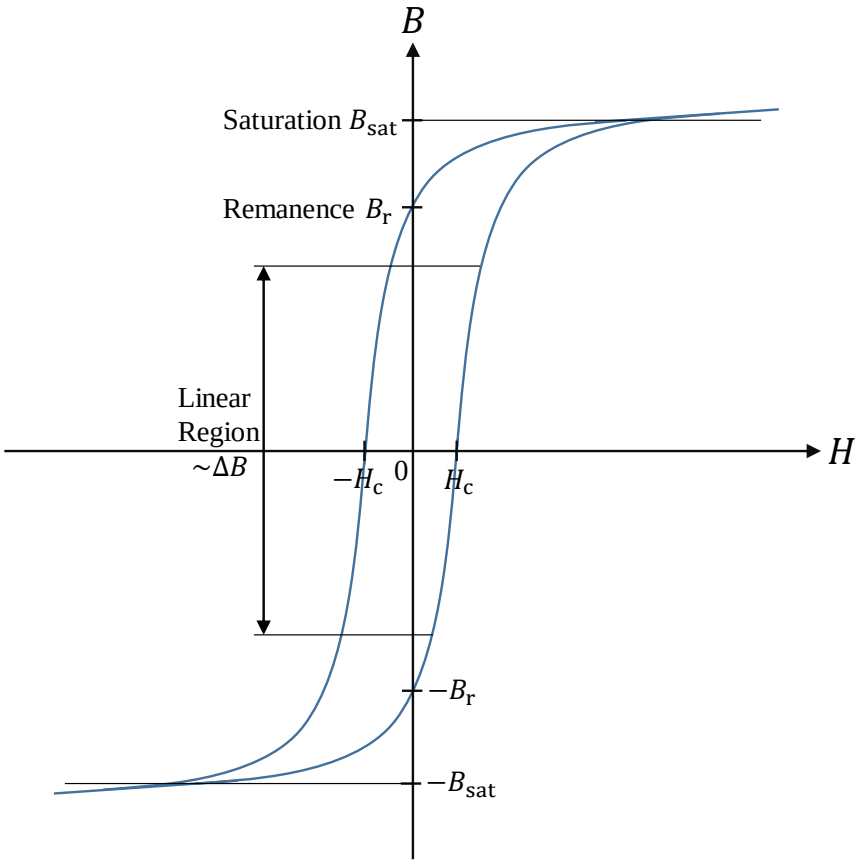

Figure 3.5: Example for a BH-characteristic of a magnetic material. Aimed working area should be the approximately linear region (marked).

Biasing of the transformer core

Fast rise time inductive adders require a short stack height to reduce the propagation delay through the stack. Important factors influencing the stack height are the required number of layers as well as the layer height, as described in section 3.4. The minimum layer height is mainly limited by the height of the capacitor and the height of the magnetic core. To reduce the required cross sectional area, and therefore the height of the magnetic core, a biasing circuit is beneficial. This circuit drives a current through the magnetic cores and sets the reference flux density to a negative value. In this way the available flux density swing (ΔB) can be increased.

Disadvantages of the biasing circuit include unwanted ripples introduced by the additional circuit through the stack. The bias circuit consists of a cable which is going through all magnetic cores in the stalk. A constant DC current is driven through the cable by a DC power supply. To protect the power supply from a transient over-voltage, an inductor (L_{bias}) is connected in series between the IA and the power supply. Since during the pulse the same output voltage is induced in the biasing cable as in the stalk, the cable needs to be sufficiently insulated. During the output pulse the current through the inductor increases and requires a free wheeling path once the pulse is switched off. This free wheeling path is provided by a diode in parallel to the power supply. The required inductor (L_{bias}) can be estimated from the pulse length Δt, output

voltage V_{out} and the maximum acceptable current increase ΔI, using:

$$L_{\text{bias}} = V_{\text{out}} \cdot \frac{\Delta t}{\Delta I} \tag{3.17}$$

Considering a 3 µs long pulse, 20 kV of output voltage and 1 A current increase, the required inductance is $L_{\text{bias}} = 60$ mH.

The fact that the magnetic flux induced by the biasing circuit in the magnetic material of the IA is opposing the induced flux of the pulse leads to the problem that both fluxes add up in the magnetic core of the series inductor of the biasing circuit. The inductor needs to be designed in such a way that it never saturates. A saturated biasing inductance would behave as a short-circuit in parallel to the load of the IA and would lead to a high current in the primaries, a fast discharge of the capacitor and probably destruction of the LV bias power supply. If the required biasing current is known, the remaining parameters to design the inductor for the biasing circuit are mainly defined by the magnetic material.

The formula for the inductance of a toroidal coil is $L_{\text{tor}} = \mu_0 \mu_{\text{r}} N^2 \frac{h_{\text{z}} \cdot \ln \frac{r_2}{r_1}}{2\pi}$, where N is the number of turns, h_{z} the height of the toroidal core, r_2 the outer radius and r_1 the inner radius [107]. The saturation magnetic field strength of the magnetic material must be higher than the total magnetic field strength, excited by the biasing current and the pulse current:

$$H_{\text{tot}} = H_{\text{bias}} + H_{\text{pulse}} = \frac{N \cdot I_{\text{bias}}}{l_{\text{m}}} + \frac{N \cdot I_{\text{pulse}}}{l_{\text{m}}} = \frac{N}{l_{\text{m}}} \cdot (I_{\text{bias}} + I_{\text{pulse}}) \tag{3.18}$$

where l_{m} is the magnetic path length of the toroidal core. With $I_{\text{pulse}} = \frac{V \cdot \Delta t \cdot 2\pi}{\mu_0 \mu_{\text{r}} \cdot N^2 h_{\text{z}} \cdot \ln \frac{r_2}{r_1}}$ the total magnetic field strength becomes

$$H_{\text{tot}} = \frac{N}{l_{\text{m}}} \cdot I_{\text{bias}} + \frac{V \cdot \Delta t \cdot 2\pi}{\mu_0 \mu_{\text{r}} \cdot l_{\text{m}} h_{\text{z}} N \cdot \ln \frac{r_2}{r_1}}. \tag{3.19}$$

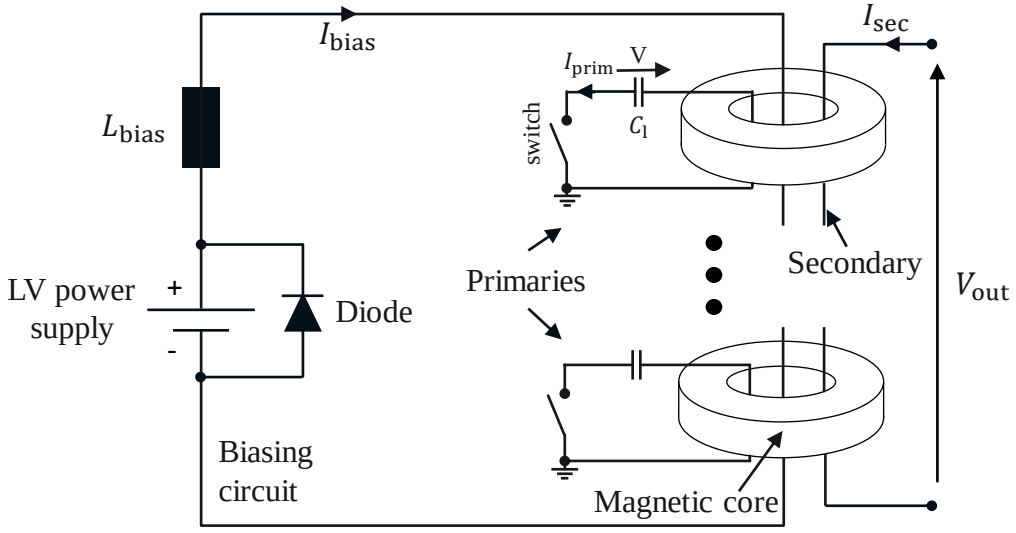

Figure 3.6: Schematic of the biasing circuit ($N = 1$)

For each material an optimum number of turns for the inductor exists to not saturate the core. For the FCC inductive adder prototype an inductor has been produced with a tape wound, nanocrystalline

magnetic core (material: VITROPERM 500F). The used core has a relative permeability of $\mu_\mathrm{r} \approx 50000$, a saturation magnetic field of 1.2 T and an effective cross sectional area of about $A_\mathrm{eff} = 2.5$ cm^2, which leads to an optimum number of turns N of about 25. Figure 3.4.2 shows a schematic of the biasing circuit.

After some tests with the manufactured inductor for the biasing circuit it turned out that the magnetic core was becoming nonlinear for higher output voltages $>\approx 8$ kV and that the change of permeability of the magnetic material introduced a ripple in the output pulse waveform of the IA. For this reasons a second inductor was manufactured without magnetic material. This air coil has the advantage of a constant inductance independent of the voltage-time integral, but requires a much higher number of turns to compensate for the low permeability ($\mu_\mathrm{r} = 1 \rightarrow N > 300$). A more detailed documentation of the design and construction of the air coil can be found in section A.3 of the appendix.

3.4.3 Primary circuit

The performance and capabilities of the IA are highly influenced by the primary circuit. Each layer of the IA has a primary circuit that can consist of one or several parallel branches. The main components of the primary circuit are pulse capacitor, semiconductor switch and free-wheeling diode. In addition there is a gate driver, charging circuit and high and low voltage power supplies. The circuit is mounted on a printed circuit board (PCB) and is connected to the core housing of each layer to form the primary winding of the transformer. The rated voltages of the pulse capacitor, semiconductor switch and diode have to withstand the operational voltage of the layer. Rise and fall times of the switch have to be fast enough for the system requirements. As described in section 3.4.1, the parasitic inductance of the primary circuit should be as small as possible. Therefore, for each branch the components on the PCB should be placed such that there is a low loop inductance. As analytically and numerically calculated in [57] the inductance of one branch of the primary circuit is several tens of nH, even if the circuit is designed for low inductance purpose. An effective way to further reduce the inductance is to connect several branches in parallel, as is also required for higher output current. In this way the primary inductance can be reduced to less than 10 nH [57]. The gate driver for the semiconductor switch needs to be designed with a sufficient rise time and current capability to drive the gate of the MOSFET. Charging resistors (R_ch in Fig. 3.7) and diodes are needed to charge the pulse capacitors from the power supply. The free wheeling diode protects the switch from over voltages by carrying the inductive magnetizing current after switch off and should be placed close to the core. In addition the free wheeling diodes of a layer conduct the load current if the MOSFETs of that layer fail to turn-on. Figure 3.7 shows the equivalent circuit of an IA layer.

Semiconductor Switch

The semiconductor switch in the primary circuit is the main switching device of the IA. It can be realized with different component types and materials depending on the switching requirements. Examples for different types are GTO, IGBTs and MOSFETs. During the last decade research, especially on MOSFETs, developed devices based on other materials than silicon (Si) to improve switching performance. Components with silicon carbide (SiC) or gallium nitride (GaN) are available on the market with significantly shorter switching times. The voltage and current rating need to be chosen carefully to avoid operating the device outside the specs. Using the devices with a certain margin ($\sim 50 - 80$ %) of the maximum ratings is advisable. Furthermore the gate driver should be matched to the device requirements.

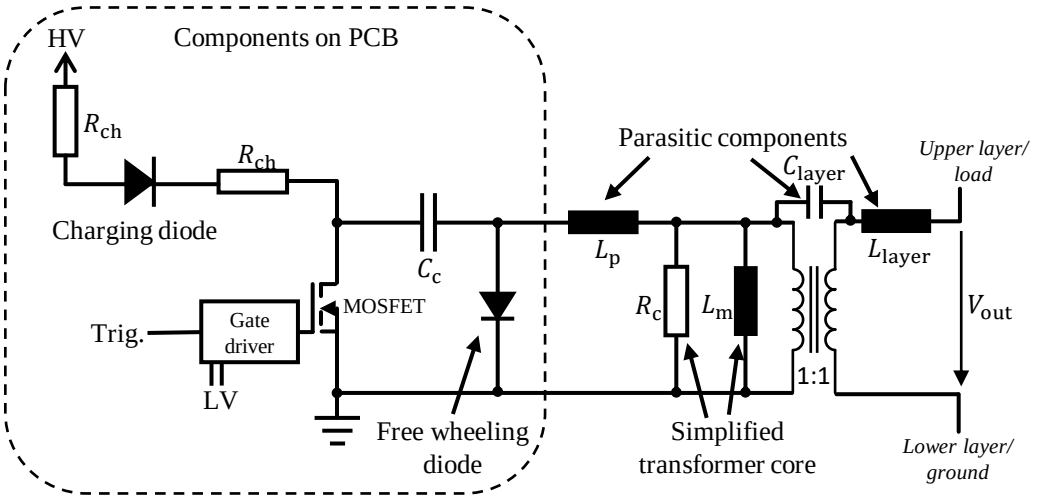

Figure 3.7: Equivalent circuit of an IA layer

Pulse capacitor

The pulse capacitor characteristics can influence the pulse shape of the inductive adder and needs to be chosen carefully. The droop and rise time of the pulse are influenced by the capacitance and the parasitic inductance of the capacitor, respectively. Also the package dimensions of the capacitor must be within the required dimension specification of one layer/branch. To obtain a small layer height also the package height of the capacitors needs to be small. Unless modulation is used (see section 3.5), the required capacitance of the layer C_l is the sum of all branch capacitances C_b of one layer and can be calculated with:

$$C_\mathrm{l} = C_\mathrm{b} \cdot n_\mathrm{branch} = \frac{\Delta t \cdot I_\mathrm{c,l}}{\Delta U} = \frac{\Delta t \cdot n_\mathrm{branch} \cdot I_\mathrm{c,b}}{\Delta V} \,, \tag{3.20}$$

where n_branch is the number of parallel branches per layer, $I_\mathrm{c,l}$ is the current of one layer, $I_\mathrm{c,b}$ is the current of one branch, Δt is the time for which the pulse current is flowing and ΔV is the acceptable voltage drop per layer during Δt. The current and voltage ratings of the capacitor are dependent on the current and voltage ratings of one branch and should be designed including a margin. A large fraction of the parasitic inductance of the primary circuit is introduced by the inductance of the pulse capacitor [57]. Therefore capacitors with a low inductance should be selected. Also the return path of the primary circuit contributes to the total parasitic inductance, making also circuit layout an important factor.

3.5 Modulation layer

The so called modulation layers can be added in the stack to modulate the output pulse. Modulation means that the pulse shape is manipulated into a desired form, within a certain range, as it is described in more detail by various authors in [28, 48, 55, 59]. The modulation techniques can be distinguished by digital and analogue modulation. Digital modulation describes the turning on or off of a single or several constant voltage layers in the stack during the pulse. In this way the charging voltage of the layers is added or removed to the output pulse and a stepped flat-top can be generated. This approach can be used to compensate the droop of a pulse. Passive analogue modulation describes a layer in the adder stack

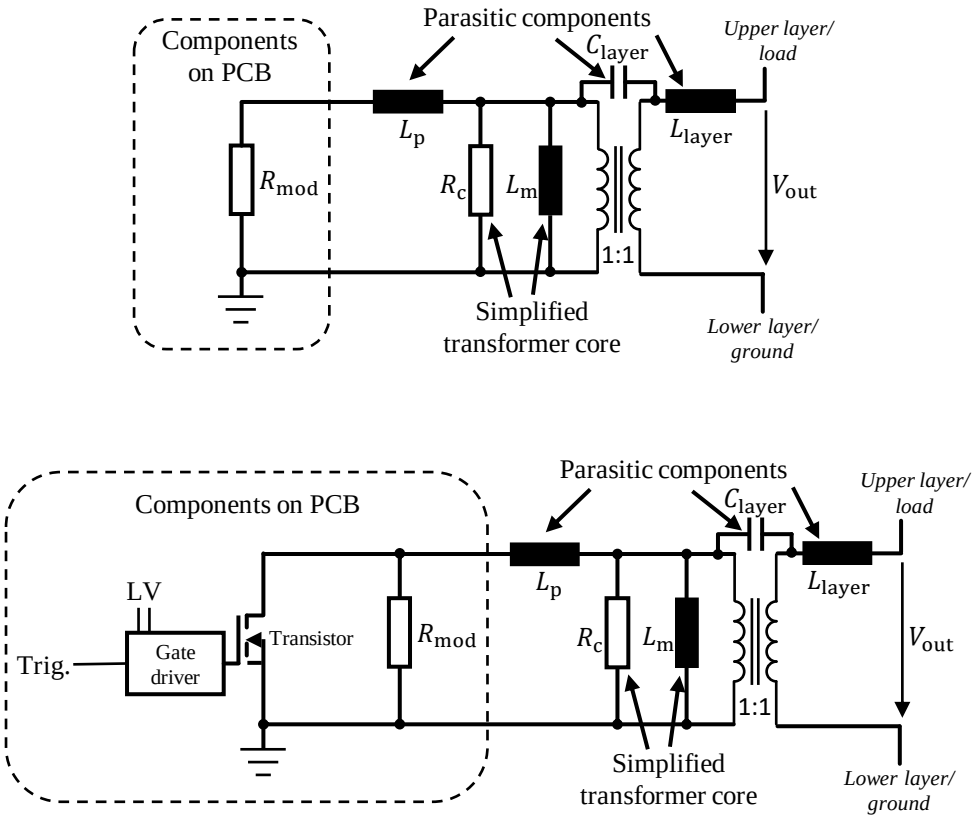

Figure 3.8: Equivalent circuit of a passive (top) and an active (bottom) analogue modulation layer

with only a resistor in the primary circuit. Effectively the resistor is parallel connected to the magnetizing inductance of the transformer core. This RL circuit causes an inverse decaying voltage in series with the pulse generated by the constant voltage layers, which results in a compensation of the droop over the connected load. This passive modulating circuit can be made more flexible by adding an RF transistor in parallel to the resistor. By controlling the gate of the transistor the current through the resistor and therefore the voltage drop can be modulated. In this way the modulation of the output voltage can be actively controlled. Therefore this modulation technique is called active analogue modulation. Figure 3.8 shows the equivalent circuit of an active and passive analogue modulation layer. The different modulation technologies are powerful tools to optimize the pulse output waveform. As reported in [59] pulse flat-top stabilities of up to ± 0.02 % can be reached. Since technology of modulation layers is described in detail by various authors ([28, 48, 55, 59]) and is not one of the main challenges of the FCC injection requirements it will not be discussed in detail. The special case of using modulation layers together with a biasing circuit has not been documented in the literature, even if it was applied by Gower in [48] and is thus discussed further here.

Modulation layers and core biasing: In case of an IA with biasing circuit the modulation layers require the biasing current in the opposite direction through the magnetic core than the constant voltage layers. In case of the modulation layer the stalk can be considered as the primary winding of the transformer and the core housing as the secondary winding. The flux induced by the current of the biasing cirucit needs to oppose the flux induced by the current flowing through the stalk to set the saturation point

of the magnetic core in the third quadrant of the BH-curve. Therefore the biasing circuit needs to go through the modulation layers in the opposite direction than it goes through the constant voltage layers. In other words: In the constant voltage layers the biasing current direction through the magnetic core needs to be the same as the current through the stalk and therefore opposite to the current direction through the core housing. In the modulation layers the biasing current direction through the core needs to be opposite to the current through the stalk and therefore the same as the current direction through the core housing. Figure 3.9 shows a schematic of the biasing circuit in an IA with modulation layer. In contrary to the constant voltage layers where the inductance of the core should be kept high to reduce the magnetising current, in analogue modulation layers a low inductance has advantages. Therefore linear shaped BH-curves should be used in analogue modulation layers. If the BH-characteristics of the cores used in the constant voltage layers and the cores used in the modulation layers are different and a higher current value is used to reset the cores of the modulation layers the number of windings of the biasing circuit through the cores of the modulation layers can be increased. In this way a stronger biasing of the modulation layer cores can be achieved without changing the biasing current in the cores of the constant voltage layers.

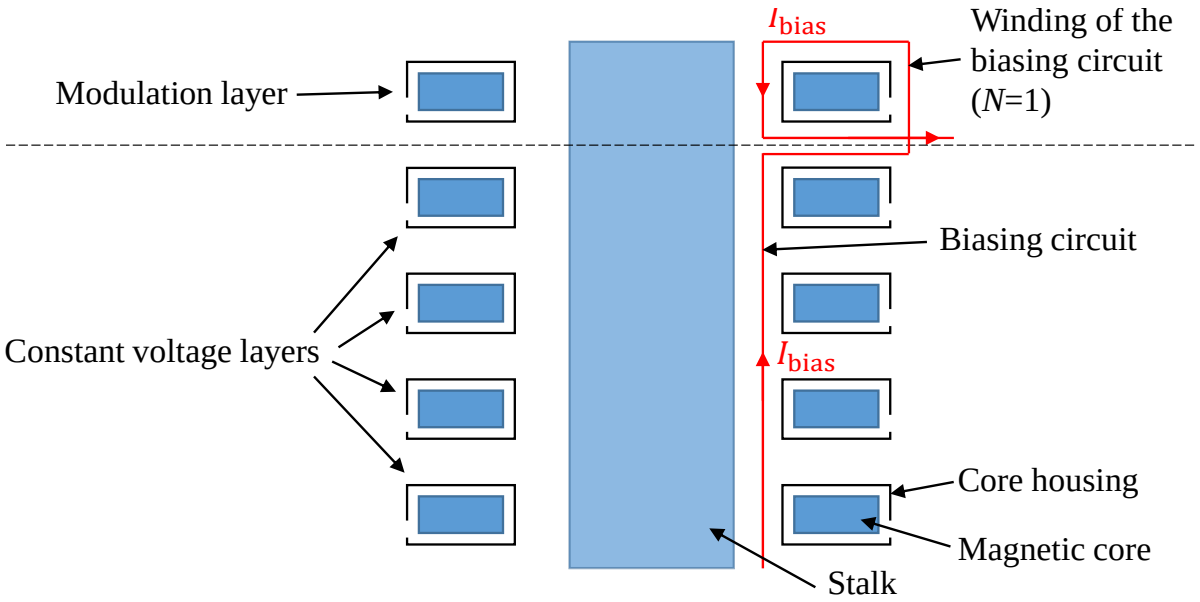

Figure 3.9: Biasing circuit location in case of an IA with modulation layer. For a higher biasing effect in the modulation layer core $N > 1$ can be chosen.

4 Design of the FCC inductive adder

This chapter presents the requirements for the FCC injection kicker system and the design steps for an inductive adder (IA) pulse generator.

4.1 System requirements

The requirements for the FCC injection system are defined by the injection beam parameters, including its energy, and the kicker magnet. The LHC at 3.3 TeV is the baseline for the high energy booster (HEB) to inject into the FCC. Therefore the design of the FCC-hh injection system is based on the HEB parameters. Other injector options were studied and can be found in [13, 98]. Table 4.1 shows the parameters for the FCC-hh at 3.3 TeV injection energy.

Table 4.1: FCC injection parameters with LHC as HEB at 3.3 TeV

Parameter	Unit	Value
Kinetic energy	TeV	3.3
Available system length	m	120
Deflection angle	mrad	0.18
Field rise/fall time definition	%	0.5-99.5
Field rise/fall time	ns	430
Field flat-top duration	µs	2.0
Field flat-top ripple	%	±0.5
Repetition rate	Hz	10

Based on the parameters of Tab. 4.1 the kicker magnet system was designed and the requirements for the injection kicker pulse generator were specified. The initial magnet design is presented by Chmielinska in [31]. The chosen system impedance, 6.25 Ω, was a trade off between the kicker magnet system, that requires a relatively short length, and thus a low characteristic impedance, in order to present minimum beam coupling impedance, and the IA to satisfy the field rise time requirement. The 430 ns of field rise time were divided into 75 ns for each pulse generator and 355 ns for each kicker magnet. The total injection system will consist of 18 kicker systems per beam [29, 30, 111]. As a worst case it is assumed that the generator rise time and the magnet fill time add up linearly to the field rise time. The required current for the kicker magnet is 2.4 kA, which results in a required IA output voltage of 15 kV for an impedance of 6.25 Ω. Tab. 4.2 shows the requirements for each injection kicker pulse generator.

The required output current of 2.4 kA is approximately six times higher than the highest output current for a MOSFET based inductive adder pulse generator found in the literature, as shown in Tab. 3.1 of chapter 3.2. The low system impedance in combination with the fast rise time is challenging, and such a combination of

Table 4.2: FCC injection kicker parameters with LHC as HEB

Parameter	Unit	Value
System impedance	Ω	6.25
Output current	kA	2.4
Output voltage	kV	15
Field pulse length	μs	2.0
Field rise/fall time definition	%	0.5-99.5
Field rise/fall time	ns	430
Field flat-top ripple	%	±0.5
Generator pulse length	μs	2.4
Repetition rate	Hz	10

these requirements have not been reported in the literature. The pulse duration of 2.4 μs is more than 2.5 times larger than the longest reported pulse length in literature for IAs with MOSFETs as switches. With IGBT switches, pulse length of up to 10 μs have been reported [43, 81].

4.2 Design choices for the prototype

A prototype IA has been designed according to the requirements presented in Tab. 4.1. The system impedance of the injection kicker system is a compromise between its two main components: kicker magnet and pulse generator. For the baseline FCC injection at 3.3 TeV, the deflection angle is 0.18 mrad; in order to reduce the installed length of kicker magnets from 120 m to 40 m [31], a current of at least 2.4 kA is required. The LHC-like transmission line magnets, which are planned to be used for the FCC, require a low impedance of less than 10 Ω to reduce the required voltage to an acceptable level for the IA. An advantage of a lower voltage is that it is easier to insulate than higher voltages. Additionally the pulse should be transmitted with standard 50 Ω cables: this reduces the possible impedance to integrer fractions of 50 Ω. However, a low impedance makes the IA insulation design more complicated due to the decreasing insulation gap. At the same time the rise time per layer increase with lower impedance as shown in Fig. 3.4 of chapter 3.4.1. A higher system impedance (> 30 Ω) requires a higher output voltage to generate the same current, resulting in many layers and therefore long pulse rise times. As a compromise an impedance of 6.25 Ω was chosen which makes it presumably feasible for both kicker magnet and IA, to realise the required parameters. The required pulse current of the system is 2.4 kA resulting in a output voltage of 15 kV. As a next step for the IA design, the voltage per layer should be defined. The voltage per IA layer should be as high as possible but is limited by the maximum voltage of the semiconductor switches, the capacitor and the voltage-time integral of the magnetic core. It is desireable not to connect semiconductor switches in series in order to avoid more complicated gate drivers. SiC MOSFETs were chosen as the switching devices (see section 6.2). The fast rise time and low on-state resistance of SiC MOSFETs are beneficial for the envisaged performance. Even though SiC technology is rather new there are commercially available MOSFETs of 1.2 and 1.7 kV on the market with suitable device characteristics [36, 37, 87, 97]. Comparable IGBT or MOSFET devices based on Si-technology would have longer rise times and/or higher on state resistance. Further developments of SiC devices can be expected in the near future. Considering the more economical and higher current rated 1.2 kV SiC-MOSFETs the operating voltage of one layer, after a derating to 80 %, would be 960 V. To generate an output voltage of 15 kV, a minimum of 16 constant voltage layers is required. The current capability of

1.2 kV SiC MOSFETs on the market is about 200 A [36, 37, 87, 97]. For redundancy reasons a derating to about 60 % of the rated value is envisaged. Besides the load current the MOSFETs will also carry the magnetising current of the magnetic cores which is considered to be negligible compared to the load current, provided that the cores do not saturate. 24 parallel branches were chosen, which is the maximum number of branches which will fit around the circumference of one core housing of OD 374 mm: this corresponds to a core OD of 285 mm. A high number of parallel branches reduces the current stress on a single branch. At the same time it also reduces the total parasitic inductance L_p of each primary layer, which is advantageous.

4.2.1 Insulation design

The minimum dimensions of the inside radius of the core housing r_o, the outside radius of the stalk r_i and hence the insulation thickness $\delta = r_\mathrm{o} - r_\mathrm{i}$ depends on the electric field strength limit in the insulation material, as described in section 3.4.1. The maximum accepted electric field strength of the insulation material should not be exceeded, therefore the limit is defined with a margin of 60 % ($E_\mathrm{limit} = 0.4 \cdot E_\mathrm{max}$). In equations 3.2 and 3.6 of chapter 3.4.1 the influence of the maximum electric field strength E_max and the dimensions of the insulation are shown. Equation 3.6 of section 3.4.1 shows that the ratio of the outer and inner insulation diameter ($\frac{d_\mathrm{o}}{d_\mathrm{i}} = \frac{2 \cdot r_\mathrm{o}}{2 \cdot r_\mathrm{i}}$) remains constant for a given system impedance. Figure 4.1 shows the dependency of the outer insulation diameter d_o upon the inner insulation diameter d_i for a given specific permittivity of $\varepsilon_\mathrm{r} = 2.7$ and primary inductance of $L_\mathrm{p} = 5$ nH. An IA with a defined system impedance corresponds to a linear rising line in Fig. 4.1. The electric field strength limit shows the outer diameter at which the maximum electric field limit (see above) of the insulation is not exceeded, for a given inner diameter. The limit is defined as 1 kV/mm in case of air and 10 kV/mm in case of oil, which are approx. 40 % of the theoretical breakdown field strengths. The resulting hyperbolic function marks the border between a possible insulation (above the graph) and too weak insulation (below the graph). To build an IA of a certain impedance, the minimum possible diameter ratio is the intersection point of the E_limit graph and the line corresponding to the impedance. Figure 4.1 shows in the upper graph the design limits for an IA with air as insulation material ($\varepsilon_\mathrm{r} = 1$) and in the lower graph with oil as insulation material ($\varepsilon_\mathrm{r} = 2.7$). Based on simulations presented by Holma in [57], the primary inductance per layer was estimated to be 5 nH. To compare the plots the scaling of the axes should be considered. The minimum required inner insulation diameter for an air insulated IA would be approximately 1.8 m. Magnetic cores with such large diameters are complicated to manufacture and would make the IA heavy and costly. Using oil as insulation material reduces the minimum required inner insulation diameter to about 7 cm. However, the resulting insulation gap between core housing and stalk is in the range of 1 mm. By increasing the outer insulation diameter to 108 mm the insulation gap can be increased to 2.3 mm: in addition the maximum electric field strength is reduced. Another reason to chose 108 mm is that the CLIC damping ring IA built at CERN and described in [55, 59] has this dimension, too. Having two devices with the same dimensions in the lab makes re-use of parts such as magnetic cores feasable. The 6.25 Ω prototype IA will be built with a stalk diameter (inner diameter of the insulation) of $d_\mathrm{i} = 103.4$ mm, an inner diameter of the primary winding (outer diameter of the insulation) of $d_\mathrm{o} = 108$ mm and an layer height of $h = 40$ mm. The insulation material will be oil with a relative permittivity of $\varepsilon_\mathrm{r} = \sim 2.7$ and a relative permeability of $\mu_\mathrm{r} = 1$. Therefore the secondary stray inductance of one layer is $L_\mathrm{layer} = \frac{\mu_0 \mu_\mathrm{r} \cdot l}{2\pi} \cdot \ln \frac{d_\mathrm{o}}{d_\mathrm{i}} = 348$ pH and the secondary stray capacitance of one layer is $C_\mathrm{layer} = \frac{2\pi\varepsilon_0\varepsilon_\mathrm{r} \cdot l}{\ln \frac{d_\mathrm{o}}{d_\mathrm{i}}} = 138$ pF.

As described in section 4.2.3, the use of modulation layers is necessary to reduce the required capacitance per layer. A result of the voltage drop over the modulation layers is the need for additional constant

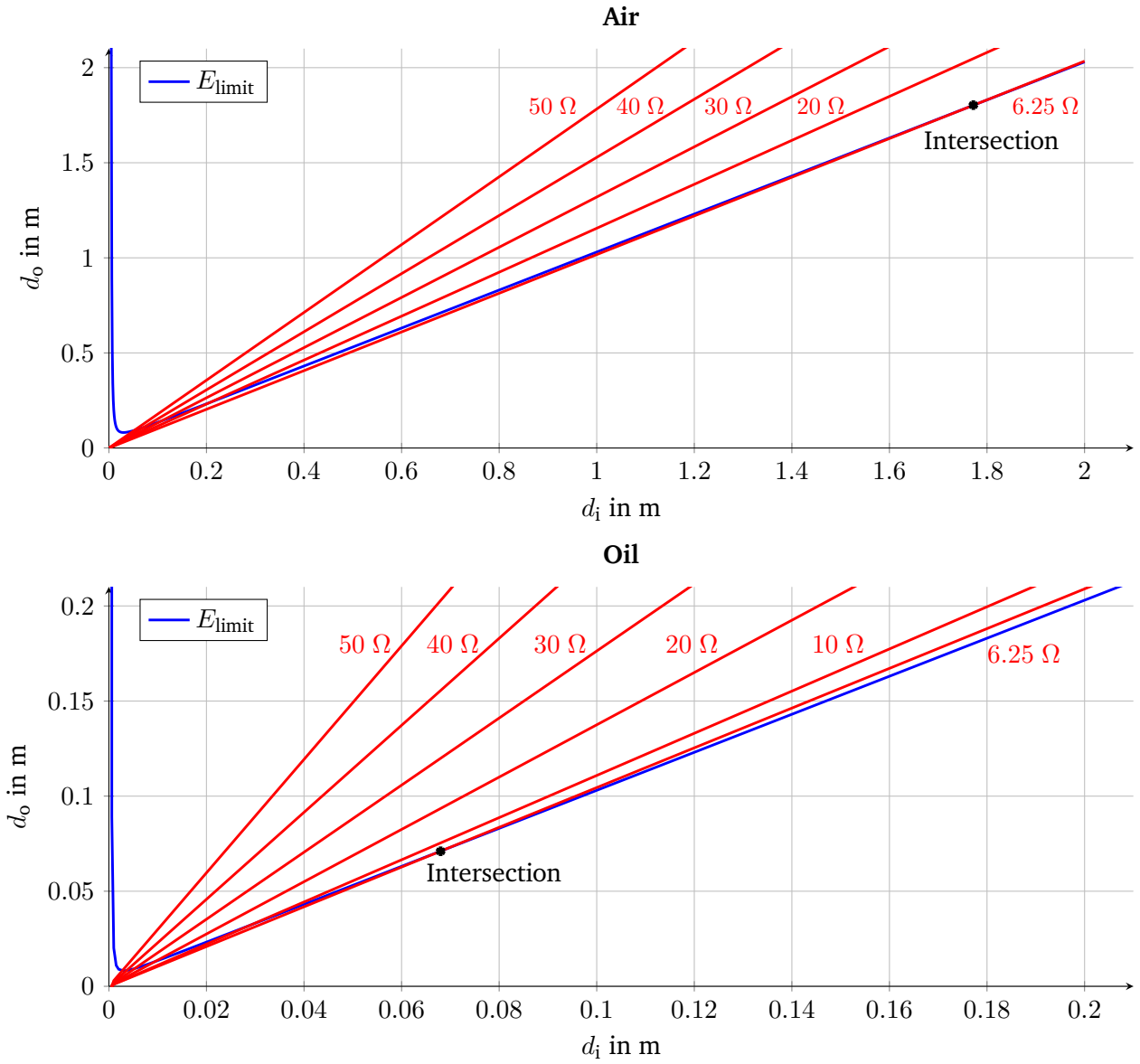

Figure 4.1: Calculated design limits for air (top, $\varepsilon_{\text{r}} = 1$) and oil (bottom, $\varepsilon_{\text{r}} = 2.7$) insulation with $E_{\text{limit}} = 1\ \frac{\text{kV}}{\text{mm}}$ for air and $E_{\text{limit}} = 10\ \frac{\text{kV}}{\text{mm}}$ for oil according to equation 3.2 and 3.6 of chapter 3.4.1 with $L_{\text{p}} = 5$ nH, $\mu_{\text{r}} = 1$ and $l = 40$ mm.

voltage layers in the IA stack to reach the desired output voltage. Depending on the position of the modulation layers in the IA stack, the voltage of the stalk can become higher than the output voltage of the IA. If all constant voltage layers are located at the top end (voltage output end) of the stack, the stalk potential would become higher than the output voltage and, hence, will increase the electric field stress of the insulation. This issue can be avoided by moving the modulation layers to the lower end (short-circuit end) of the IA stack or distributing them equally along the IA stack between the constant voltage layers. Since the modulation layers have a different characteristic impedance than the constant voltage layers, the position of the modulation layers in the stack can also influence the ripple of the pulse flat-top.

4.2.2 Magnetic core design

From the pulse requirements the properties of the magnetic core can be calculated. The required magnetic cross sectional area depends on the voltage-time integral of the pulse;

$$\int V_{\text{layer}} \mathrm{d}t = A_{\text{Fe}} \cdot \Delta B \rightarrow A_{\text{Fe}} = \frac{(t_{\text{pulse}} + (t_{\text{rise}} + t_{\text{fall}})/2) \cdot V_{\text{layer}}}{\Delta B_{\text{c}}}, \tag{4.1}$$

where A_{Fe} is the effective core cross-sectional area, t_{pulse} the pulse flat-top duration, V_{layer} the voltage of one IA layer and ΔB_{c} the magnetic flux density swing of the core,the rise t_{rise} and fall t_{fall} time are approximated to increase linearly. To avoid saturation of the core a margin should be added to the core cross-sectional area, which is considered with the factor $(1 + \alpha_{\text{m}})$, where $0 < \alpha_{\text{m}} < 1$. Finally the equation for the magnetic cross-sectional area becomes:

$$A_{\text{Fe}} = \frac{(t_{\text{pulse}} + (t_{\text{rise}} + t_{\text{fall}})/2) \cdot U_{\text{layer}}}{\Delta B_{\text{c}}} \cdot (1 + \alpha_{\text{m}}). \tag{4.2}$$

A manufacturing fill factor η_{Fe} is defined to allow for the fraction of the cross section required for insulation between the tapes of magnetic material. The core's actual cross sectional area can be calculated with $A_{\text{c}} = \frac{A_{\text{Fe}}}{\eta_{\text{Fe}}}$.

With a field flat-top length of 2 µs and a field rise time of 430 ns the flat-top length of the pulse generator will be ~ 2.43 µs. The layer voltage is considered to be 960 V and the magnetic flux density swing of the used material is $\Delta B = 2.2$ T. If a margin for the core of approximately $\alpha_{\text{m}} = 40$ % is considered, the magnetic cross sectional area is $A_{\text{Fe}} = 14.85$ cm^2. With a fill factor of $\eta_{\text{Fe}} = 75$ % the actual cross sectional area is $A_{\text{c}} = 19.79$ cm^2 ≈ 20 cm^2. The flux density swing of 2.2 T can only be achieved if the core is biased close to saturation in the 3^{rd} quadrant of the BH-curve (Fig. 3.4.2). The design of the biasing circuit is described in chapter 3.4.2. Without the biasing circuit the required magnetic cross section would be approximately twice as large, which would increase the costs significantly and could increase the height, and thus propagation delay, of the stack. For the prototype IA nanocrystalline tape wound cores with a cross sectional area of $A_{\text{c}} \approx 20$ cm^2 and a fill factor of $\eta_{\text{Fe}} = 75$ % will be used. A high saturation flux density is envisaged and the BH-curve, for the constant voltage layers, will be square shaped to allow to reset the magnetic core with a relatively low biasing current. The dimensions of the magnetic cores for the modulation layers are identical to those of the constant voltage layers. However, the BH-characteritic for the modulation layer cores should be linear, with a much lower permeability, as described in section 4.2.3.

4.2.3 Capacitor design

The pulse capacitors of the inductive adder are distributed among all branches of a layer. The capacitor slightly discharges during the pulse and this contributes to the droop of the output pulse. The required capacitance per layer C_{l}, to achieve the required pulse flatness without any other compensation method, can be estimated with

$$C_{\text{l}} = \frac{\Delta t \cdot I_{\text{layer}}}{\Delta V}, \tag{4.3}$$

where Δt is the pulse flat-top duration, I_{layer} the total current per layer and ΔV the acceptable voltage droop during Δt. For the FCC injection requirements, a layer capacitance of $C_{\text{l}} = \frac{2.4\ \mu\text{s} \cdot 2.4\ \text{kA}}{0.005 \cdot 960\ \text{V}} = 1.2$ mF would be required. Using 24 parallel branches, each branch would need a capacitor of 50 µF. For ΔV

a value of $0.5\ \% \cdot 960\ \text{V} = 0.005 \cdot 960\ \text{V}$, referred to one layer, was chosen even if a droop of $1\ \%$ from $+0.5\ \%$ to $-0.5\ \%$ would be acceptable: this gives a margin for ripple. Capacitors with a capacitance of $50\ \mu\text{F}$ with a rated voltage of at least 1.2 kV would be unacceptably large, would increase the layer height and would be too expensive. With passive analogue modulation layers, as described in chapter 3.5, the droop can be compensated and the required layer capacitance can be reduced. The magnetic core in the modulation layers is initially chosen to be the same core as for the constant voltage layers with a cross sectional area of about $20\ \text{cm}^2$ and a fill factor of $75\ \%$. The effective cross sectional area is therefore $A_{\text{Fe}} = 20\ \text{cm}^2 \cdot 75\ \% = 15\ \text{cm}^2$. As for the constant voltage layers, saturation of the core must be avoided: $A_{\text{Fe}} > \frac{\Delta t \cdot V_{\text{mod}}}{\Delta B}$. The voltage of a single modulation layer is therefore limited to $V_{\text{mod}} = \frac{A_{\text{Fe}} \cdot \Delta B}{\Delta t} = 1375\ \text{V}$. With the current being equal to the output current of 2.4 kA the modulation resistor can have a maximum value of $R_{\text{mod}} = \frac{V_{\text{mod}}}{I_{\text{out}}} = 0.573\ \Omega$. Adding three modulation layers of $0.45\ \Omega$ causes a voltage drop of the output voltage by $3 \cdot 0.45\ \Omega \cdot 2.4\ \text{kA} = 3240\ \text{V}$. With three constant voltage layers can compensate the voltage drop caused by the modulation layers. To estimate the droop that is compensated by the modulation layers, the inductance of the magnetic core is of importance. Contrary to the constant voltage layers, a lower inductance is advantageous for the modulation layer as a larger droop can be compensated for. The required inductance for the modulation layer can be estimated by $L_{\text{mod}} = \frac{V_{\text{mod}} \cdot \Delta t}{\Delta I_{\text{m}}}$. The inductance of the core can be decreased by adding an air gap in the core, by specifying a flat (linear) BH-curve, by using a core with smaller E_{sat} or appropriately biasing the core in the 1^{st} quadrant. If an inductance of $40\ \mu\text{H}$ is considered, as it was measured for magnetic cores with linear BH-characteristics in chapter 6, the droop compensated by one layer is $\Delta V_{\text{Rmod}} = \frac{R_{\text{mod}}^2 \cdot I_{\text{out}} \cdot \Delta t}{L_{\text{mod}}} = 29\ \text{V}$ for $R_{\text{mod}} = 0.45\ \Omega$. If this voltage drop is considered, for each of the three modulation layers, for the calculation of the required capacitance per layer:

$$C_{\text{l}} = \frac{\Delta t \cdot I_{\text{out}}}{\Delta V + 3 \cdot \Delta V_{\text{Rmod}} / N_{\text{CVlayer}}} = 612.5\ \mu\text{F}. \tag{4.4}$$

The resulting capacitance per branch is therefore $C_{\text{b}} = 612.5\ \mu\text{F}/24 = 25.5\ \mu\text{F}$. The required capacitance depends on the voltage droop compensated by the modulation layers and therefore on the effective permeability of the magnetic core in the modulation layers. The capacitor of one branch of the prototype will have a nominal value of $25\ \mu\text{F}$.

Table 4.3 shows the design parameters of the IA prototype for the FCC injection kicker system. Although the FCC prototype IA uses 3 modulation layers, each with a resistance of $0.45\ \Omega$, this was chosen to be compatible with the available magnetic cores ($L_{\text{m}} = 40\ \mu\text{H}$). However, these three layers require that an extra 3-4 constant voltage layers are used to compensate for the voltage drop across the modulation layers: in addition, these extra layers increase the output pulse rise time. Hence, it is suggested that in the future cores with lower magnetizing inductance are investigated for the modulation layers. As an example, a modulation layer core with $L_{\text{mod}} = 1\ \mu\text{H}$, would permit a modulation resistor of only $0.25\ \Omega$ to be used: this would reduce the voltage drop to 600 V, rather than 3200 V, thus only a single extra constant voltage layer would be required. In addition, this modulation circuit would permit the capacitance per layer to be reduced from the present $600\ \mu\text{F}$, to approximately $250\ \mu\text{F}$ – reducing cost and potentially height and thus delay per layer.

Table 4.3: Design parameter for the inductive adder prototype

Parameter	Symbol	Value	Unit
output current	I_{out}	2.4	kA
system impedance	Z_{IA}	6.25	Ω
output voltage	V_{out}	15	kV
IA pulse duration	$t_{\text{IA,pulse}}$	2.4	µs
rise time definition		0.5-99.5	%
output current rise time	t_{r}	75	ns
output current fall time	t_{f}	75	ns
constant voltage layers	N_{CVlayer}	19	-
modulation layers	N_{MODlayer}	3	-
branches per layer	N_{branch}	24	-
voltage per layer	V_{layer}	960	V
current per branch	I_{branch}	~ 105	A
cross section area per core	A_{c}	20	cm^2
stalk (inner insulation) diameter	d_{i}	103.4	mm
primary inner (outer insulation) diameter	d_{o}	108	mm
secondary parasitic capacitance per layer	C_{layer}	138	pF
secondary parasitic inductance per layer	L_{layer}	348	pH
capacitance per layer	C_{l}	600	µF
capacitance per branch	C_{b}	25	µF

4.3 Simulation in PSpice

The IA has been modelled in PSpice to predict the behaviour and confirm the analytical calculations. To reduce the complexity of the schematic and make global changes easier, the IA was divided into sub-circuits. Figure 4.2 shows the schematic of one sub-circuit representing one layer of the IA.

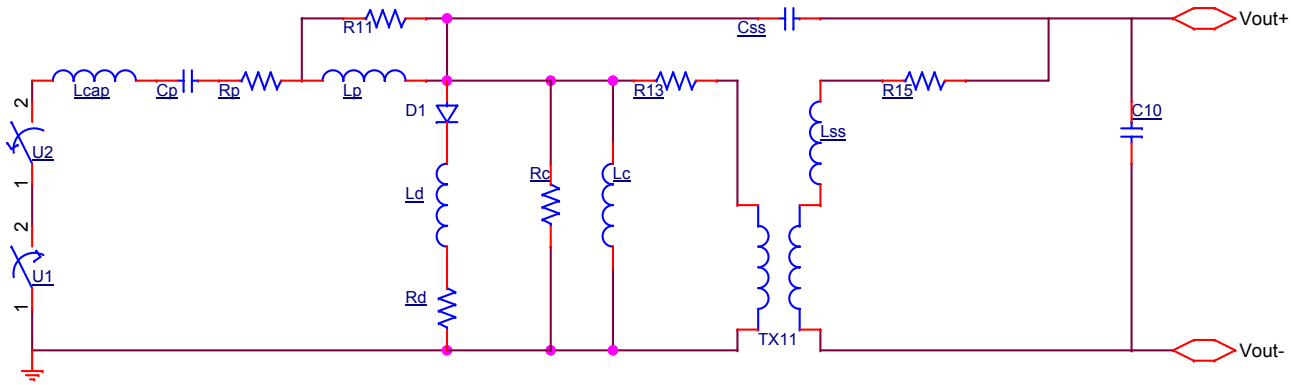

Figure 4.2: PSpice sub-circuit model of one constant voltage layer with a simple opening and closing switch

The MOSFET is represented by two switches, one closing (U1) and one opening (U2) switch. It was decided to represent the MOSFETs in this way in order to be able to progress rapidly with the design, as no

PSpice model of the MOSFETs was initially available. In addition, this is the approach used successfully by Holma [55, 58]. Pulse capacitor (Cp), freewheeling diode (D1) and transformer core (Lc, TX11, Rc) are represented by lumped elements. Parasitic effects are considered and represented by lumped elements in the model. The parasitic inductance of the primary circuit, excluding the capacitors, (Lp), pulse capacitor (Lcap) and freewheeling diode (Ld) are considered. The coaxial transmission line geometry of the stalk and primary winding are represented by capacitance Css and inductance Lss. Several resistors represent either ohmic losses in materials ($R_\mathrm{c}, R_\mathrm{p}$) or serve as damping elements (R11) in parallel to inductances, to avoid convergence errors. Resistor R13 prevents an inductive loop between the primary of Tx11 and Lc.

The capacitor value is 25 µF per branch, which results in a total capacitance of 600 µF per layer. The parasitic inductance of one capacitor was measured to be 28 nH, hence with 24 parallel branches 1.2 nH is considered for Lcap. Based on simulation results presented in [57] the total inductance of the primary circuit of a layer including the capacitor was estimated to be about 5 nH. Therefore the primary inductance Lp of the PSpice model was set to 3.8 nH. The parameters for the equivalent circuit of the magnetic core were determined by measurements (see table 6.1). The parasitic capacitance and the inductance due to the coaxial structure and the resistance of the stalk were calculated analytically. Other values, such as the parasitic inductance of the diode, the on state resistance of the MOSFET switches and their switching times were taken from the datasheets of the components and considering the geometry of the layout. Table 4.4 shows the parameters and the values used in the simulations.

Table 4.4: Component parameters for the PSpice simulation

Parameter	Value	Unit
Rclose of U1	1	µΩ
Rclose of U2	1.1	mΩ
Lcap	1.2	nH
Cp	600	uF
Vcap	915	V
Lp	3.8	nH
Ld	1	nH
Rd	10	mΩ
Rc	50	Ω
Lc	400	uH
Css	137	pF
Lss	350	pH
R11	100	Ω
C10	1	pF
R13	1	µΩ
Rp	0.1	mΩ
Rmod	0.45	Ω

In later simulations the switch was modelled using a PSpice MOSFET model provided by the manufacturer. A subcircuit was used to connect 24 MOSFET models in parallel. Each MOSFET of the subcircuit has a gate resistor connected to it's gate pin and DC voltage sources connected to the temperature reference pins. The connectors of the subcircuit allow the gate resistor, drain and source of all MOSFETs to be appropriately connected in parallel at the subcircuit box. Each gate pin was connected to a pulse source, the drain pin to the pulse capacitor and the source pin to the ground reference of the layer circuit. Figure 4.3 shows the

PSpice circuit of a constant voltage layer using a subcircuit with 24 parallel connected MOSFET models.

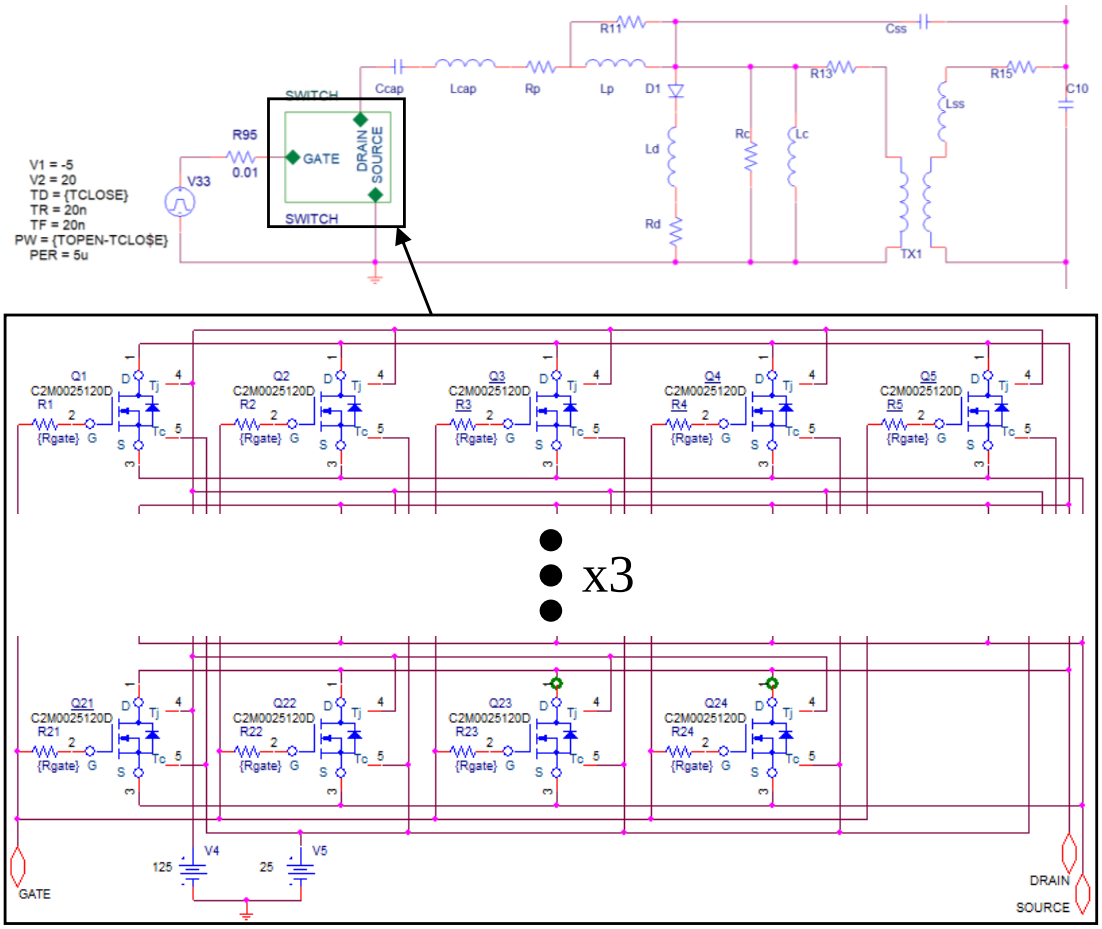

Figure 4.3: PSpice model of a constant voltage layer using a subcircuit with 24 parallel connected MOSFET models, provided by the MOSFET manufacturer

Figure 4.4 shows the PSpice schematic of a passive analogue modulation layer. The primary circuit of the passive modulation layer is modelled by a single modulation resistor (Rmod). The modulation resistor serves as an additional current path. Together with the magnetizing inductance of the transformer core (Lc) an RL-circuit is formed. At the beginning of the pulse no current flows through the magnetising inductance, all the current flows through the modulation resistor resulting in a voltage drop. During the pulse a part of the current transfers to the core inductance and the current through the modulation resistor hence reduces and therefore the voltage drop across the modulation layer decreases. Since the primary and secondary windings of the transformer are strongly coupled, the secondary voltage of the modulation layer also reduces and hence the capacitor droop can be compensated. The shape of the current during the pulse can be adjusted by changing the characteristics of the RL-circuit. If an additional transistor is connected in parallel to the modulation resistor, the current through the resistor can be actively controlled by controlling the base-emitter current of the transistor. In this way the output voltage of the IA can be actively modulated. Therefore a modulation layer with a transistor in the primary circuit is called active analogue modulation layer. The modulation techniques are described in detail by J. Holma in [55].

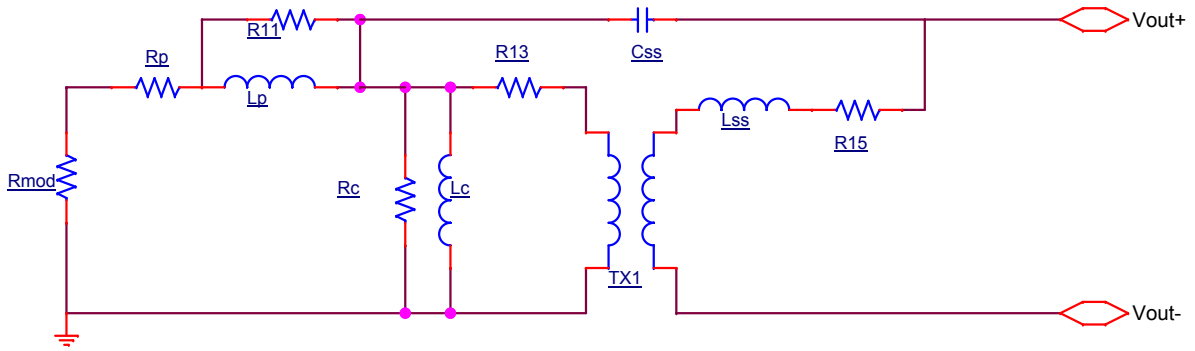

Figure 4.4: PSpice model of a passive analogue modulation layer

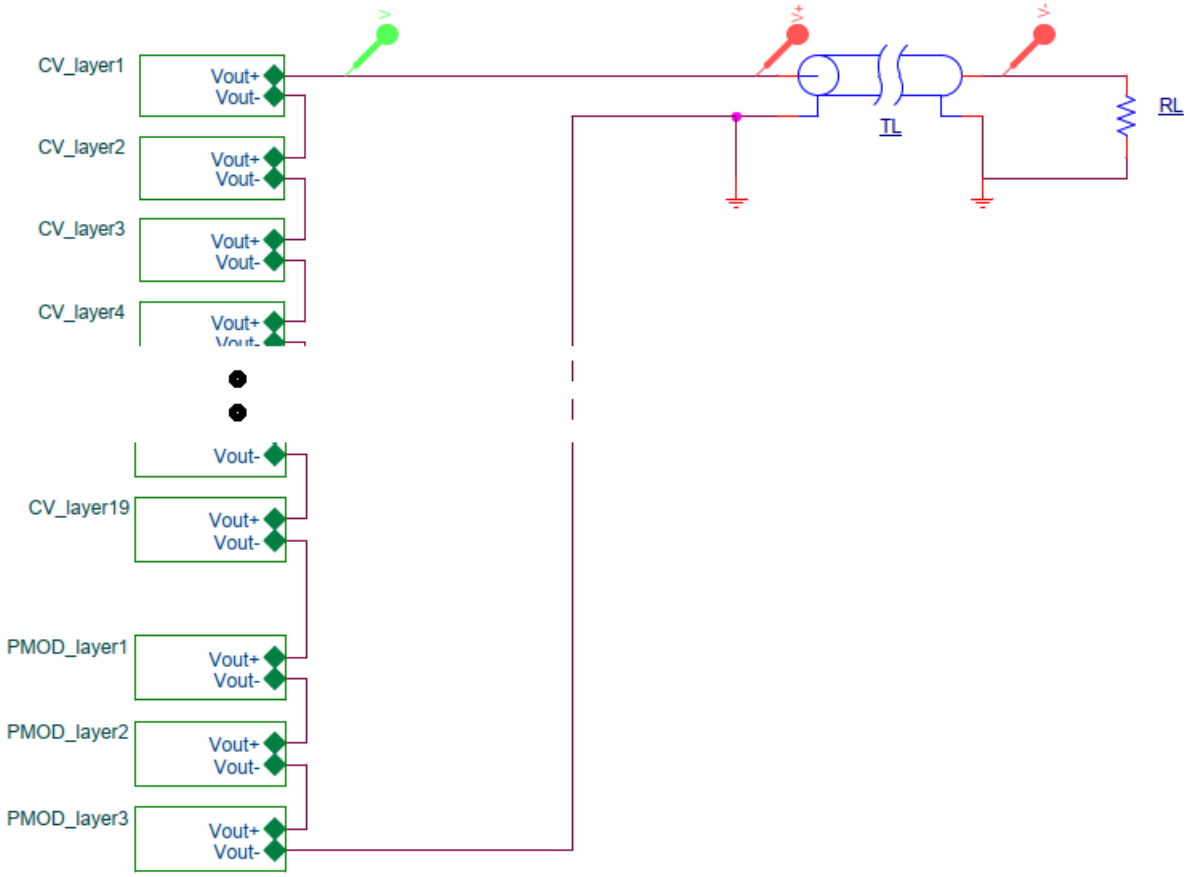

Figure 4.5: PSpice model of the IA stack consisting of 19 constant voltage layers and 3 passive modulation layers connected to a transmission line and matching load resistor

Figure 4.5 shows a PSpice model of an entire IA stack consisting of 19 constant voltage layers (CV_layer) and three passive analogue modulation layers (PMOD_layer) at the short-circuit side of the stack. Each constant voltage layer shown in Fig. 4.5 contains the sub-circuit shown in either Fig. 4.2 or Fig. 4.3 and each modulation layer contains the sub-circuit shown in Fig. 4.4. The IA is modelled as connected to a lossless transmission line (TL) with an impedance of $6.25\ \Omega$ and a single way delay of 355 ns, representing

a transmission line kicker magnet. The model of the transmission line is then terminated with a matched termination resistor (RL) to avoid reflections.

4.3.1 Simulation results

With the PSpice models described above, the output waveform of the IA can be simulated. The trigger times of the closing and opening switch need to be set in such way that the pulse is applied for the required pulse duration. Furthermore, in case of the switch-model shown in Fig. 4.2, the $10 - 90$ % switching duration was adjusted to be 32 ns, the same value as the datasheet value of the C2M0025120D MOSFET [37] used. The predicted output voltage can be probed at node Vout+ of laver CV_layer1. The field in the kicker magnet can be predicted in the model by probing the voltage difference between the input and output of the transmission line and integrating this difference with respect to time. Figure 4.6 shows the simulation results of the PSpice model using the simple switch and the PSpice model using the supplier MOSFET model. The predicted output voltage is a negative pulse which is shown in Fig. 4.6 with positive polarity. The pulse output voltage of the inductive adder has a rise time of 98 ns (0.5 % $-$ 99.5 %) in case

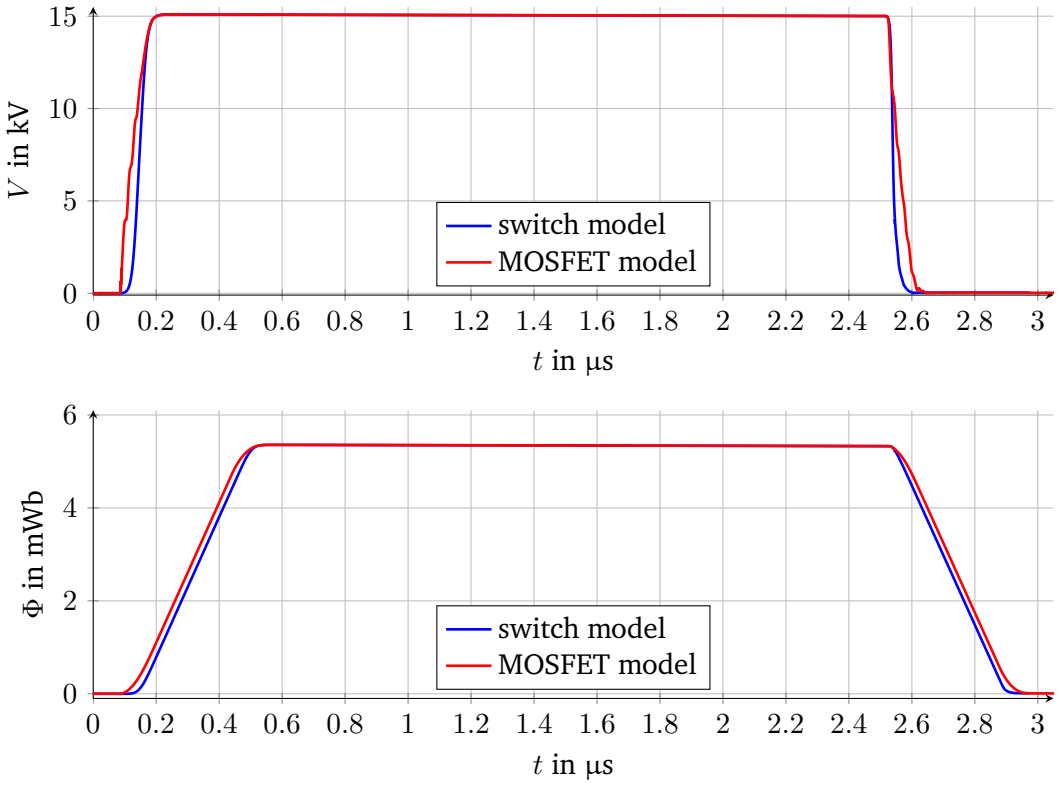

Figure 4.6: Simulated output voltage (top) and magnet field (bottom) of the kicker system modelled in PSpice

of the ideal switch model and 115 ns (0.5 % $-$ 99.5 %) in case of the supplier MOSFET model. The pulse duration ($V_{\text{out}} > 99.5$ %) is 2.3 µs in both cases and the pulse voltage fall time is 73 ns with the ideal switch model and 115 ns with the MOSFET model. The pulsed magnetic field in the magnet has a rise time (0.5 % $-$ 99.5 %) of 385 ns (ideal switch model) and 418 ns (MOSFET model). The pulse flattop is 2 µs for both cases and the fall time is 385 ns (ideal switch model) and 425 ns (MOSFET model). Simulations with

differently distributed modulation layers in the stack showed, that the ripple induced by the modulation layers is the lowest if all modulation layers are located at the short-circuit side of the stack, as shown in Fig. 4.5. The presented simulation results were conducted with the modulation layers at the short-circuit side of the IA stack.

Table 4.5: PSpice simulation results with the simple switch model and with the MOSFET model

Value Unit	$t_{\text{V,rise}}$ ns	$t_{\Phi,\text{rise}}$ ns	$t_{\text{V,fall}}$ ns	$t_{\Phi,\text{fall}}$ ns	$t_{\text{V,flattop}}$ µs	$t_{\Phi,\text{flattop}}$ µs	droop of V V	droop of Φ µWb
simple switch	98	385	73	418	2.30	2.00	73 (± 0.25 %)	21.3 (± 0.5 %)
MOSFET model	115	418	115	425	2.30	2.00	89 (± 0.3 %)	27.6 (± 0.5 %)

The voltage rise time $t_{\text{V,rise}}$ is in both cases longer than the required 75 ns. However the field rise time $t_{\Phi,\text{rise}}$ in the transmission line magnet is in both cases faster than the required 430 ns. Since the generator rise time and the magnet fill time do not linearly sum up to the field rise time, the requirement for the field rise time is still fulfilled even though the rise time of the generator is slower than required. In addition, as a result of the relatively fast field rise and fall, even with a 2.3 µs flattop of the generator pulse, a constant magnetic field of 2 µs can be achieved.

The output pulse rise time is slower or equal to the fall time. This is due to the fact that, once the switches are on, the remaining rise time is determined by the L/R of the circuit. Whereas, once the switch turns off (high-impedance), the fall time of the output voltage is determined mainly by the parasitic capacitance between primary and secondary (Css) per layer, by the number of layers and the load resistance: in case of the FCC-hh injection, the nominal impedance of the system is relatively low at $6.25\ \Omega$.

4.3.2 Influence of parasitic capacitance of coaxial geometry

The parasitic capacitance between the primary and secondary winding of a layer C_{layer} was derived in chapter 3.4.1. Although in reality this capacitance is distributed between the primaries and secondary windings, it is modelled as n-capacitors, one lumped at the top of each layer (called Css in Fig. 4.2). The value of the capacitance is defined by the geometry of the cylinder that is formed by the primary winding, secondary winding and the permittivity of the insulation in between.

MOSFET turn-on

During the off time of the IA output the parasitic capacitor is uncharged. During the rise time of the output voltage pulse, the parasitic capacitance of each layer are charged. Since each layer increases the potential of the stalk by a fraction of the output voltage, the parasitic capacitance of each layer is charged to a different voltage. The voltage V_{Clayer} across the parasitic capacitance C_{layer} of a layer, during the pulse flattop, can be calculated from:

$$V_{\text{Clayer,n}} = (n-1) \cdot V_{\text{c}}, \tag{4.5}$$

where n is the number of the layer in the stack ($n = 1$ for bottom layer) and V_{c} is the charging voltage across the pulse capacitor of each layer. Note the expression '(n-1)', in equ. 4.5, rather than 'n': this is because the primary voltage of each layer is V_{c}. It can be seen that $V_{\text{Clayer}} = 0$ V for $n = 1$. The reason for this is that in the first layer of the stack, both the stalk and the primary winding have the same potential

before, during and after the pulse, therefore the voltage across the parasitic capacitance of this layer is 0 V.

The charge stored in the lumped parasitic capacitance of a layer during the pulse $Q_{\text{Clayer,n}}$ can be calculated from its parasitic capacitance C_{layer} and the charging voltage during the pulse $V_{\text{Clayer,n}}$ with:

$$Q_{\text{Clayer,n}} = C_{\text{layer}} \cdot V_{\text{Clayer,n}} = C_{\text{layer}} \cdot (n-1) \cdot V_{\text{c}}. \tag{4.6}$$

Equation 4.6 shows that the charge in the parasitic capacitance is different depending on the position of the layer in the stack, since also the charging voltage of the parasitic capacitance depends on the layer number. Each layer of the IA raises the potential of the stalk above itself and hence charges the parasitic capacitance of all the following layers in the stack by V_{c}. The amount of charge the switch of a layer needs to conduct to charge the parasitic capacitances of the stack above itself, can be calculated with:

$$Q_{\text{SWlayer,n}} = (N-n) \cdot C_{\text{layer}} \cdot V_{\text{c}}, \tag{4.7}$$

where $Q_{\text{SWlayer,n}}$ is the charge going through the switch of layer n to charge the parasitic capacitance C_{layer} in layers n+1 through N by voltage V_{c}, and N is the total number of layers in the stack. Therefore the MOSFETs of the first layer carry the largest charge whereas the last layer carries none. The MOSFETs must have adequate current rating, especially when the output voltage is high and there is a large number of layers.

MOSFET turn-off

Discharging of the parasitic capacitance, between primaries and secondary, happens at turn-off of the MOSFETs, when the output voltage pulse is reducing in magnitude. The discharging current of the capacitance is carried by the free wheeling diode of the layers. The free wheeling diode of the top layer (n=N) in the stack carries the highest discharging current - it consists of the charge stored in the parasitic capacitance (C_{layer}) of this layer and the current associated with discharging the parasitic capacitors of all layers below. The current peak through the free wheeling diode decreases with the layer number in the stack. The current load on the diode is highest for the n^{th} constant voltage layer (top of stack) and zero for the first layer (bottom of stack). The charge conducted by the diode during MOSFET turn-off, $Q_{\text{diode,n}}$, can be calculated.

$$Q_{\text{diode,n}} = \sum_{i=1}^{n-1} Q_{\text{Clayer,i}} = \sum_{i=1}^{n-1} (i-1) \cdot C_{\text{layer}} \cdot V_{\text{c}} \tag{4.8}$$

In addition to the current peak during turn-off, caused by discharging the parasitic capacitances, the diode also conducts the magnetizing current of the transformer core. The magnetizing current is a relatively low current of < 50 A, which increases during the pulse duration and decreases after the pulse. The current to discharge the parasitic capacitors is a transient current that can reach kA and occurs during the fall time of the pulse. The transient current peak can be can be estimated with:

$$I_{\text{diode,n}} = \frac{\mathrm{d}V_{\text{Clayer,n}}}{\mathrm{d}t} \cdot C_{\text{layer}}, \tag{4.9}$$

where $\mathrm{d}V_{\text{Clayer,n}}$ is the voltage drop over the capacitor during turn-off and $\mathrm{d}t$ the time during which the parasitic capacitor is discharged (transition time). To show this effect a 30 layer IA with a characteristic impedance of $Z_{\text{IA}} = 10\ \Omega$, a capacitor charging voltage in each layer of 1 kV and a matches load of $10\ \Omega$

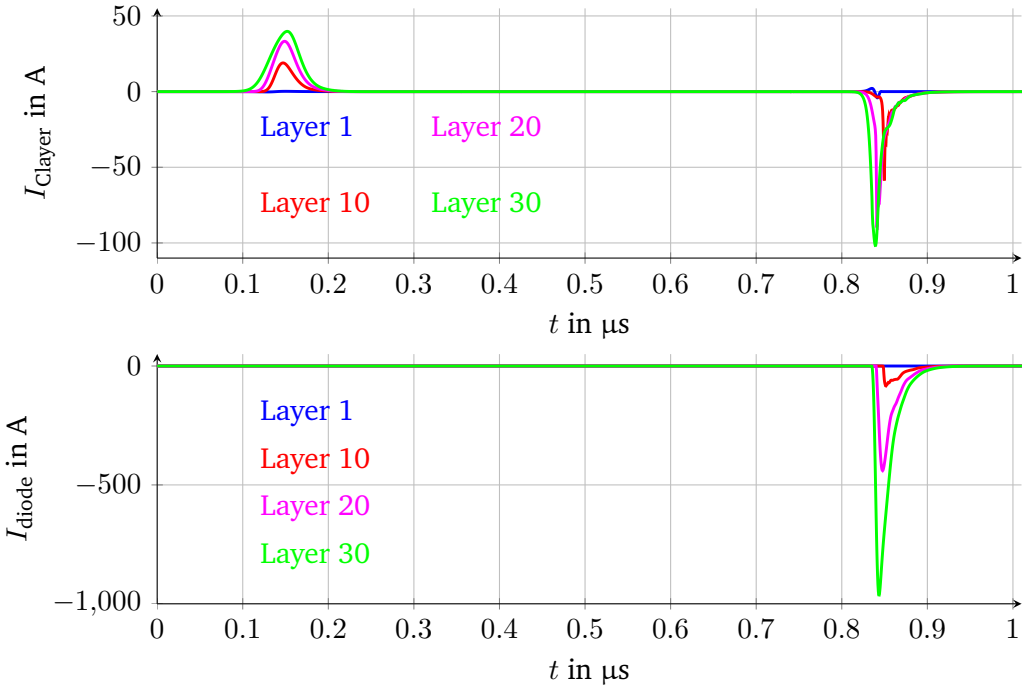

Figure 4.7: Example for the simulated current through the parasitic capacitor I_{Clayer} (top) and the free wheeling diode I_{diode} (bottom) of a simulated $10\ \Omega$, 30 layer IA

has been simulated with a pulse length of 1 µs. The effect would be significantly greater with a lower impedance IA (C_{layer} larger). In Fig. 4.7 it can be seen that the current through the parasitic capacitance of a layer increases as one goes up the stack. It is lowest in the first layer on the short-circuit side of the IA, increases with the layer number and is biggest in the layer on the HV output side. Figure 4.7 also shows the current through the free wheeling diode at turn-off of the MOSFETs. The current peak through the diode at turn-off is highest in the 30th layer, and decreases with reducing layer number. It can be seen that the current peak through the diode of a layer is significantly bigger than the discharging current of the parasitic capacitor of the layer. As described earlier, the reason for this high diode current is that the current to discharge the parasitic capacitances of the layers below the top layer are also flowing through the free wheeling diode of the top layer. The sum of the discharge current peak of C_{layer} of all layers is therefore equal to the current peak through the diode of the highest layer. The magnetizing current of the core can be neglected for this consideration since its contribution is significantly smaller. The diode must be rated for this peak current which can be greater than the load current and will occur at every pulse.

4.4 Redundancy and reliability of the FCC IA

Thanks to the modular design of the IA it is easy to implement redundancy. In case of a high redundancy also a high reliability is given since broken elements are not necessarily critical for the operation of the system. Different methods could be implemented for dealing with a failure.

A failure that causes the malfunction of one of the layers could be detected and the affected layer will not

be triggered until the defect is repaired. Instead an additional spare layer in the IA stack will be triggered to compensate the missing voltage caused by the faulty layer. In this way the redundancy can be defined by the number of additional layers added to the IA.

A limitation of this method is the rise time of the output pulse. Due to the fact that more layers are added to the stack, the stack length and therefore the propagation time increases. For this reason the total number of layers, including constant voltage layers, modulation layers and redundant layers, is limited by the rise time requirements of the output pulse.

Another way to improve the reliability of the IA without adding an entire layer to the stack is to underrate the components. For example by setting the layer voltage to 70 % of the rated component voltage. In case of a faulty layer the voltage of the remaining layers could be increased to keep the output voltage constant. This method would not change the number of operating layers in the stack and might therefore have less impact on the pulse rise and fall time.

Given a fault in the primary circuit the operation of single branches can be observed and triggering can be stopped in case a faulty behaviour is detected. The remaining branches of the layer would take over the current and must be designed accordingly. An example for this kind of problem would be a broken trigger line to the branch, a broken gate driver or a sc-switch failing open. If a MOSFET fails to short-circuit the layer must be insulated from the charging power supply.

In any case, a system with redundancy would require sensors and control electronics in each layer and branch. Furthermore a system is required that indicates which layer and branch is defective for quick replacement.

The realisation of a control system to increase reliability of the IA would be an important component for an operating system in an accelerator complex. The prototype IA designed for the FCC injection system is built for experimental purposes only and therefore not equipped with such a system.

5 Fault conditions

The modularity of the inductive adder (IA) makes it possible to readily implement a redundancy in the system that makes it feasible to continue operation even after a fault has occurred in the system. The number of layers in the IA and the number of parallel branches per layer should be designed such that the failure of one element does not have fatal influences upon the total system operation. Several fault conditions that can happen with an IA were simulated and discussed in detail by Holma in [55] and are therefore only briefly summarized in Tab. 5.1.

Table 5.1: Summary of possible fault conditions based on simulations of Holma in [55]

Fault description	Consequences
Delayed or advanced triggering of a single layer	Pulse rise and fall times are increased Pulse flat-top duration is shortened Pulse flat-top amplitude is reduced
Switch does not turn on	Pulse flat-top amplitude is reduced Pulse flat-top droop increases Power losses in switches increase
Switch does not turn off	High power losses in the switch, which does not turn off Risk of saturation of a magnetic core Considerable voltage across the load during off-time
Switch fails to short-circuit	Very high current can flow through the short-circuited switch during a pulse High power losses in parallel switches during a pulse High current in the free-wheeling diode after the pulse
Short-circuit in the load	High power losses and high peak current in switches High peak current in diodes Risk of high transient voltage during turn-off
Open circuit in the load	Risk of high transient peak voltage in the secondary
Saturation of a magnetic core	High power loss and high peak current in switches in the layer, in which the core saturates High peak current in diodes of the layer, in which the core saturates
Layer does not turn on	Pulse flat-top amplitude is reduced Diodes of faulty layer carry load current during pulse
Layer does not turn off	Risk of core saturation in the layer Full discharge of capacitors into load
Trigger signal is too long	Risk of core saturation in all layers

5.1 System protection methods in fault case

To protect the IA against some of the described faults in Tab. 5.1 a protection mechanism can be implemented. An over current protection can prevent switches failing in many of the mentioned fault cases - e.g. saturation of the core and a short-circuit in the load, where the current through the switch would otherwise become too high and destroy the MOSFET. Due to the low on state resistance of SiC MOSFETs, and therefore a low voltage drop over the switch, a current pickup or current sensing resistor would be necessary to detect the over current. After the over current is detected a fast transistor circuit can pull down the gate pin of the MOSFET. The protection should be very fast ($<< 1$ µs) to ensure the MOSFET turns off before the temperature limit is exceeded or the magnetic core saturates. Some gate drivers provide a desaturation detection (DESAT) and turn-off (soft turn-off) to protect the switch against excessive over current. Even if these features are mainly designed for IGBT drivers they might be available also for SiC MOSFETs in the near future and would simplify the design for an efficient switch protection.

5.2 Fast switch-off in case of core saturation

The magnetic core of each layer must not saturate: In case of saturation the magnetising current rapidly increases which leads to a high stress on the MOSFET and can cause its damage. To avoid core saturation all cores are designed with a margin in their cross sectional area. The additional cross sectional area provides a certain time buffer to react in case too long pulse length is detected. A fast over current protection, as described in chapter 5.1, could be able to prevent destruction of switches since it would detect the over current and could turn off the switch. However, if the over current is detected, saturation of the core may have already started. Hence, depending on the layer voltage, the switch needs to be turned off within a few tens of ns to avoid that the current exceeds the critical value and damages the switch: hence, there must be a reasonable margin between the normal pulse current in the MOSFET and the maximum safe current in the MOSFET.

5.3 System protection for biasing circuit

An IA with a biasing circuit, as designed in this thesis introduces an additional complexity to the system that requires additional protection mechanisms. In case of a fault in the biasing circuit that interrupts the biasing current, the magnetic cores would saturate directly or during the next pulse, depending on in which point of the BH-curve the failure happens. A protection system would be appropriate that detects the current in the biasing circuit and prevents a trigger signal being generated if the biasing current is not within a specific range. However, since the biasing circuit is of a rather robust design with mainly passive components, the probability of a fault is small.

5.4 Consequences of a system failure for the FCC injection kicker system

The injection kicker systems for the FCC-hh consists of 18 kicker magnet systems per beam. Each kicker magnet system has a kicker magnet, a pulse generator and everything else necessary to operate both of

these. If the pulse generator is an IA, as described in this thesis, there are various failure modes that can occur and have an impact on the kick strength of the beam. In the best case the failure would not affect the operation of the machine but in the worst case it could cause a beam loss and the beam to be dumped in the collimation systems or other machine components downstream. In case the beam hits a superconducting magnet it is likely to cause a quench of the superconductors and therefore downtime of the machine.

One big advantage of the IA as a pulse generator is the high modularity that makes it possible to build the system in such way that operation is possible even if one or more components of the IA fail. Table 5.2 gives an overview of possible failures that can occur within a FCC kicker system using an IA as pulse generator and shows the effect of the failure. The high number of kicker systems makes it possible that even if one entire system does not work the kick strength is only reduced by 5.6 %. Even if normal operation is not possible with the reduced kick strength, due to low beam quality, it does not cause a beam loss and therefore is not of a high risk for other accelerator components. In case of a failing layer the system kick strength would be reduced by only $0.3 - 0.4$ %. Due to the reduced voltage drop over the modulation layer a fault of the modulation layer can even cause both an increased kick strength and an increased flat-top droop.

Table 5.2: Failure modes, possible failure cause and consequences of the FCC injection kicker system

Failure mode	Possible cause	Consequence
One layer fails	fault of trigger system fault in switch fault in capacitor saturated core	$0.3 - 0.4$ % less system kick strength
One kicker system fails	fault in magnet fault of IA	5.6 % less system kick strength
Modulation layer fails	fault in modulation resistor	0.6 % higher system kick strength and increased droop

Many of the proposed solutions to get a fault tolerant system rely on a efficient and reliable electronics and control system for the FCC kicker system. The reliable detection of the various possible failure modes, fast data processing and a efficient fault repair are fundamental to take advantage of the redundancy and reliability advantages of the IA.

6 Measurements on components

To build a prototype of the inductive adder (IA) as described in chapter 4 several sample components have been selected, tested and analysed. This chapter describes the tests conducted and outlines the final choice of components used for the prototype.

6.1 Magnetic cores

In a pre-selection phase several magnetic materials have been measured and tested. Only materials featuring appropriate parameters for the IA application were selected for measurements. Different measurements were conducted to validate the suitability of the sample cores. All measured cores are nanocrystalline, tape wound cores because of the high saturation flux density and relatively low losses. The physical dimensions of the cores should be within a small margin to fill the core housing efficiently.

6.1.1 Measurement of pulsed magnetizing current

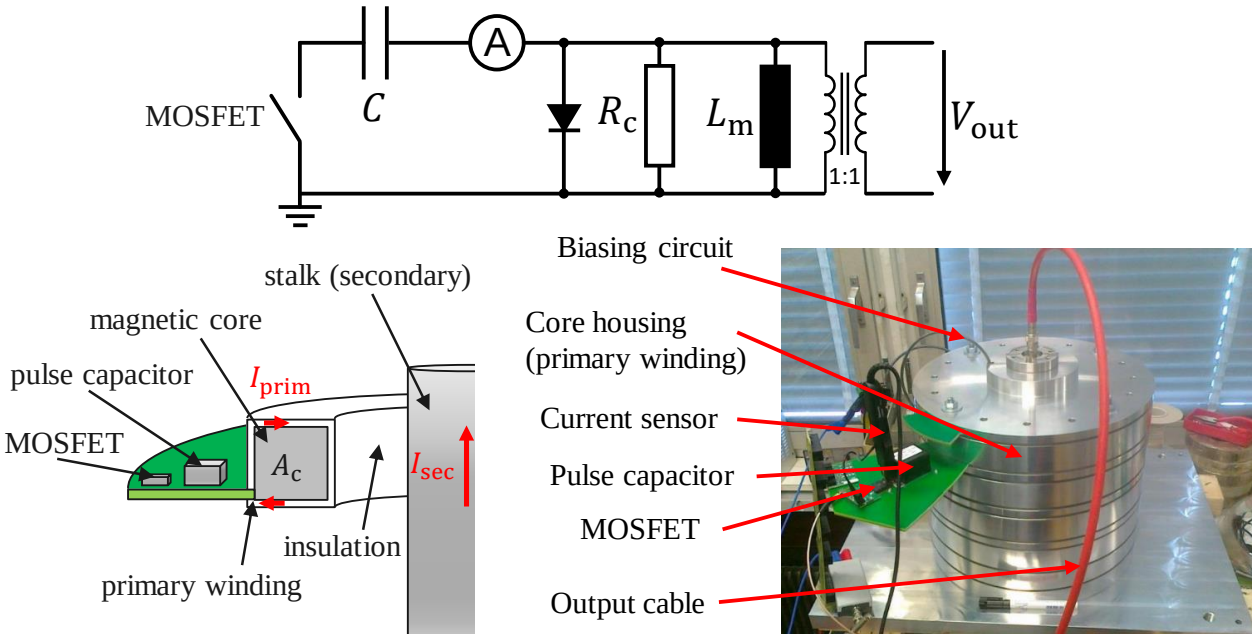

Figure 6.1: Equivalent circuit, schematic drawing and test setup to measure the magnetizing current of a magnetic core

The pulse characterisation of each of the magnetic cores was conducted on a test bench which had been constructed for the IA prototype for the CLIC study [55, 109]. For the measurements, a single branch of the IA is connected to the primary winding of a 1:1 transformer. The branch together with the winding form a primary loop of the IA. The secondary of the IA (stalk) serves as the secondary winding of the 1:1 transformer, no load is connected to the secondary: hence, the secondary current is nominally zero. Figure 6.1 shows the equivalent circuit, a schematic drawing and the test setup for measuring the magnetizing current of the magnetic core. The current in the primary loop and the secondary voltage are measured. Since the current in the secondary winding of the IA is zero, the primary current is related to the core losses and magnetizing current of the magnetic core. The measured cores had the dimensions of $d_\mathrm{o} = 282$ mm, $d_\mathrm{i} = 149$ mm with a height of $h_\mathrm{c} = 25$ mm. The primary current is interpreted as consisting of a step current (core losses) and a linearly rising inductive current (magnetizing current), before the core saturates.

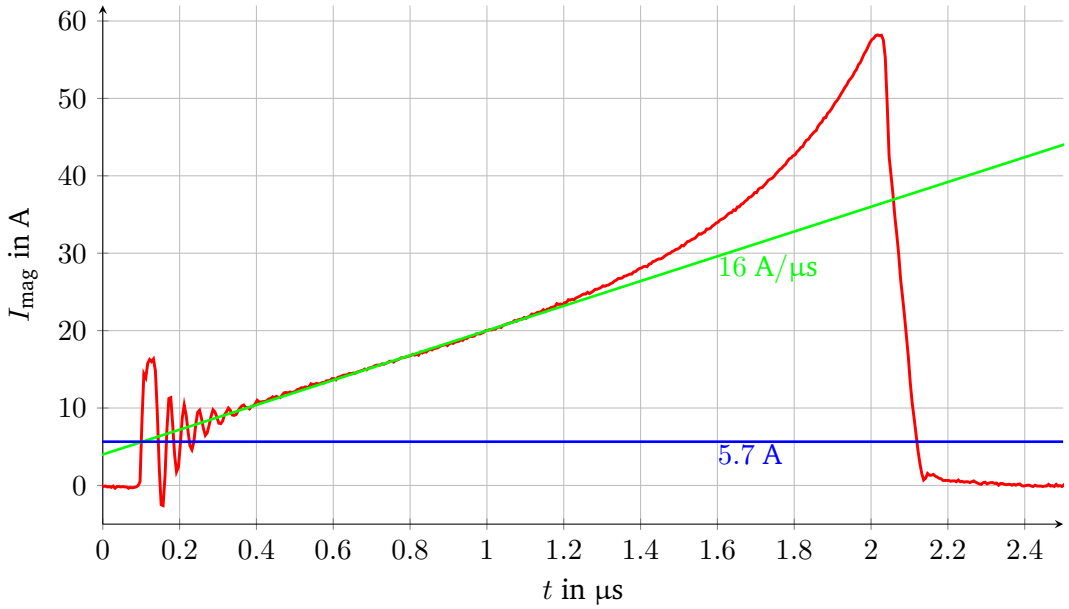

Figure 6.2: Primary current (red) measured for an applied voltage of 700 V; decomposed into a core loss current (5.7 A, blue) and a magnetizing current (linearly increasing by 16 A/µs, green)

Figure 6.2 shows the primary current for a sample core during a pulse with a capacitor charging voltage of 700 V. For the prototype, a layer voltage of up to 1000 V is planned, which needs to be taken into account when interpreting the measurements, since then the reachable pulse duration at 1000 V will be reduced accordingly to 7/10th of the measured duration at 700 V. After the initial transient oscillation the current linearly increases with 16 A/µs before the core saturates and the current then increases exponentially. The step component of the current is about 5.7 A. The core losses, modeled by R_c, can be calculated from the step current component I_DC in the primary loop and the charging voltage of the capacitor V_c.

$$R_\mathrm{c} = \frac{V_\mathrm{c}}{I_\mathrm{DC}} = \frac{700\ \mathrm{V}}{5.7\ \mathrm{A}} = 123\ \Omega \tag{6.1}$$

The magnetizing inductance L_m can be calculated from the current ramp $\frac{\Delta I}{\Delta t}$ and the charging voltage of

the capacitor.

$$UV_\mathrm{c} = L_\mathrm{m}\frac{\Delta I}{\Delta t} \rightarrow L_\mathrm{m} = V_\mathrm{c}\frac{\Delta t}{\Delta I} = 700\ \mathrm{V} \cdot \frac{1}{16\ \mathrm{A/\mu s}} = 44\ \mu\mathrm{H} \tag{6.2}$$

The magnetizing current shown in Fig. 6.2 was measured for a core with a linear BH-curve. In Fig. 6.3 the magnetizing current of a linear (upper part) and square (lower part) shaped BH-characteristics are shown, each with different biasing currents. The descriptions „linear“ and „square“ refer to the different shape of the BH-curve depending on the material and on the heat treatment of the material applied by the supplier. If the BH-curve is very steep (high relative permeability) and forms a square or rectangular it is called square shaped and if the BH-curve is flat (lower relative permeability) it is called a linear shaped BH-curve. Figure 6.5 in chapter 6.1.2 shows various BH-curves of different magnetic cores.

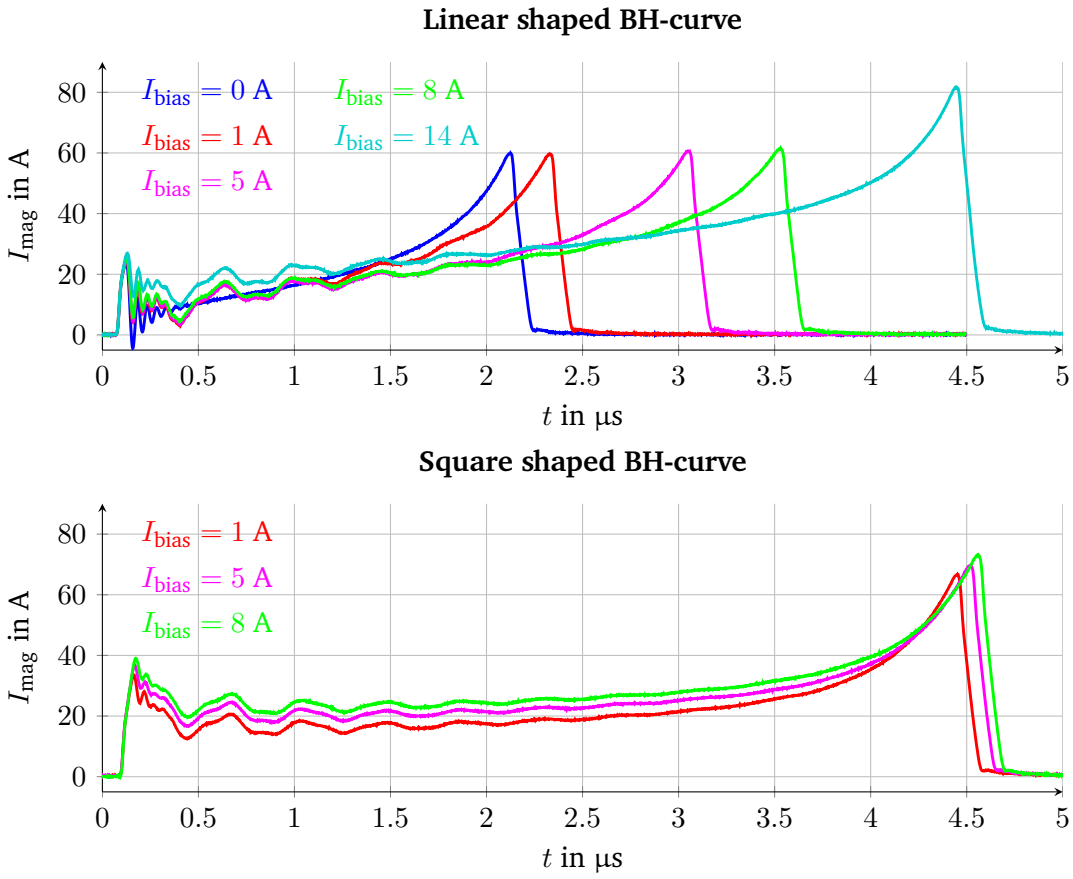

Figure 6.3: Measured magnetising current of sample magnetic cores with linear (top) and square (bottom) shaped BH-curve at 700 V capacitor voltage

The duration of the pulse applied to the core was set to a value where the saturation effect becomes visible. The measurements have been conducted with biasing currents of 0 A (blue), 1 A (red), 5 A (magenta), 8 A (green) and 14 A (yellow), as shown in Fig. 6.3. In case of the square shaped BH-characteristic the measurement could not be conducted for a biasing current of 0 A since the core has a remanent field close to the saturation flux density. Similar measurements were not conducted for 14 A bias, since the core was at its saturation flux density in the 3rd quadrant of the BH-curve. It can be seen that the achieved pulse duration, for a given capacitor voltage can be increased by biasing the magnetic core into the 3rd

quadrant. In case of the linear BH-characteristic the pulse length up to the saturation point increases approximately linearly with the biasing current. In case of the square shaped BH-curve the pulse length of a low magnetising current (1 A) and the higher magnetising current of 8 A do not vary much since the core is already saturated in the 3rd quadrant of the BH-curve with a small bias current. In case of the linear BH-characteristic, it can be seen that the biasing circuit introduces ripples on the magnetizing current which are not visible in case of 0 A biasing current, where the biasing circuit was not connected. The current was also measured to confirm that if the biasing circuit was connected without a current flow through it, the ripple was present and hence is due to the bias circuit. The two cores with different BH-curve shape, for which the performance is compared in Fig. 6.3, are from the same manufacturer (Vakuumschmelze). The material used for both cores is identical, therefore the saturation flux density is approximately the same. The shape of the BH-curve is 'programmed' with a temperature treatment after the core is produced. It can be noticed that the weight of the cores of manufacturer 2 are approximately 900 g ($\sim$ 13.5 %) less than the weight of the cores of manufacturer 1. Manufacturer 2 mentioned that its material is around 20 % lighter than „standard material". However, also a smaller fill factor can cause a lighter core, the influence of a slightly smaller fill factor can be neglected compared to the saturation flux density if comparing the pulse lengths reached with the different core types.

6.1.2 BH-curve measurement

To compare the saturation flux density of the sample cores, the BH-curve was measured. Figure 6.4 shows the test setup for the BH-curve measurement. The sine wave of a function generator is amplified and connected to the primary winding (5 turns) of the transformer core. The current in the primary circuit is

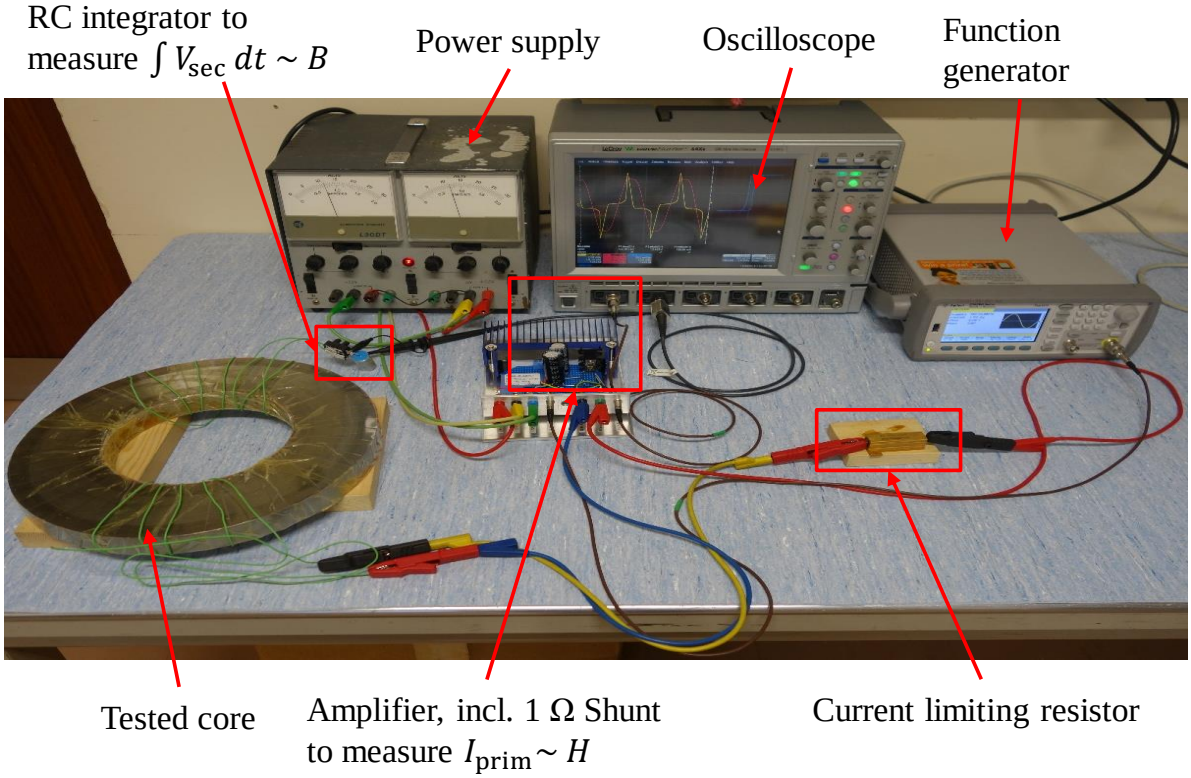

Figure 6.4: Test setup for BH-curve measurement on the sample cores

measured with a $1\ \Omega$ shunt using an oscilloscope. The secondary winding (7 turns) of the core is connected to an RC integrator and the output is also measured with the oscilloscope. The magnetic flux density can be calculated from the integrated output voltage V_{sec} with

$$B = \frac{\int V_{\text{sec}} dt}{N_2 \cdot A_2} = \frac{V_{\text{sec}} \cdot R_{\text{int}} \cdot C_{\text{int}}}{N_2 \cdot A_{\text{Fe}}}, \tag{6.3}$$

where R_{int} and C_{int} are the resistor value and capacitor value of the RC integrator, respectively, N_2 the number of secondary windings and A_{Fe} the effective cross section area of the core. The integration can be realized with a simple RC circuit (lowpass) or an integrating circuit based on an operational amplifier. For lower frequencies, the RC circuit can be used. Higher frequencies require the use of an operational amplifier circuit. The BH-curves were measured at 500 Hz; for this an RC integrator is sufficient. The corresponding magnetic field strength H can be calculated from the primary current measured with the shunt resistor $I_{\text{prim}} = \frac{V_{\text{prim}}}{R_{\text{shunt}}}$ with

$$H = \frac{I_{\text{prim}} \cdot N_1}{l_{\text{e}}} = \frac{V_{\text{prim}} \cdot N_1}{R_{\text{shunt}} \cdot l_{\text{e}}}, \tag{6.4}$$

where N_1 is the number of primary turns and l_{e} the effective magnetic path length of the core. Plotting the measured integrated voltage versus the shunt voltage shows the shape of the BH-curve of the magnetic core. With an oscilloscope in XY-operation the two measured values can be plotted as a function of each other to get the BH-characteristics. After saving the waveform, the scaling can be adapted by using equations (6.3) and (6.4). The scaling was calculated using the average magnetic path length and cross section area of the core. Calculated according to IEC60205 the magnetic path length would be 7 % shorter and the average cross section area 3 % smaller. The BH-curve helps to compare many important factors of the cores, such as saturation flux density, remanent flux density, coercive field strength and permeability of the core for a given frequency. The measured BH-curves are shown in Fig. 6.5, different cores of one kind are shown in different shades of one color. The BH-curve measurements confirm the pulse current measurements. The saturation flux density of supplier 1 is higher than from supplier 2 and 3, which was used for the cores of the CLIC damping ring inductive adder prototype. Also in terms of permeability of the cores, which is equivalent to the steepness of the BH-curve, the BH-curve measurements confirm the measurements of the magnetizing current. Due to the varying steepness, also the required biasing current to set the initial working point of the core in saturation can be explained.

Table 6.1: Sample cores with measured values (italic values measured on differently sized cores)

supplier	BH-char.	R_{c} in Ω	L_{m} in µH	ΔB_{sat} in T	I_{bias} in A
1 (Vacuumschmelze)	square	55	282	2.4	1
1 (Vacuumschmelze)	square	50	367	2.4	1
1 (Vacuumschmelze)	square	65	191	2.4	1
1 (Vacuumschmelze)	square	75	160	2.4	1
1 (Vacuumschmelze)	linear	150	56	2.4	14
1 (Vacuumschmelze)	linear	160	42	2.4	14
2 (Magnetec)	linear	230	30	2.1	5
2 (Magnetec)	linear	200	30.6	2.1	5
3 (Hitashi Metals)	linear	*70*	*28.8*	2.0	20
3 (Hitashi Metals)	linear	*70*	*28.8*	2.0	20

Table 6.1 lists all ten sample cores and summarizes the measurement results. The requirements for a magnetic core for the IA prototype are a high saturation flux density, low biasing current and low losses.

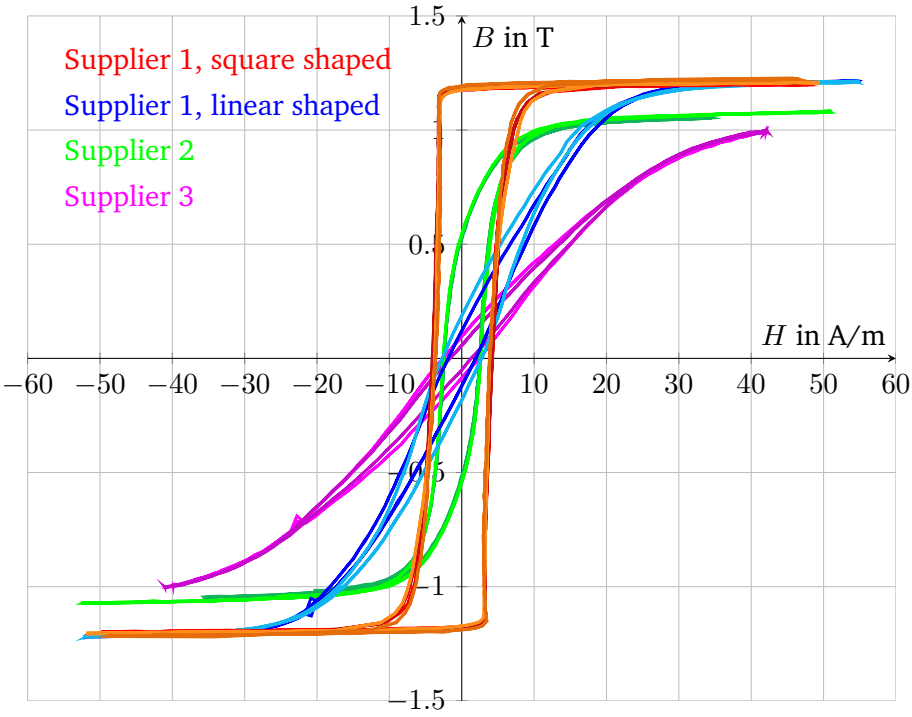

Figure 6.5: Measured BH-curves of the sample cores at 500 Hz

The high saturation flux density leads to a high magnetic flux density swing (ΔB) and helps to reduce the required cross-sectional area of core material, the low biasing current makes the design for the biasing circuit easier and low losses cause less heating of the material. The best cores fulfilling this requirements are those with the square shaped BH-curve of supplier 1. The other suppliers did not offer cores with a square shaped BH-curve. The high saturation flux density and low biasing current are the strongest argument for this core the relatively high losses, represented by a low R_c can be accepted. Therefore, for the constant voltage layers of the FCC IA prototype the cores with a square shaped BH-curve of supplier 1 will be used. Since for the modulation layers a flat, linear BH-curve is preferred (see section 4.2.3) the magnetic cores of supplier 3 are envisaged to be used.

6.2 Semiconductor switches

Many appropriate semiconductor switches with both turn-on and turn-off capability exist on the market. IGBTs are available up to several hundred Ampere and several kV, but do not have the required fast switching times. Silicon MOSFETs are presently available up to 1200 V and a few hundred Ampere: although the switching times are generally fast, the on-state resistance of Si-MOSFETs is still in the range of several hundred mΩ, which causes a relatively high voltage drop for a low impedance system, such as the FCC injection. Silicon Carbide (SiC) MOSFETs are available with rated voltages of up to 1700 V and pulse currents of more than 100 A. To reach higher currents MOSFETs can be connected in parallel. SiC MOSFETs are characterized by a low on-state resistance, usually less than 50 mΩ, and relatively fast switching times. The relatively high voltage rating and low on-state resistance, combined with fast switching, makes SiC MOSFETs the preferred devices for the IA prototype [109, 110].

During the initial design period (2015/2016) of the IA prototype, only relatively low current SiC MOSFETs, with the highest voltage ratings were commercially available on the market from two suppliers. However, several suppliers advertised suitable SiC MOSFETs to be released in the near future. Table 6.2 gives an overview of datasheet values of SiC MOSFETs on the market or to be released.

Table 6.2: Datasheet values of SiC MOSFETs on the market or released soon

Manufacturer		CREE	CREE	Microsemi	Rohm
Rated voltage	kV	1.2	1.7	1.2	1.2
DC current	A	90	72	80	95
Pulse current	A	250	160	190	237
Rise time	ns	32	20	9	44
Fall time	ns	28	18	22	28
On state resistance	mΩ	25	45	40	22
Price per pc.	Euro	60	90	40	60

From the four listed MOSFETs only the first three were deliverable. The MOSFETs have been tested and did not show any significant performance differences among themselves during the tests. For availability reasons, the 1.2 kV MOSFET from CREE was selected for the prototype IA. In any case, all of the listed MOSFETs can be used for the inductive adder, which makes sourcing of spares easier since several suppliers can be used. The gate driver used for the SiC MOSFET should be able to turn off the MOSFET with a negative gate voltage as recommended in [2, 24, 38, 77, 88]. Furthermore the gate driver should have a galvanically insulated (> 1.2 kV) trigger and power supply to avoid that a failure of the MOSFET causes failures in other parts of the connected circuits. For the FCC prototype the gate driver circuit is based on a commercially available insulating gate driver circuit from Wolfspeed [38]. The original 9 A gate driver chip was replaced by one capable of delivering 14 A [63] and the gate resistor was reduced from $6.67\ \Omega$ to $2.4\ \Omega$ to achieve faster turn-on of the MOSFET. To reduce the spread of turn-on delays of the MOSFETs, the opto-isolator of the original board was replaced by a digital isolator [95] with lower propagation delay and reduced jitter.

6.2.1 Radiation hardness of SiC components

A potentially critical point is the radiation hardness of SiC components. Since the generator is ideally placed as close as possible to the kicker magnet to avoid or minimize cable lengths, it could be placed inside the tunnel. Semiconducting devices are known for single event effects (SEEs) induced by high energy hadrons (HEH), as they are generated in particle accelerators [6, 46, 79, 94]. Similar conditions can be found in aerospace applications for electronic circuits [19], but also on the earths surface due to cosmic rays [113]. SEEs can temporarily disturb semiconducting devices or permanently destroy them [74], as previous experiments on SiC components showed [71]. Since SiC technology is relatively young, investigations on the radiation hardness of SiC devices are still ongoing [74, 75]. Tests conducted by the author at the CHARM facility at CERN [76] with a method used for Si devices were not successful. A common method to increase the resistance to SEE of Si devices is to derate the operation voltage of the component. If SiC components for higher voltages are used, this method is expected to improve also the resistance against SEEs of SiC components.

6.3 Capacitors

The pulse capacitors require a high capacitance to realise the required pulse current and duration with a low voltage droop. At the same time the dimensions of the capacitor should be kept small to realize a small layer height to allow fast rise times and compact stacks while keeping the width small to allow sufficient parallel branches: thus a high energy density is desirable. In addition, the inductance of the primary circuit is influenced by the parasitic inductance of the capacitor itself. To obtain a high energy density with low inductance, custom made sample capacitors were ordered from European suppliers and tested upon arrival. The parasitic inductance of the sample capacitors has been determined by measuring the oscillating discharge of a short-circuited capacitor, as described in [70] and applied in [56]. Figure 6.6

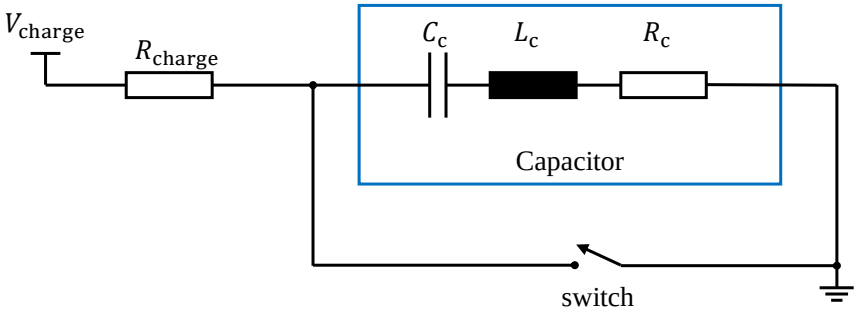

Figure 6.6: Lumped element schematic of the capacitor measurement setup

shows a lumped element schematic of the circuit used to measure the parasitic inductance and resistance. The short-circuit is realized with a wide copper plate. The resistance and the inductance of the copper plate cannot be separated from those of the capacitor and are interpreted to belong to the capacitor. However, as the plate is wide, this should only infer a small error. The capacitor was charged to a voltage of 20 V and short-circuited mechanically. The circuit shows an oscillation at a resonant frequency f_{res} and the voltage across the capacitor is measured. From the resonant frequency of the oscillation the parasitic inductance L_{c} can be calculated with $L_{\text{c}} = \frac{1}{4\pi^2 f_{\text{res}}^2 C_{\text{c}}}$. From the decay of the voltage the parasitic resistance R_{c} can be calculated with $R_{\text{c}} = -2\psi\sqrt{L_{\text{c}}/C_{\text{c}}}$. ψ is the damping factor $\psi = \frac{-\ln(A/A_0)}{\omega t}$ where A_0 is the oscillation amplitude at the time $t = 0$, A the amplitude at time t and $\omega = 2\pi f$.

Table 6.3: Comparison of sample capacitors

Type		Cap1	Cap2	Cap3	Cap4	Cap 5
capacitance	µF	25	25	25	30	35
tolerance	%	±10%	±10%	±10%	±10%	±10%
voltage	V	1500	1300	1100	1100	1100
parasitic inductance	nH	28	30.6	31.1	39.4	35.5
parasitic resistance	Ω	0.32	0.27	0.22	0.28	0.26
energy density	J/cm^3	0.274	0.212	0.166	0.182	0.212
dimensions h x w x l	mm	35x49x70	50x35x57	55x40x41.5	50x35x57	50x35x57

The results are shown in Tab. 6.3 and presented in [110]. The preferred capacitor, for its low inductance and relatively high voltage rating and energy density, is labelled „Cap1“. Another argument in favour of Cap1 was the relatively small height of 35 mm.

6.4 Diode

During normal operation the free wheeling diodes serve as current path for the magnetizing current and the discharging current of the parasitic capacitance after the pulse is switched off. The voltage rating should be at least as high as the voltage rating of the MOSFET. PSpice simulations showed that the current flowing through the diodes after switch off reaches a peak of over 620 A per layer for the FCC prototype IA. This current was found in the uppermost layer of the IA stack. The current peak is less for the IA layers below as described in chapter 4.3.2. In case the layer is not triggered the diodes have to carry the full output current of the IA. Since the output current of the FCC prototype IA (2.4 kA) is significantly higher than the free wheeling current and the discharging current of the parasitic capacitance, the diode should be designed to carry the output current of the IA. To ensure such a high current, each branch should be equipped with 2 diodes of a pulse current capability of at least 100 A each. In this way a margin of about 100 % is achieved. Several Si and SiC diodes with a rated voltage of 1.2 kV and a pulse current of over 100 A are available on the market and can be used. Examples for diodes suitable for use in the prototype IA can be found in the references [39, 62]. However, PSpice simulations showed that for an IA with many layers (> 30) and low impedance ($< 10\ \Omega$) the discharging current of the parasitic capacitance can reach kA while the magnetizing current, depending on the used magnetic material, reaches ~ 100 A. For such an IA the discharging current of the parasitic capacitance and the free wheeling current can be higher than the load current and the diodes need to be rated to conduct the highest current that can occur.

6.5 Printed circuit board

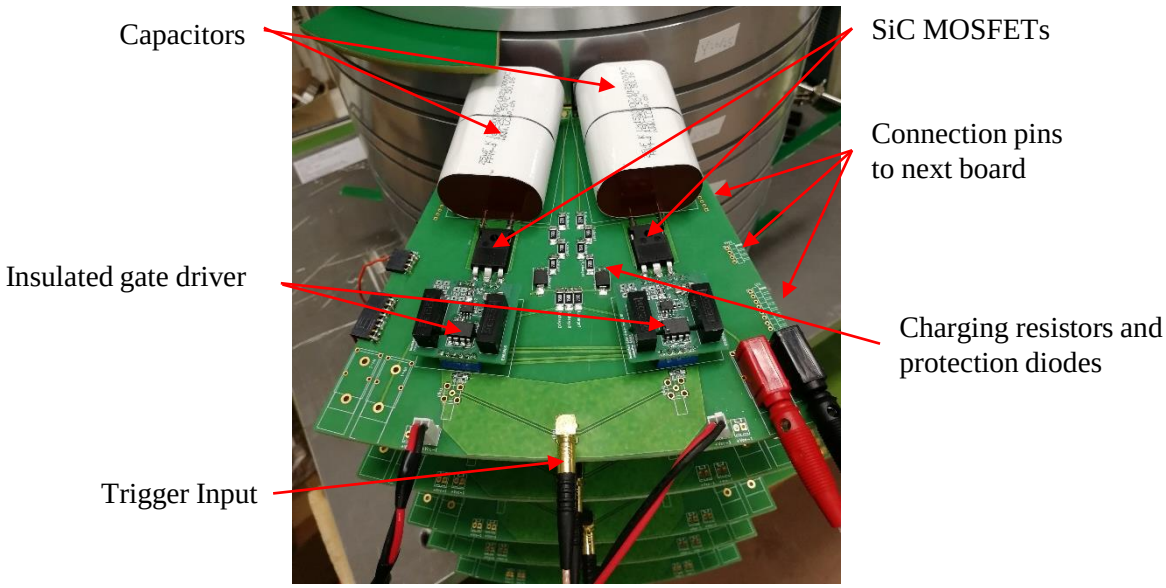

Figure 6.7: PCB for the inductive adder prototype

The printed circuit board (PCB) is designed to carry all main components and supply them with power. One circuit board carries two branches, each with a MOSFET, insulating gate driver, capacitor and free

wheeling diodes. The board is also equipped with the trigger input, high voltage charging circuit and provides the low voltage for the driver circuit. To build a 24 branch layer, 12 PCBs need to be connected along the outer circumference of the IA. Therefore connecting pins and sockets on the sides of the PCB are necessary. The decision of two parallel branches per PCB was made as a trade of between high modularity and low manufacturing costs. The CLIC prototype [55] is designed with two large PCBs in each layer what leads to high manufacturing costs and can cause problems with the synchronous distribution of the trigger signal. Smaller PCBs are cheaper to manufacture but require an increased effort with connections between PCBs and trigger cables. The mechanical stability of the PCBs in one layer is only given by the stability of the PCB itself, therefore the PCBs are produced with a thickness of 3.2 mm. The parasitic inductance of the primary circuit should be kept as small as possible, which requires an adequate PCB design with tight component placement and wide tracks between the components and the return current path on the underside of the PCB. Figure 6.7 shows the PCB designed for the IA prototype with capacitors, MOSFETs, insulating gate driver and connections.

7 Assembly of the prototype

This section describes the assembly of the hardware components of the IA prototype. The prototype was first assembled as a small scale version with 10 layers and a height of ca. 45 cm to conduct initial measurements. Supported by the findings of the first analysis, the 22 layer prototype was built. All components were manufactured by various external suppliers and ordered to CERN. The components of the stalk were brazed by a specialised workshop at CERN. The first revisions of the PCB were hand soldered by the author, in later versions the major part of small components were assembled by the manufacturer. Soldering of bigger PCB components (capacitors, MOSFETs, diodes, etc.) and the assemlbling of the IA structure was conducted by the author.

7.1 Transformer stack

In the first step the magnetic core was insulated on its outside to prevent short-circuits between the magnetic tapes of the tape wound core and the core housing. The insulated core is then placed between the two aluminum parts of the housing, which are fixed together with screws near the inner circumference, as shown in Fig. 7.1. An O-ring is placed in a groove between the aluminum parts to prevent oil flowing out

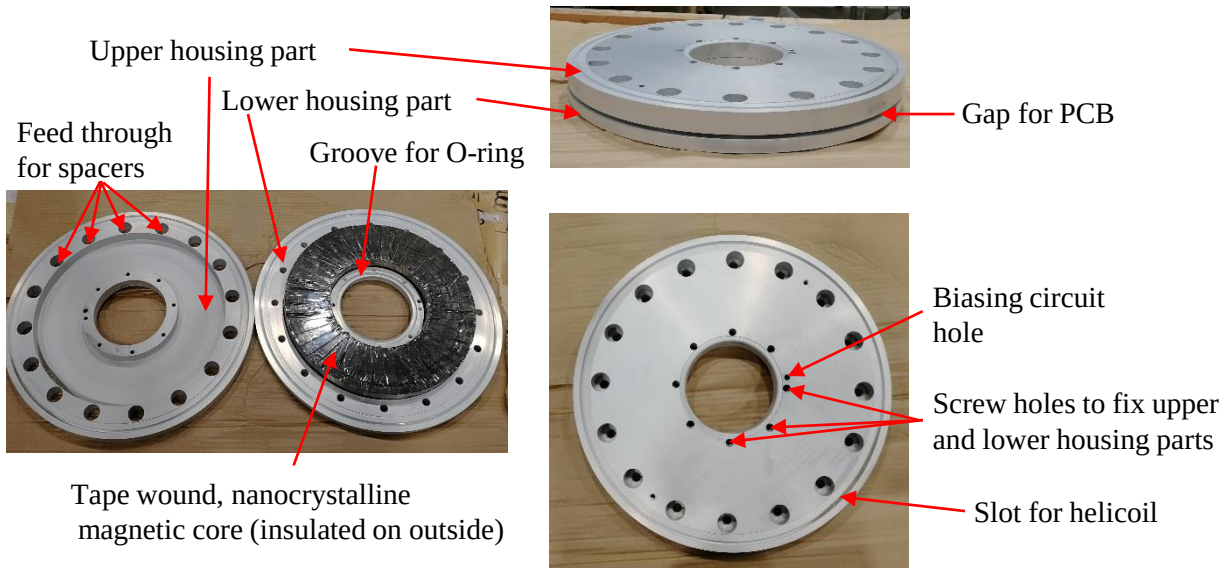

Figure 7.1: Assembly of the two housing parts (primary winding) and the insulated, nanocrystalline tape wound core

of the insulation gap. The two aluminum parts form the primary winding of each layer by totally enclosing the core and are electrically in good contact at their inner circumference. On the outer circumference, a gap is present in which later on the PCB is inserted to close the primary circuit. Figure 7.1 shows the assembly of the housing parts and the insulated magnetic core.

As a next step the pre-assembled layers are stacked upon each other, separated by spacers to prevent the grounded part of one layer touching the upper (high voltage) part of the layer below. The spacers pass through holes inside the upper aluminum housing of a layer and provide electrical contact between the two lower aluminum housings, which are at ground potential. Between two layers an O-ring needs to be inserted to prevent the insulation oil from leaking out. The O-ring is kept in place by a support ring (Fig. 7.2). The stalk passes through the center of the stack and is kept in place by one ceramic insulator at each end. Due to the mechanical strength of the stalk there are no additional spacers required to keep the stalk in place. On the lower end of the IA the stalk is connected to the ground part of the first layer. The connection is done with an oil tight feed through. With the stalk centered, the insulation between the primary windings and the stalk is 2.4 mm. Figure 7.2 shows the assembly steps of the stack. At the top

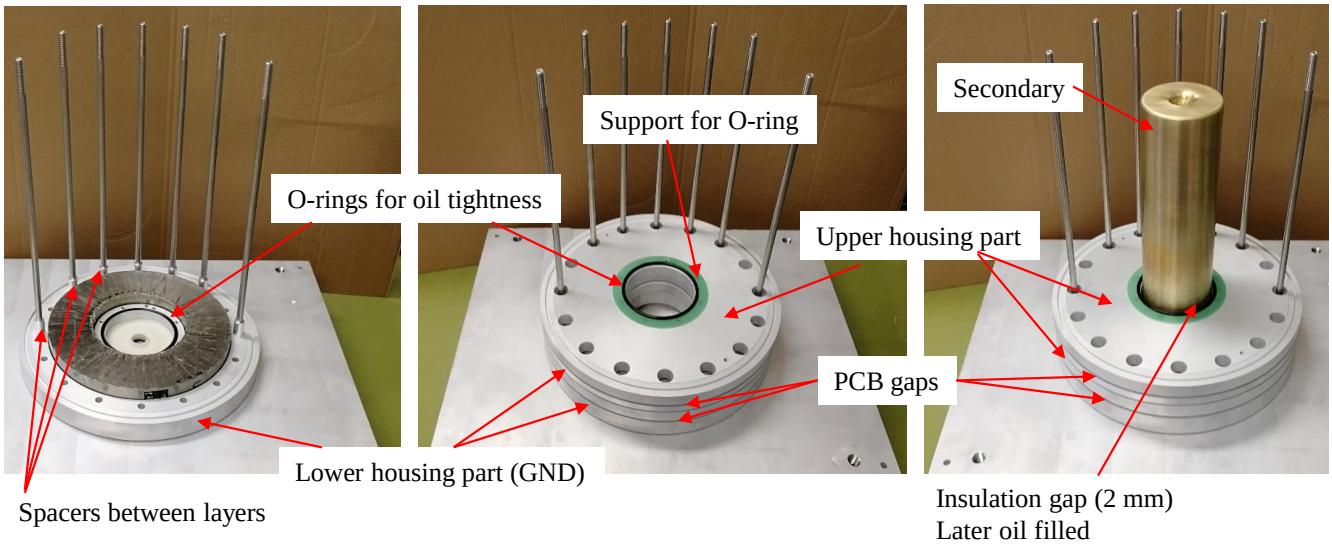

Figure 7.2: Assembly of the stack consisting of the pre-mounted layers and the stalk

of the stack a grounded aluminum plate closes the oil compartment: a feed through for the high voltage output is mounted on this plate. Depending on if the output is connected on the bottom or top of the stack a positive or negative voltage pulse can be generated. The other end of the stalk is then connected to ground.

Insulation breakdown tests

After the 10 layer prototype was successfully assembled a partial discharge measurement was carried out to test the electric strength of the insulation. For this purpose the short-circuit at the lower end of the IA was replaced with an open circuit. A high voltage transformer and a partial discharge measurement device were connected to the high voltage output of the IA. Figure 7.3 shows the test setup for the partial discharge and break down measurements on the 10 layer prototype. More information about partial discharge measurements can be found in [15, 93]. The measurements were conducted with a 50 Hz AC voltage and

all values reported from the partial discharge measurement are peak values. Besides information regarding partial discharges in the insulation of the IA, the breakdown voltage can also be measured. During the measurements with the stalk for the $6.25\ \Omega$ oil insulated prototype, no partial discharge inception voltage could be measured in the oil, before the breakdown voltage was reached. This could be due to the small insulation gap where the electric field can be considered homogeneous. All partial discharges observed on the $6.25\ \Omega$ prototype could be shown to occur in cables or feed through. For air as insulation medium the breakdown voltage was measured to be at about 7.5 kV.

Considering a typical value of 2.5 kV/mm as the breakdown field strength of air a theoretical breakdown voltage of 4.9 kV was calculated. The measured breakdown voltage of 7.5 kV is 53 % higher than the calculated value. Nevertheless, the breakdown field strength of air depends on several parameters such as humidity, pressure and temperature. Paschen's law describes the dependency of the break down voltage in gas on the product of pressure and gap size in a homogenious field. Using Paschen's law as described in [15] a breakdown voltage of about 8 kV is predicted. The measured 7.5 kV is 94 % of the 8 kV from Paschen's law.

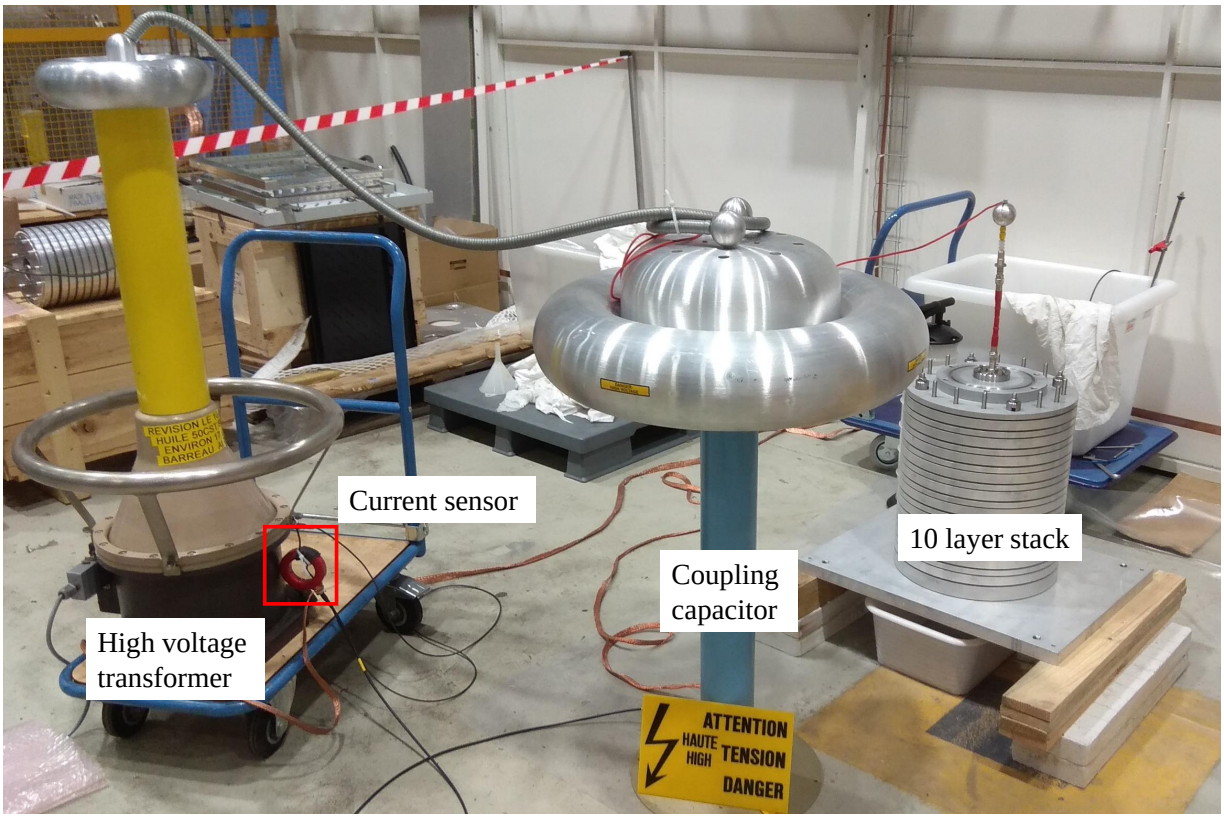

Figure 7.3: Test setup for the partial discharge and breakthrough measurements on the 10 layer stack in a HV laboratory of building 867 at CERN

After the measurements on the air insulated IA the insulation gap was filled with oil. To avoid introducing air bubbles in the oil, which would reduce the insulating properties significantly, the oil was filled up from the bottom of the stack through a tube. After the insulation gap was filled with oil a breakdown voltage of 15 kV was measured. For oil, considering a typical value of 25 kV/mm breakdown field strength, the calculated breakdown voltage is 49 kV and the measured breakdown voltage of 15 kV is only 30 % of the

calculated value. The difference between the measured and calculated breakdown voltages can have several reasons. The geometry of the HV parts is not perfect, hence field enhancements might occur. In addition the gaps between the layers introduce an uneven structure in the outer cylinder surface, and therefore field enhancement, that reduces the breakdown voltage. However, the field enhancement hypothesis would be expected to also reduce the breakdown voltage with air insulation.

The different materials (oil, aluminum, O-ring) cause triple-points that can also give field enhancements. However, the O-ring triple point would also apply to an air insulation. The difference in percentage of the calculated breakdown voltage between air and oil has also been observed in other applications at CERN. Especially a relatively small insulation gap is reported to cause a reduction of the insulation properties of oil. Other explanations for a lower breakdown voltage could be impurities in the oil such as small metallic pieces, dust or air bubbles. In several applications with oil insulation a vacuum is used to remove air bubbles. This means could not be applied for the oil insulation of the IA. Also a misaligned stalk in the stack would be expected to cause the breakdown voltage to reduce, especially in case of small insulation distances, as is the case for the $6.25\ \Omega$ prototype.

With a stalk with a diameter of 70 mm, which corresponds to an impedance of $25\ \Omega$, the breakdown voltage with air as insulation material was measured to be 55 kV. Based on 2.5 kV/mm the calculated breakdown voltage of the air insulated setup is 38 kV, the measured value of 55 kV is 45 % higher. Paschen's law gives a breakdown voltage of about 60 kV for the $25\ \Omega$ setup. The measured 55 kV is 92 % of the 60 kV from Paschen's law. Even if the electric field is not as homogeneous as in the $6.25\ \Omega$ setup, Paschen's law predicts the breakdown voltage within 10 % of the actual value. The breakdown test for the $25\ \Omega$ setup was not repeated with oil insulation since the calculated breakdown voltage of 380 kV could cause damages to the prototype in case of a breakdown. In literature it can be found that for standardized surge voltage measurements the breakdown voltage in oil can be estimated to be two to three times higher compared to AC breakdown tests [70]. Considering a breakdown voltage of twice the AC breakdown values, the measured values of the $6.25\ \Omega$ prototype would be sufficient for the planned output voltage of 15 kV including a margin. Table 7.1 summarises the measurement results of the breakdown tests.

Table 7.1: Calculated and measured breakdown voltage V_{bd} of the IA insulation with air or oil

impedance in Ω	6.25	6.25	25	25
insulation material	air	oil	air	oil
calc. AC V_{bd} in kV	4.9	49	38	380
$V_{\text{bd,Paschen}}$ in kV	8.0	-	60	-
meas. AC V_{bd} in kV	7.5	15	55	-
est. pulse V_{bd} in kV	15	30	110	-

7.2 Printed circuit boards (PCBs)

The primary circuit consists of the transformer core with the primary winding and a PCB that carries the pulse capacitors, MOSFETs, free wheeling diodes, and all electronics and remaining hardware necessary to operate the circuit such as e.g. the insulating gate driver circuit. The primary circuit obtains power from low and high voltage supplies. In addition, the primary contains a charging circuit with charging resistors and diodes, trigger line, and connection plugs. The PCB is connected to the primary winding by

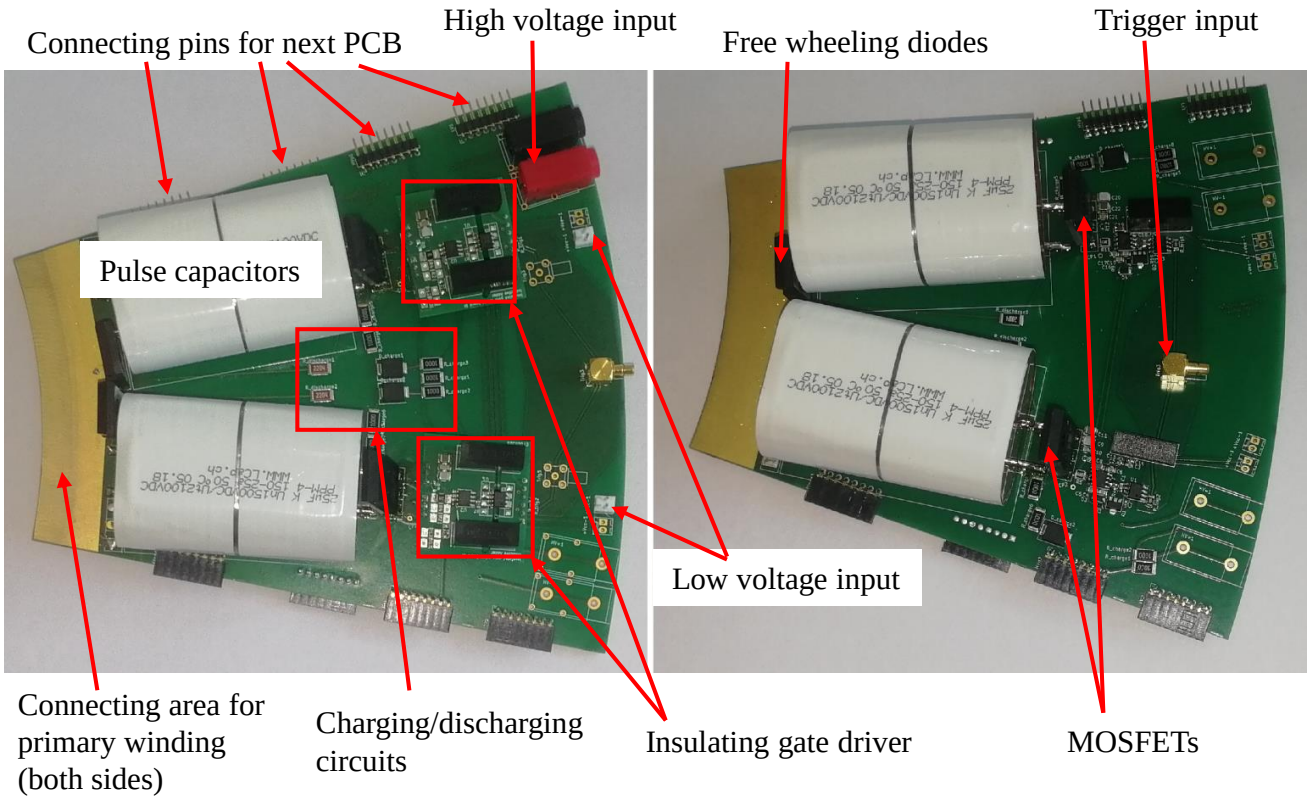

Figure 7.4: The PCB with two parallel branches of the primary circuit with the insulating gate driver on separate PCBs (left) and on the main PCB (right)

inserting it in the gap between the top and bottom parts of the housing shown in Fig. 7.1. The electric connection is realised with helicoils that are inserted in a slot along the outer circumference of both core housing parts (Fig. 7.1) and press on the copper connection area of the PCB from both sides - this provides a high quality electrical connection suitable for the high-frequency components of the pulse current. The number of branches per PCB has been studied. Two branches per PCB was selected as the best trade off between manufacturing costs, modularity and practicability. The PCBs can be connected to further PCBs to increase the number of branches per layer. The maximum amount of PCBs for one layer is 12, which results in 24 parallel branches. In this case the outer circumference of the housing is fully equipped with PCBs. The design of the PCB was revised several times during the development process. The insulating gate driver circuit was initially placed on a separate PCB that could be plugged into the main PCB. This design made it possible to easily modify the gate driver circuit during testing. Later on the insulating gate driver circuit was implemented on the main PCB to reduce the parasitic inductance between the gate driver output and the MOSFET gate-source. Figure 7.4 shows two versions of the PCB with two parallel branches of the primary circuit. The gate driver circuit is based on a commercially available insulating gate driver circuit from Wolfspeed [38]. The original 9 A gate driver chip was replaced by one with 14 A [63] and the gate resistor was reduced to $2.4\ \Omega$ to achieve faster turn-on of the MOSFET. To improve the parallel operation capabilities of the gate driver circuit, the opto-isolator of the original board was replaced by a digital isolator [95] with lower propagation delay and reduced jitter.

The charging circuit of the PCB connects the high voltage DC input pins with the high voltage side of the capacitor of each branch. To limit the peak current, especially when each MOSFET is in the on-state

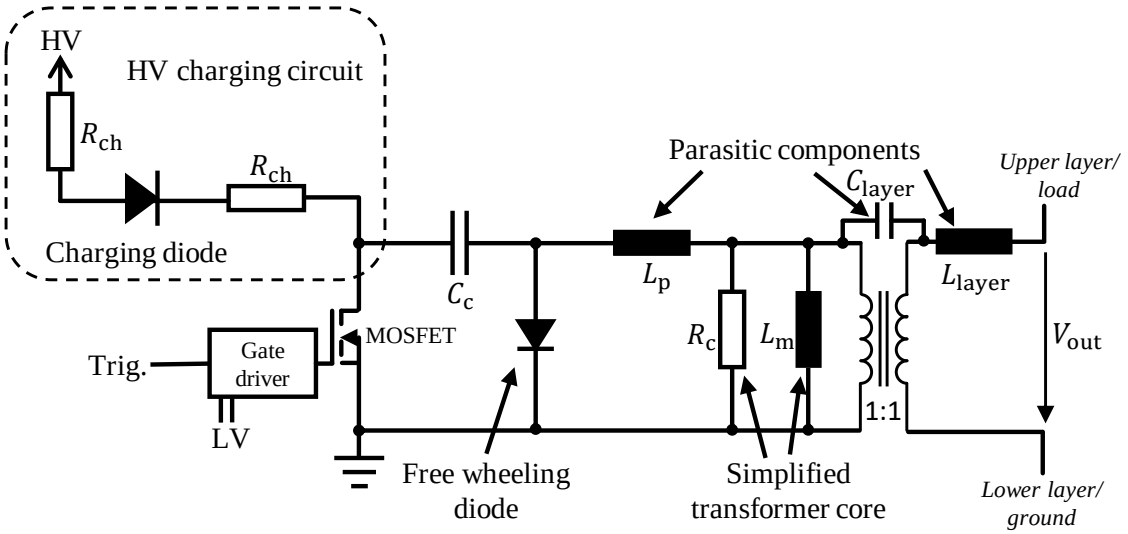

Figure 7.5: Schematic of one IA layer including charging resistors and diode for one branch

(see below), several series resistors are placed in the charging circuit. In addition, to avoid all branches discharging into a short-circuit of another, parallel, branch or into the charging circuit there is also a diode placed in each charging path (Fig. 7.5). In case of a fault, the gate driver circuit includes high voltage insulation from the trigger line and DC supply voltage of the gate driver. This insulation is realised by a digital isolator and insulating voltage regulators. The MOSFET gate is driven with 20 V and -5 V to ensure fast switching times, safe turn-off and low on-state resistance. The used gate driver is capable of a maximum output current of 14 A. The schematic of one IA layer with the components of the charging circuit for one branch is shown in Fig. 7.5. The low voltage power for the gate drivers is provided by insulating voltage regulators. The output voltage of the regulators depends on the input voltage level. In this way the turn-on and turn-off voltage of the gate driver can be fine tuned by adjusting the voltage of the power supply. To take advantage of each layer of the IA being connected to ground, the source pin of each MOSFET is connected to the local ground and the pulse capacitor is connected to the drain pin and the upper core housing of the primary winding, as shown in Fig. 7.5. During the charging time, when the MOSFET is off, the capacitor is connected to ground via the primary winding and to the high voltage of the DC supply on the other side, as shown in Fig. 7.5. When the MOSFET is triggered, the high voltage side of the capacitor is connected to ground by the MOSFET. As a result the former ground potential of the other capacitor pin has now the potential of the negative charging voltage, which is therefore applied to the primary winding of the transformer. The charging power supply is connected to ground, via the charging resistors, during the pulse due to the on-state MOSFET. The voltage applied to the primary winding is negative and generates a negative voltage at the output of the IA. The output voltage polarity can be chosen depending on which end of the IA the output cable is connected: the opposite end of the stack is typically grounded.

7.3 Full-scale prototype assembly

After the assembly of the stack, the cable for the biasing circuit is placed through its designated hole (shown in Fig. 7.1). The cable should be insulated according to the output voltage of the IA since the voltage

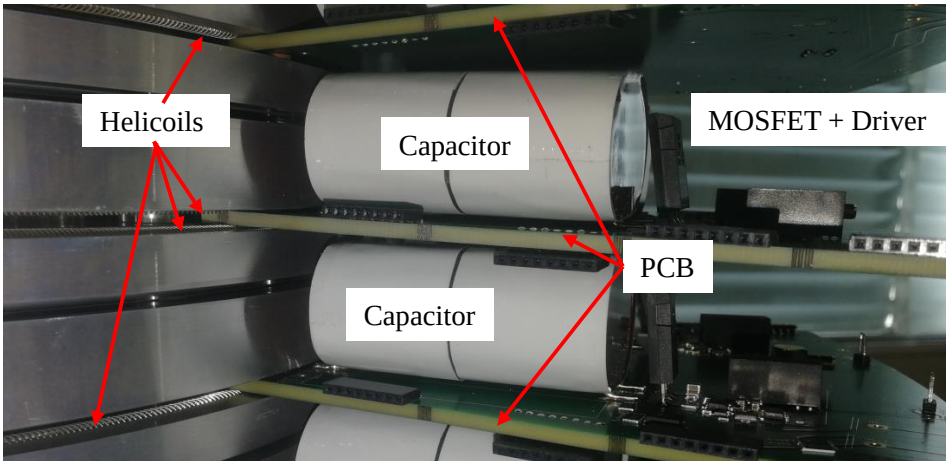

Figure 7.6: Connection of the PCBs to the primary winding with helicoils (canted coil springs)

induced in the cable of the biasing circuit is as high as the IA output voltage. As described in chapter 3.4.2, an inductance is connected in series with the biasing circuit and the current source equipped with a free wheeling diode (schematic shown in Fig. 3.4.2). As a next step, the PCBs with the primary circuits can be plugged into the gaps of the primary winding. The connection to the PCBs is realised by helicoils (canted coil springs [4]) as shown in Fig. 7.6. Depending on the measurements planned, the appropriate number of layers are equipped with PCBs to reach the required output voltage. The number of parallel branches can be adjusted by adding PCBs in each layer. The number of branches must be at least high enough to provide the output current required by the output voltage and load to avoid damaging the MOSFETs. Modifications on the circuit of each layer or replacement of broken PCBs is less effort compared with PCBs carrying a large number of parallel branches. Figure 7.7 shows the test bench with the 10 layer prototype

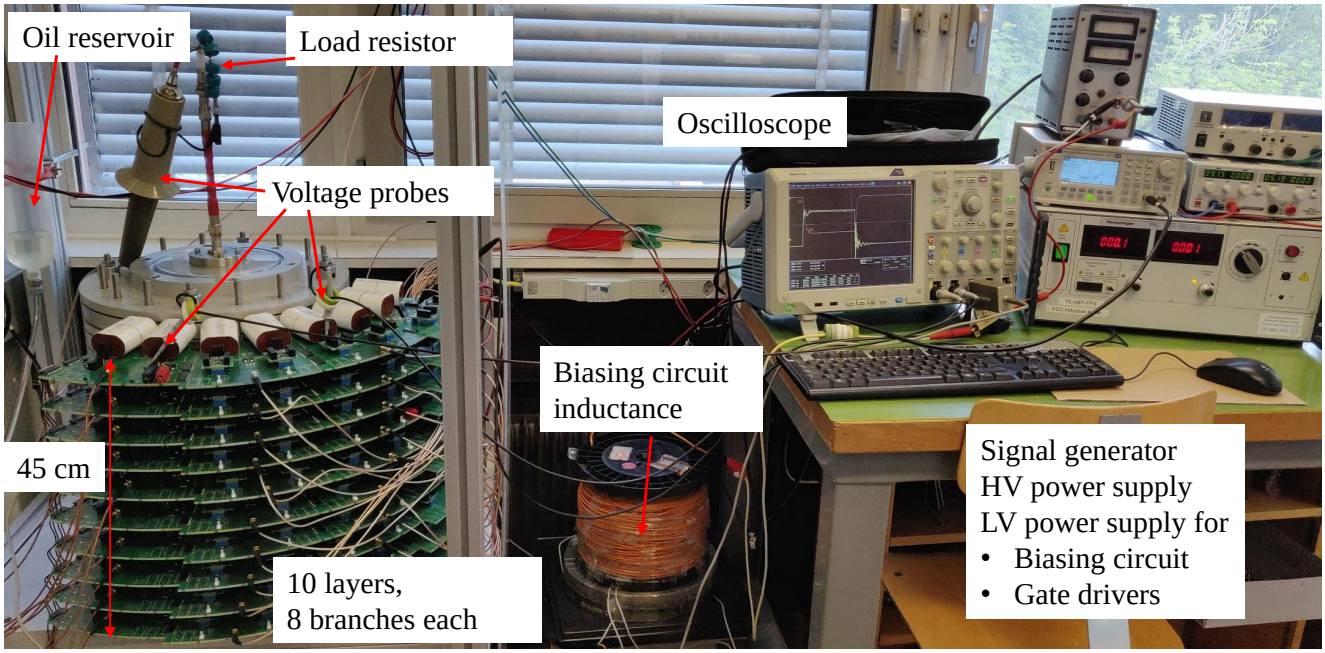

Figure 7.7: Test bench of the 10 layer prototype equipped with 4 PCBs (8 branches) in each layer

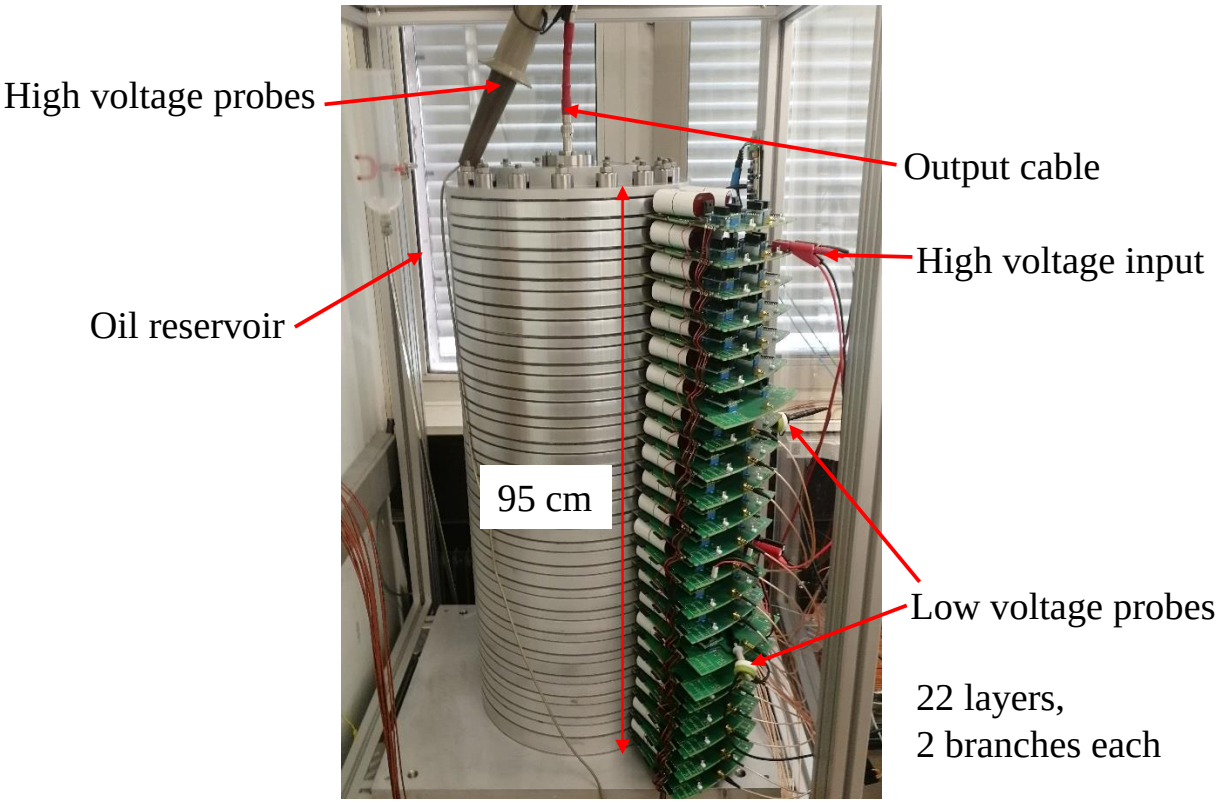

Figure 7.8: The 22 layer prototype IA equipped with one PCB in each layer

equipped with 4 PCBs (8 branches) in each layer. The test bench is also equipped with power supplies for high and low voltage, the components of the biasing ciruit, an oscilloscope and an oil reservoir for the oil insulation. The prototype with 22 layers is assembled in the same way as the 10 layer prototype and is shown in Fig. 7.8.

7.3.1 Expected manufacturing tolerances

The small insulation gap between the primary and secondary winding of approximately 2 mm, for the $6.25\ \Omega$ IA, raises concerns in terms of acceptable tolerances during manufacturing and assembly. As presented by the author in [11] the impedance could be influenced by the manufacturing tolerances of the hardware.

Figure 7.9 shows the influence of a manufacturing error, in either the outer diameter of the insulation (Error in d_o) or the inner diameter of the insulation (Error in d_i), upon the characteristic impedance Z and the maximum electrical field E_max, for an oil insulated IA. It is desirable that E_max is below 10 kV/mm: Hence, the design could be specified for a lower electric field and/or the manufacturing tolerances specified appropriately, e.g., +0, -X mm for the inner insulation diameter d_i and +0, +X mm for the outer insulation diameter d_o. To avoid confusion, it should be mentioned here that the parameters d_i and d_o are defined differently in [11]. It is considered feasible to readily machine the stalk and core housing with a tolerance better than 0.1 mm. As a worst case, considering a -0.1 mm (-0.15 %) error in the outside diameter of the stalk, with respect to nominal reduces the maximum electric field from 10 to 9.7 kV/mm (~ 3 %)

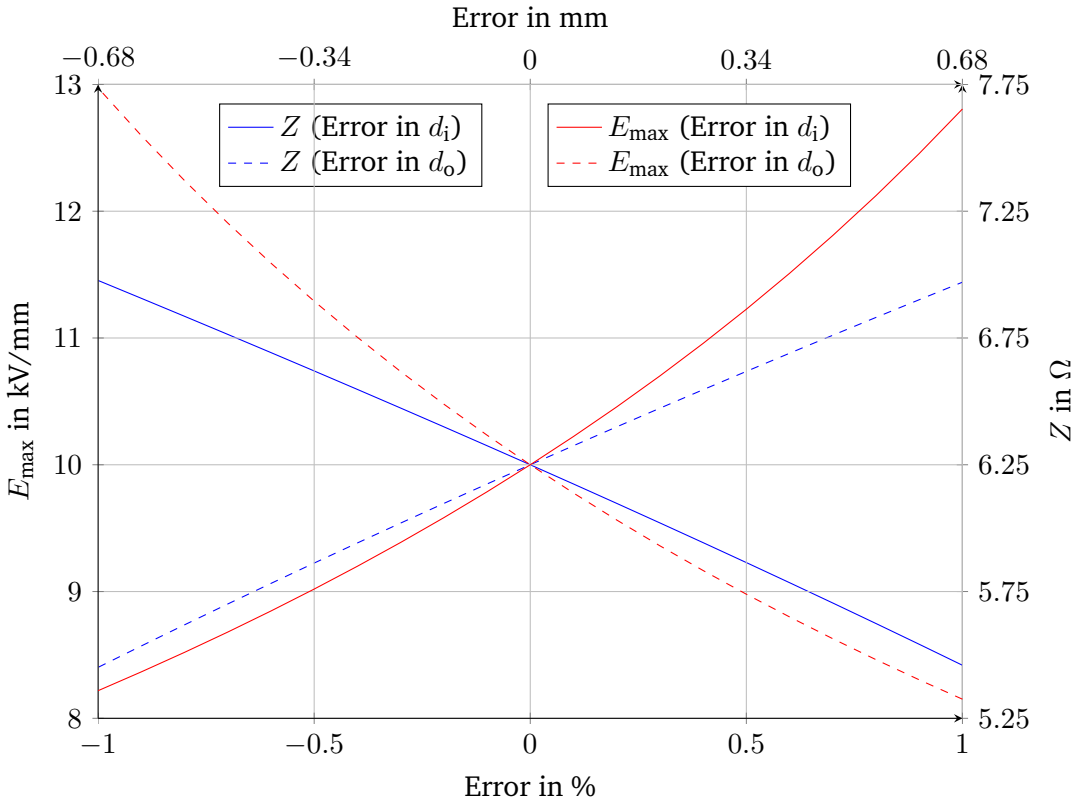

Figure 7.9: Calculated influence of a manufacturing error of the inner (d_i) or outer (d_o) diameter of the insulation

and increases the output impedance from $6.25\ \Omega$ to $\sim 6.36\ \Omega$ (~ 1.8 %). During assembly, particular attention must be paid to ensure that the stalk and core housing are as concentric as possible, to minimize an increase in field strength with respect to nominal. A maximum concentricity error of ± 0.1 mm is expected.

Voltage output: Initially the IA was designed in a way that either a single or eight parallel coaxial cables could be connected to the output of the IA. During the measurements it turned out that the impedance

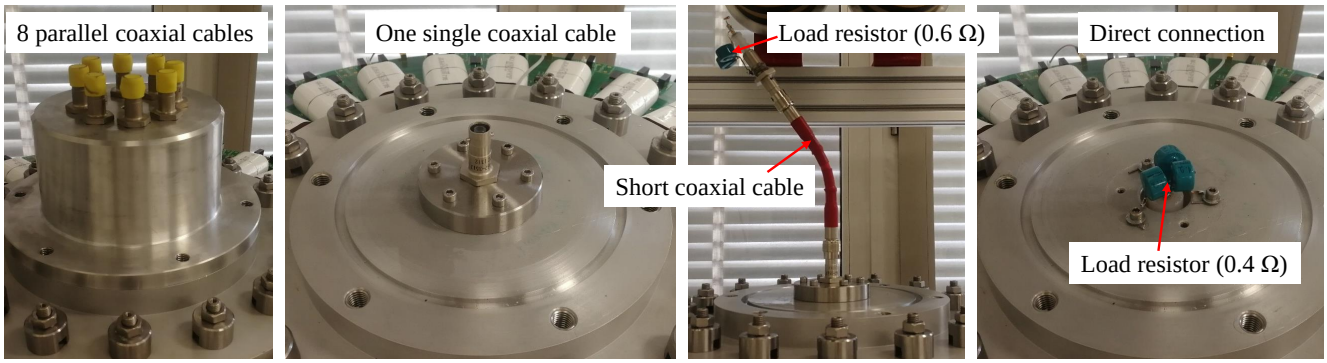

Figure 7.10: Connection of the load resistor to the output of the IA

mismatch of the cable connector and the inductance introduced by a short-cable leading to the load resistor caused the rise time of the pulse to be increased. This occurred especially for very low load resistor values, which are necessary for high current measurements of only one layer, as the L/R time constant increases. As a first attempt to reduce inductance, the short-cable connecting the load resistor was removed and the load resistor was soldered as close as possible to the IA stalk. Figure 7.10 shows the output of the IA with 8 parallel coaxial connectors, a single coaxial connector, the load connected via a short-coaxial cable and the load resistor connected directly on the IA output. Hence a significantly faster pulse rise time of the output voltage could be obtained. The IA output connector needs to be well designed to have minimal impedance mismatch. Also the short-circuit end of the IA needs to be designed without introducing significant additional inductance.

8 Measurements on the prototype

After the assembly of the 10 layer prototype and the filling of the oil first measurements were conducted [111]. All measurements were conducted with a biasing current of 0.7 A to preset the magnetic field in the cores as described in chapter 6.1. The output voltage of the gate driver was set to 20 V for on- and -5 V for off-state. The pulse length was set to 2 µs. The functionality of the PCBs was tested up to 1.1 kV. All measurements were conducted with a Tektronix DPO5034 oscilloscope with 350 MHz bandwidth and 5 GS/s. Voltages up to 400 V were measured with a 500 MHz voltage probe, up to 4 kV with a 200 MHz voltage probe and up to 20 kV with a 75 MHz voltage probe. The 10 layer prototype was upgraded to the 22 layer prototype and a network analyzer was used to measure the inductance for the PSpice model. Due to the measurement setup the output voltage of the IA is negative. In some plots the polarity of the output voltage was mathematically reversed to show a positive pulse. In the following the measurement results with the network analyzer are presented followed by the measurements on a single layer of the IA up to the rated current of 2.4 kA, measurements on the 10 layer prototype and measurements on the 22 layer prototype.

8.1 Network analyzer measurements

The inductance of the IA stack and the PCBs was calculated from the scattering parameters measured with a network analyzer [83]. From the scattering parameter S_{11}, from a one port measurement, the impedance of the system Z can be calculated with:

$$Z = \frac{1 + S_{11}}{1 - S_{11}} \cdot Z_0, \tag{8.1}$$

where Z_0 is the source impedance of the network analyzer ($50\ \Omega$). From the impedance the inductance can be calculated by separating the real and imaginary parts:

$$Z = R + jX_\mathrm{L},\ L = \frac{X_\mathrm{L}}{2\pi f}. \tag{8.2}$$

The used network analyzer was an E5071C from Agilent Technologies: the E5071C was used to calculate the inductance value directly from the measured scattering parameters. More information about network analyzer measurements can be found in [83].

The inductance of a PCB with two parallel branches was measured by connecting the network analyzer to the copper connectors that usually plug in the core housing of the IA layer. With a short-circuit directly at the card an inductance of 14 nH was measured for the connector. The connector to the PCB is shown in Fig. 8.1. The drain-source pins of the MOSFETs were short-circuited to be able to measure the inductance

of the PCB current loop. The inductance measured was 25.3 nH, considering 14 nH for the connector to the PCB, the inductance of one PCB (two parallel branches) is 11 nH. Measurements on a PCB with one single branch resulted in 36 nH, reduced by the inductance of the connector the inductance of one branch was measured as 22 nH, confirming the measurements on one PCB with two parallel branches. Based on the measurements conducted on the pulse capacitors resulting in an inductance of 28 nH for only the capacitor, the measurement results with the network analyzer seem too low. The measurement differences might be caused by neglecting the inductance in the circuit while measuring the inductance of the capacitor as described in chapter 6. However, the measured values are reasonable and measurement tolerances need to be taken into account.

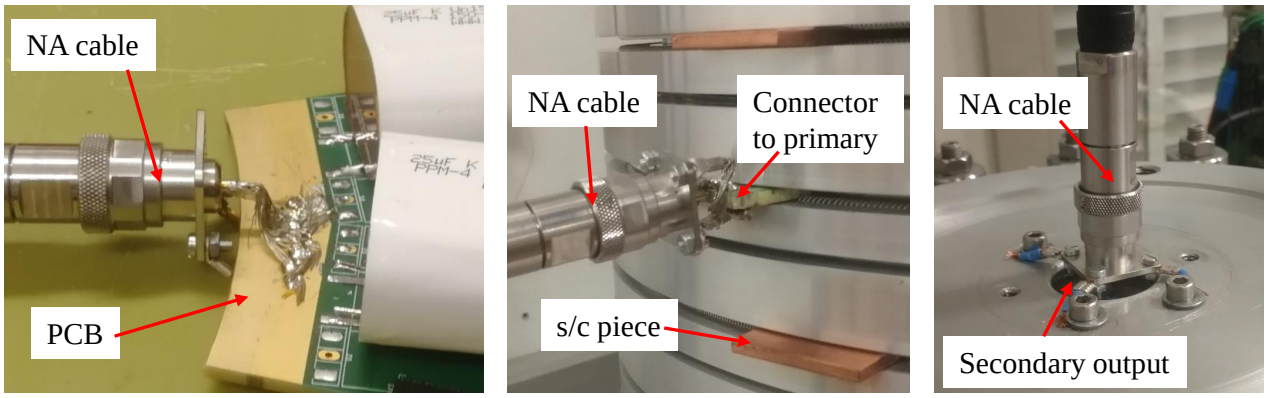

Figure 8.1: Connection of the network analyzer (NA) cable to the PCB (left), primary (middle) and secondary (right) of the IA

The inductance of the stack was measured by putting the secondary in short-circuit on the output of the IA. The primary winding of all layers were put to short-circuit except for one layer that has been connected to the network analyzer as shown in Fig. 8.1. The inductance measured in this setup was independent from the layer connected to the network analyzer and resulted in about 104 nH at 200 kHz and 94 nH at 2 MHz. The connector of the network analyzer to one of the layers is shown in Fig. 8.1, its inductance was measured to be 14 nH what results in an inductance of $80 - 90$ nH measured at the primary. The measurements were confirmed by connecting the network analyzer to the secondary output of the IA as shown in Fig. 8.1 and putting all primaries in short-circuit with four copper pieces creating the short-circuit in each layer. The copper pieces to put the layers in short-circuit (s/c piece) are also shown in Fig. 8.1. The measured inductance for this setup was 90 nH at 200 kHz and 81 nH at 2 MHz. If the number of short-circuit copper pieces of one layer was reduced to one piece in one single layer, the measured inductance increased to 94 nH at 200 kHz and 85 nH at 2 MHz. Hence the increase of inductance of one layer equipped with several PCBs spread around the circumference to only one PCB is around 4 nH. Figure 8.1 shows the connection of the network analyzer to the PCB, the primary and the secondary of the IA.

Table 8.1: Results of the inductance measurements with a network analyzer

Position	Unit	Value
PCB with two branches (MOSFETs in s/c)	nH	11
PCB with one branch (MOSFET in s/c)	nH	22
IA stack from primary (other primaries and secondary in s/c)	nH	80-90
IA stack from secondary (all layers with 4 s/c piece)	nH	81-90
IA stack from secondary (one layer with 1 s/c piece)	nH	85-94

Based on the described measurements the inductance introduced by the secondary circuit of the IA can be estimated to be $80 - 90$ nH. This inductance includes the inductance introduced by the layers and by the ends of the stalk. Table 8.1 summarizes the measurement results with the network analyzer.

As shown in chapter 4.2 the analytically calculated inductance of one layer is $L_{\text{layer}} = 348$ pH. Therefore the inductance added to the stack by both ends of the stalk can be estimated as $80\text{ nH} - 22 \cdot 0.35\text{ nH} = 72.3$ nH. An inductance of 36 nH was added on both sides of the IA stack in the PSpice model for better comparison of the simulated and measured waveforms.

8.2 Measurements on a single IA layer

For the measurements on a single IA layer the primary winding of all layers were short-circuited by adding solid copper pieces in the slots for the PCBs except for the first layer of the IA stack, which was equipped with PCBs. The gate-source voltage was set to -5 V for turn-off and 20 V for turn-on. The pulse capacitors were charged to 1 kV and the pulse duration was 2 µs.

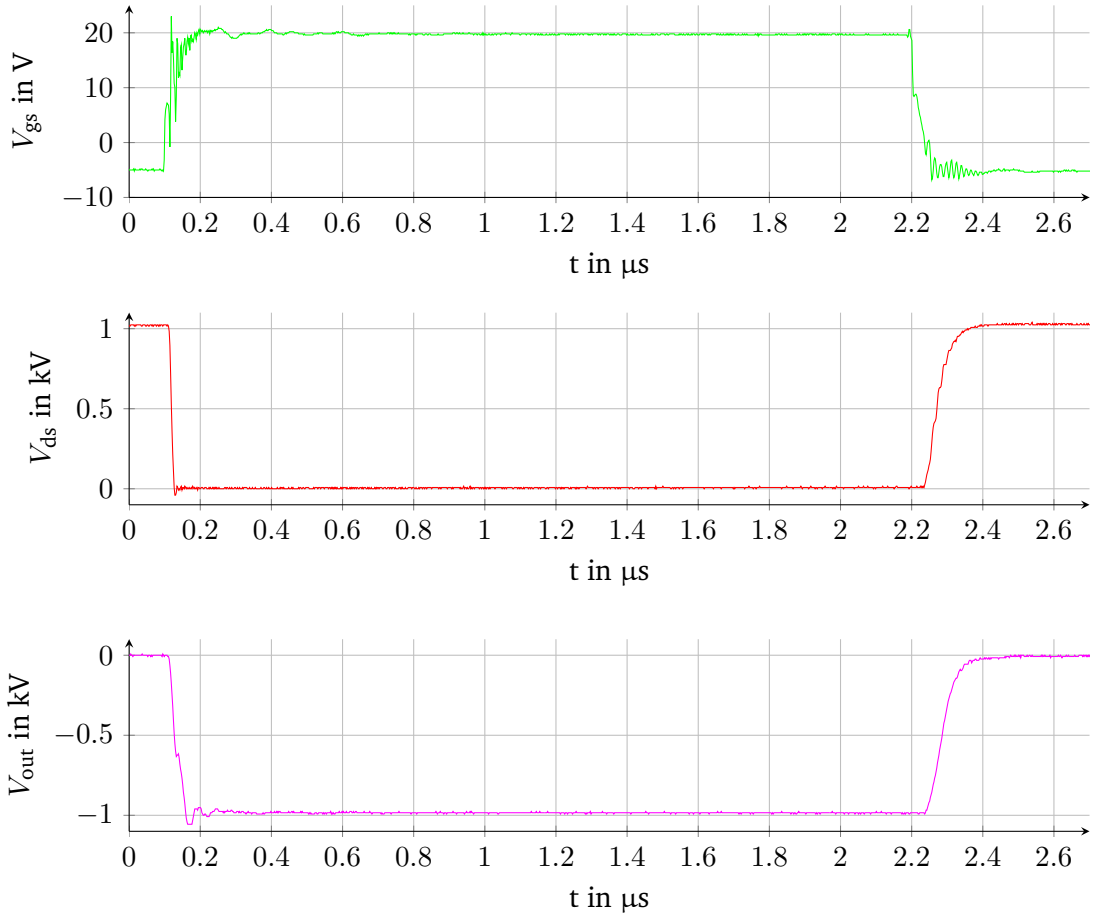

Figure 8.2: Example of measured gate-source (V_{gs}), drain-source (V_{ds}) and output (V_{out}) voltage waveforms in case of one layer with 24 branches and a load resistor of $6.25\ \Omega$

Figure 8.2 shows the gate-source (V_{gs}), drain-source (V_{ds}) and output (V_{out}) voltage waveform in case of one layer with 24 branches and a load resistor of $6.25\ \Omega$. The drain-source voltage is 1 kV prior to turn-on and close to 0 V following turn-on. The output voltage is approximately -1 kV following turn-on and 0 V following turn-off. The voltage difference between V_{ds} and V_{out} is caused by the voltage drop across the MOSFETs and across the short-circuited layers in the stack. The ripple of the gate-source voltage at turn-on and turn-off are acceptable and seem to have no negative influence on the MOSFET switching behaviour. With higher currents through the MOSFET the gate voltage ripples increase. However, for an output current of 2.4 kA the ripple had no negative effects on the MOSFET switching behaviour. From Fig. 8.2 it can be seen that the drain-source voltage rises faster than the output voltage of the IA. Reasons for the output voltage rising slower can be the inductance of the circuit and the propagation of the pulse wave through the stack. Each IA layer has been tested up to 1.1 kV and for a pulse length of up to 2.4 µs. To ensure that the magnetic cores are not saturating the magnetizing current was measured. All measurement results conducted at the single IA layer were according to the analytic calculations and simulations.

8.2.1 High current measurements on one layer

The setup with one layer in the IA was used to measure the rise time for different load resistors. In addition to the measurements the rise time was also calculated analytically and simulated with PSpice. The first PSpice simulations were conducted by modelling the MOSFET with a closing and opening switch in series.

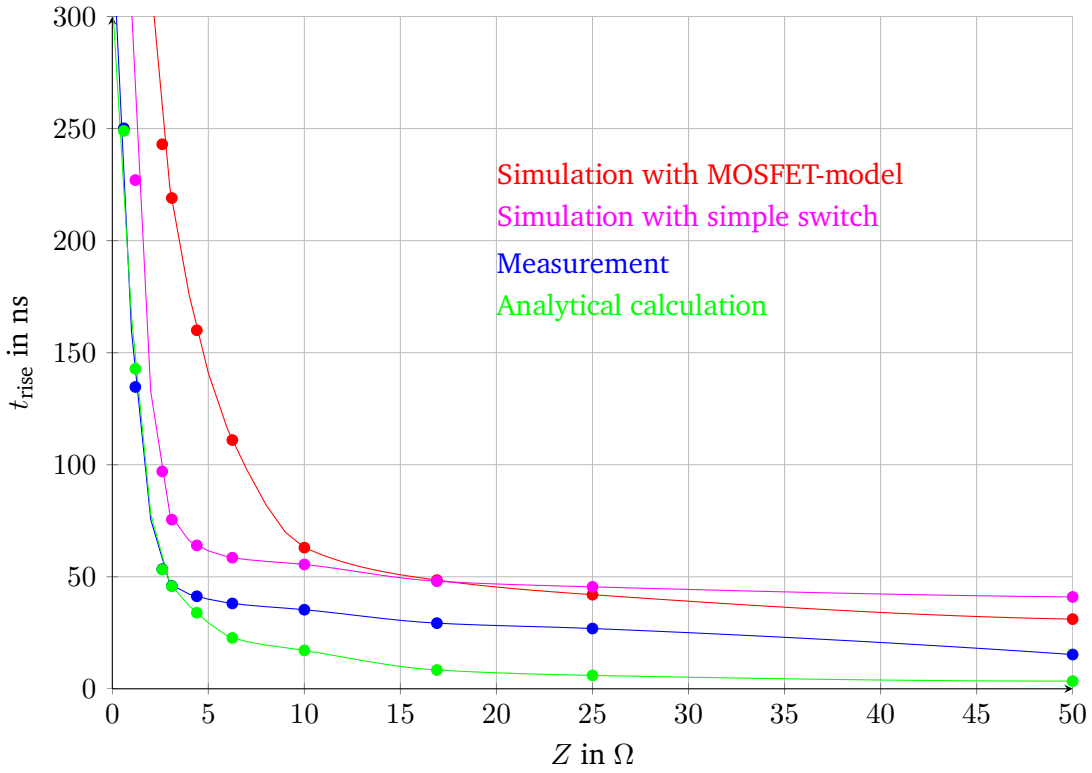

Figure 8.3: Measured, calculated and simulated rise times ($10\,\%$-$90\,\%$) of the output waveform with one layer for different load resistors

A second PSpice simulation was done with a MOSFET model provided by the manufacturer. Figure 8.3 shows the different curves for the rise time measured from 10 % to 90 %. As Fig. 8.3 shows, the analytical calculations result in the fastest rise times and can be considered the minimum possible, as they neglect switching time for the MOSFETs. The simulated rise times are significantly larger. The measured rise times are in between the calculated and simulated values. For high currents the measured rise times match well with the results of the analytical calculation. The simulated values for the PSpice model with the MOSFET model of the manufacturer are closer to the measured rise times for high load resistors and therefore lower current, whereas the simulations in which the MOSFET was simulated with simple switches match better for load resistors below 15 Ω and therefore higher currents.

8.3 Measurements on the 10 layer prototype

The influence of the primary inductance was characterised by measuring the output pulse with a fixed load resistor for a different number of parallel branches in the primary. Figure 8.4 shows the pulse rise time of the 10 layer prototype for a different number of branches in the primary. It can be observed

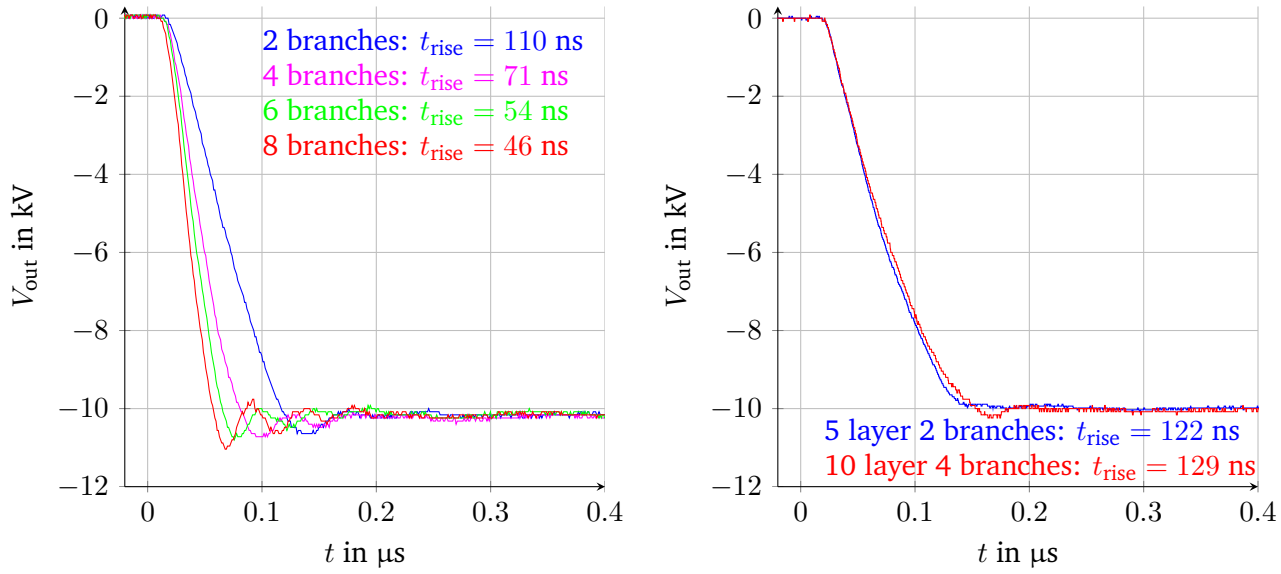

Figure 8.4: Left: output waveforms measured on the 10 layer prototype with a 50 Ω load and 2, 4, 6 and 8 parallel branches in the primary circuit. Right: output waveforms measured on the 22 layer prototype with a 16.9 Ω load with 5 layers and 2 branches each layer (blue, multiplied by 2 for comparison) and 10 layers with 4 branches each layer (red). All rise times are defined from 0.5 % to 99.5 %.

that the rise time of the output pulse is becoming smaller the more parallel branches are used. One effect causing the faster rise time could be the decreased parasitic inductance of the primary circuit when having more parallel branches. By connecting parallel branches to the layer the parasitic inductance of the primary circuit is also connected in parallel to other parasitic inductance of other branches and therefore reduced. By adding two additional branches to the first two branches the parasitic inductance is cut in half which causes a relatively big improvement of the rise time. The more parallel branches are used in the primary winding, the smaller is the impact of adding more branches. Another impact causing the faster

rise time is that the current load of one branch is reduced by adding more branches since the voltage is kept constant.

The second measurement in Fig. 8.4 shows two measurements: The blue curve shows the rise of a pulse generated with the 22 layer prototype, where the top 5 layers were equipped with one PCB each (2 branches), a load resistor of $16.9\ \Omega$ and a capacitor charging voltage of 1 kV in each layer. The red curve shows the rise of a pulse generated with the 22 layer prototype, where the top 10 layers were equipped with two PCBs each (4 branches), a load resistor of $16.9\ \Omega$ and a capacitor charging voltage of 1 kV in each layer. To compare the rise time of the two measurements, the output waveform of the measurement with 5 layers was multiplied by 2. In both measurements the current through each MOSFET is about 150 A and the drain-source voltage is 1 kV. The two waveforms show almost identical rise times with only 7 ns difference. The 10 layer IA is expected to have longer rise time, for a given current.

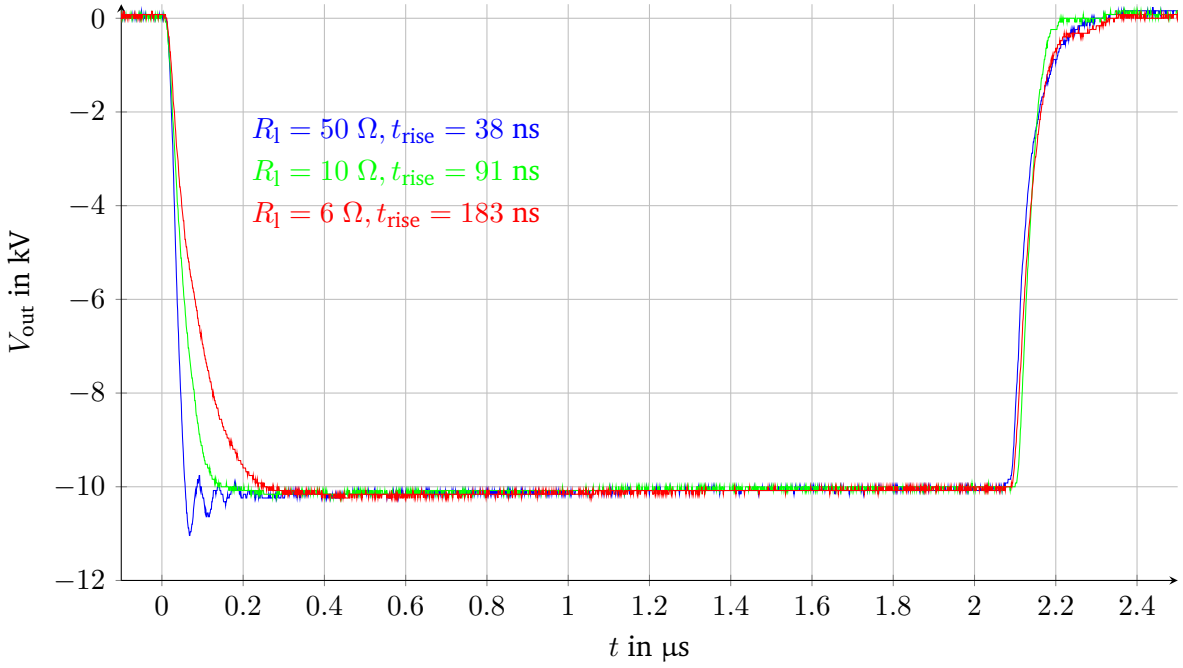

Figure 8.5: Measured output voltage of the 10 layer prototype with 8 branches per layer and different load resistors of $50\ \Omega$, $10\ \Omega$ and $6.25\ \Omega$ (rise time definition: 0.5 % to 99.5 %)

The ten layer prototype was equipped with 4 PCBs in each layer and different load resistors. Figure 8.5 shows the output voltage of the 10 layer prototype with 8 branches per layer and different load resistors. It can be observed that with a lower load resistor the rise time is becoming larger. For the $50\ \Omega$ case an overshoot was measured. The rise time difference and overshoot are caused by the mismatch of the IA to the load resistor. The IA is designed for $6.25\ \Omega$. Therefore a load resistor of $50\ \Omega$ causes a mismatch. For the $10\ \Omega$ resistor the mismatch is much less and no overshoot can be observed. Another reason for the slower rise time for lower load values can be the increased current load on the single MOSFETs since the voltage per layer is kept constant. Furthermore the L/R time constant of the circuit is increasing for a decreasing load resistor which results in slower rise times.

8.4 Measurements on the 22 layer prototype

The output waveform for the 22 layer IA generating a 15 kV pulse with a flattop length of 2.32 µs (from 99.5 % to 99.5 %) was measured. The pulse was generated with 15 constant voltage layers for which the primary windings of the remaining 7 layers were in short-circuit. Each layer was equipped with one PCB with two parallel branches. The load resistor was 50 Ω and the capacitors in each layer were charged to 1025 V to reach 15 kV of output voltage even at the end of the 2.32 µs long flattop. In this way each MOSFET conducted approximately 150 A during the pulse. Figure 8.6 compares the measurement with the simulation results. To compare the simulated model with the prototype setup the simulation models presented in chapter 4.3 were modified:

- in the switch model the resistance was increased from 1.1 mΩ to 12.5 mΩ to represent 2 instead of 24 parallel MOSFETs
- in the simulation with the MOSFET model the number of parallel MOSFETs was reduced from 24 to 2
- the total primary inductance was increased from 5 nH per layer (24 parallel branches) to $L_{\text{prim}}+L_{\text{cap}} = 60$ nH for 2 parallel branches. A second simulation was run with an inductance of 11 nH for two parallel branches.
- the capacitance per layer was reduced from 600 µF (24 parallel capacitors) to 50 µF for 2 parallel capacitors
- An inductance of 72 nH was introduced in the output circuit to obtain a total secondary inductance of approximately 80 nH as measured with the network analyzer (chapter 8.1). The 22 layers with an inductance of 350 pH per layer, together with a 36 nH inductance on both ends of the IA result in a total inductance of 79.7 nH in the secondary loop.
- the layers in short-circuit were modeled as a layer with a resistor of 0.1 mΩ in parallel to the core inductance, representing a virtual short-circuit
- the capacitor charging voltage was set to 1025 V

The upper plot of Fig. 8.6 compares the measured output waveform with the two simulation models described above. The pulse flattops of all waveforms show a very similar droop and voltage. It can be seen that the simulation with the switch model shows a shorter rise time and larger overshoot than both the measurements and the simulation with the MOSFET model. The fall time of the waveform from the simulation with the switch model is faster than the other two waveforms. The output waveform of the simulation with the MOSFET model shows the slowest rise time and a similar overshoot as the measured waveform. The fall time of the waveform form the simulation with the MOSFET model is faster than the fall time of the measured waveform.

The lower plot of Fig. 8.6 compares the output waveforms of the measurement and the two simulation models. The primary inductance was reduced from 60 nH to 11 nH, as measured with the network analyzer in chapter 8.1. The waveform of the switch model simulation shows an even shorter rise time and a stronger overshoot. The waveform of the MOSFET model simulation shows a slightly faster rise time and an overshoot and oscillation which matches well with the waveform of the measurement.

The ideal switch model is obviously not precise enough to simulate the IA. Therefore it was further optimised to match the measured waveform in a better way. For this purpose a second closing switch was connected in series with the main switch with a low on-state resistance. By adjusting the on-state resistances, switching

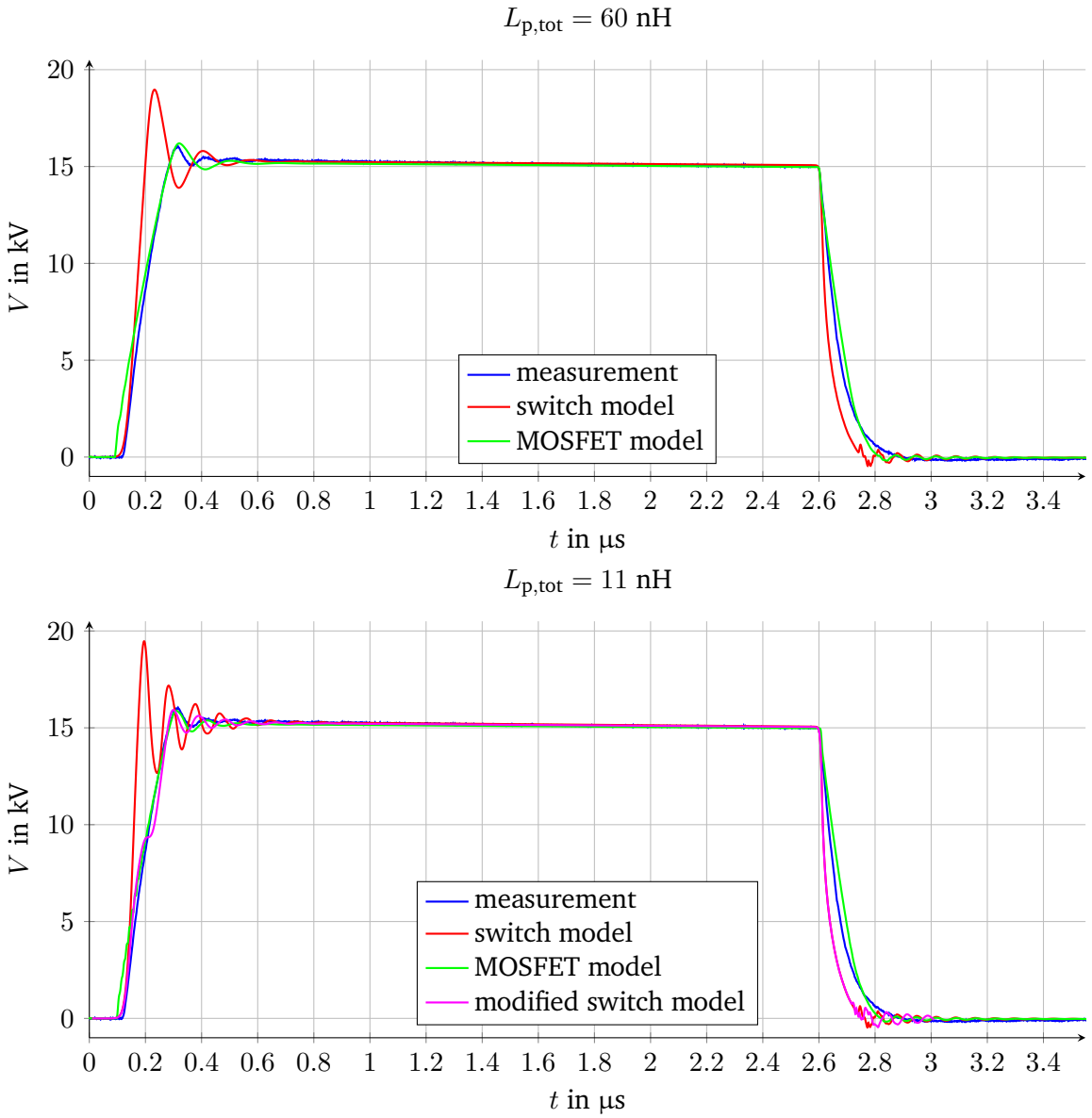

Figure 8.6: Comparison of the measured 15 kV output waveform with the simulated output waveform

speed and time of the two closing switches it was possible to approximately reproduce the measured waveform with the switch model, as shown in the lower plot of Fig. 8.6. Even if the rise time is similar, the switch model simulation shows a different turn-on behaviour than the measurement, and this behaviour could not be further optimised.

Table 8.2 compares the waveform values of the measurement with the simulation results of the MOSFET model and the single switch model. The overshoot, ripple frequency and damping of the simulated waveform, with the MOSFET model, fit well with the waveform measured for the prototype. The comparison of the simulation results with the measurement show that the primary inductance is probably significantly smaller than the initially estimated 60 nH per two branches: the measured 11 nH gives reasonable agreement of

Table 8.2: Comparison of the measured and simulated waveforms (2 parallel branches)

	Unit	Measure-ment	Switch model		MOSFET model	
			$L_{\mathrm{p,tot}} = 60$ nH	$L_{\mathrm{p,tot}} = 11$ nH	$L_{\mathrm{p,tot}} = 60$ nH	$L_{\mathrm{p,tot}} = 11$ nH
t_{rise} .5-99.5 %	ns	162	95	69	190	186
t_{rise} 1-99 %	ns	156	89	64	189	183
t_{rise} 10-90 %	ns	122	61	40	156	149
av. flattop	kV	15.2	15.2	15.2	15.2	15.2
overshoot	V	742	3668	4170	900	587
ripple frequ.	MHz	11.1	5.8	11.4	5.5	8.9
t_{fall} 90-10 %	ns	140	92	89	142	140

the MOSFET model simulation with the measurement. In general it can be noted that the influence of the inductances in the primary and also in the secondary circuit have a big influence upon the output waveform characteristics. The simulations with the suppliers MOSFET model match better than with the model using a switch. All together the measured results confirm a reasonable accuracy of the MOSFET simulation model and parasitic values used.

8.4.1 Consideration of layer position in the stack

The positions of the layers in the stack might have an influence on the pulse rise time. To confirm and evaluate this influence, 10 layers of the 22 layer prototype were equipped with PCBs at different positions and the remaining layers were put in short-circuit. The pulse capacitors of each layer were charged to

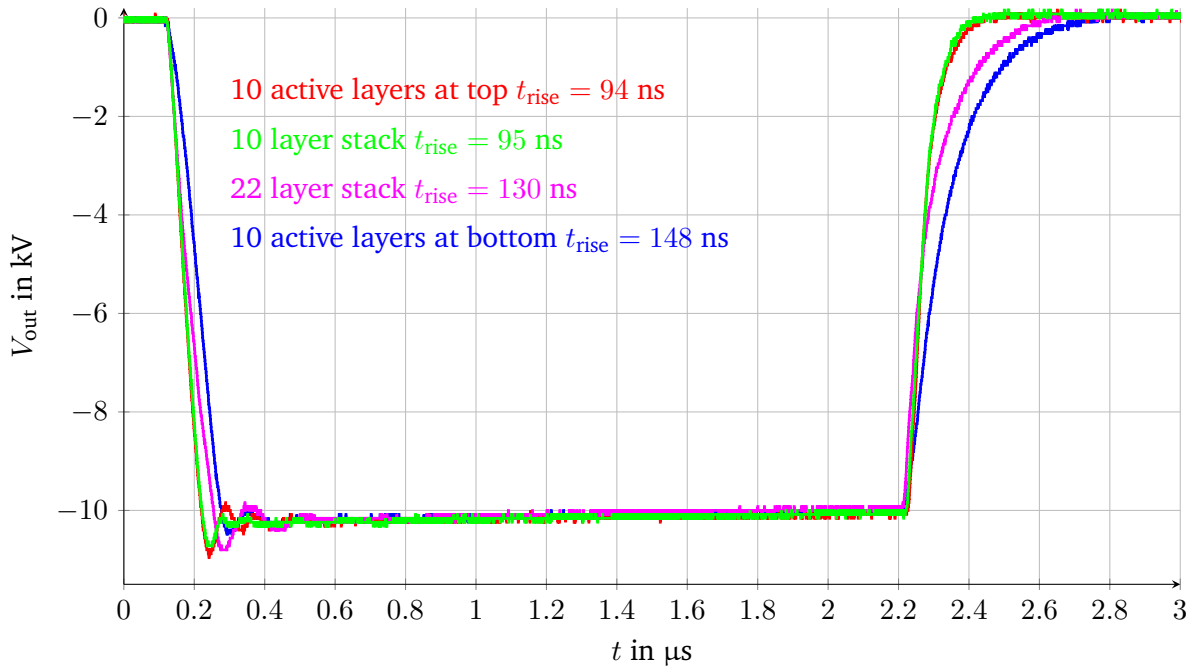

Figure 8.7: Comparison of the measured 10 kV output waveforms with different IA topologies. Rise time definition: 1 % − 99 %

$V_c = 1$ kV to generate a ≈ 10 kV pulse at the IA output. Measurements were done with the 10 PCB layers at the top of the stack and at the bottom of the stack. The output pulses were compared with measurements of the 10 layer prototype and a 10 kV pulse from the 22 layer prototype equipped with 22 layers and a capacitor charging voltage of $V_c = 455$ V. Figure 8.7 shows a comparison of the measured output pulse waveforms, the rise time definition is $1\ \% - 99\ \%$.

It can be seen that the rise time of the 10 kV output pulse is the shortest for the setup with the 22 layer prototype and 10 layers at the top. The rise time of the 10 layer prototype is similarly short and only 1 ns longer. The setup with 22 constant voltage layers has a rise time of 130 ns. In case of the 22 layer prototype with 10 layers at the bottom the rise time is longest with 148 ns. Also a longer fall time can be observed for the 22 layer stack with 10 layers at the bottom and 22 constant voltage layers compared to the 10 layer stack and the setup with 10 constant voltage layers at the top.

An explanation for the short rise time in case of the 10 layer at the top end of the stack could be that the characteristic impedance of the stack is significantly reduced if the layer is in short-circuit. The characteristic impedance of a layer is calculated with $Z_{\text{layer}} = \sqrt{\frac{L_p + L_{\text{prim}}}{C_p}}$ where L_p and C_p are the parasitic inductance and capacitance respectively and L_{prim} is the inductance of the primary circuit. In case of 2 parallel branches the characteristic impedance of the stack could be estimated analytically. A primary inductance of 60 nH results in an impedance of about $21\ \Omega$ and a primary inductance of 11 nH results in an impedance of about $9\ \Omega$. The inductance of the stack becomes $1.6\ \Omega$ if there is no PCB mounted and the primary inductance is therefore zero. The impedance change within the stack causes a significant portion of the pulse to be reflected earlier if the active layers are on top of the stack, what leads to a similar two way propagation time as in case of a shorter stack.

8.5 Analogue modulation with biasing

Modulation layers as a tool to modulate the output pulse of an IA have been described in chapter 3.5. The biasing circuit to bias the magnetic core and shift the working point into the third quadrant of the BH-curve to generate longer pulses was described in chapter 3.4.2. The use of modulation layers in an IA together with biasing of the magnetic cores has been applied by Gower in [48]. Even if it was applied in the paper, the challenges of applying both, modulation and biasing, haver never been documented in literature so far. As described in chapter 3.5 it is necessary to change the direction of the biasing current for the biasing layers. Therefore the biasing circuit is leaving the IA after passing through the constant voltage layers and is fed through the modulation layers from the opposite side. Figure 8.8 shows a picture of the modified biasing circuit and a schematic where the biasing loop through the modulation layer is described.

To confirm that modulation of the output waveform is possible when operating the IA in bias mode, two different measurements were conducted: The output pulse was modulated with one passive analogue modulation layer for a given magnetic core and different modulation resistors were used to demonstrate the influence of the modulation resistor on the output waveform. The output waveform was modulated with one passive analogue modulation layer for a given modulation resistor and different magnetic cores were used for the modulation layer to demonstrate the influence of the magnetic material. For both measurements magnetic cores with a square shaped BH-characteristic were used in the constant voltage layers. The biasing

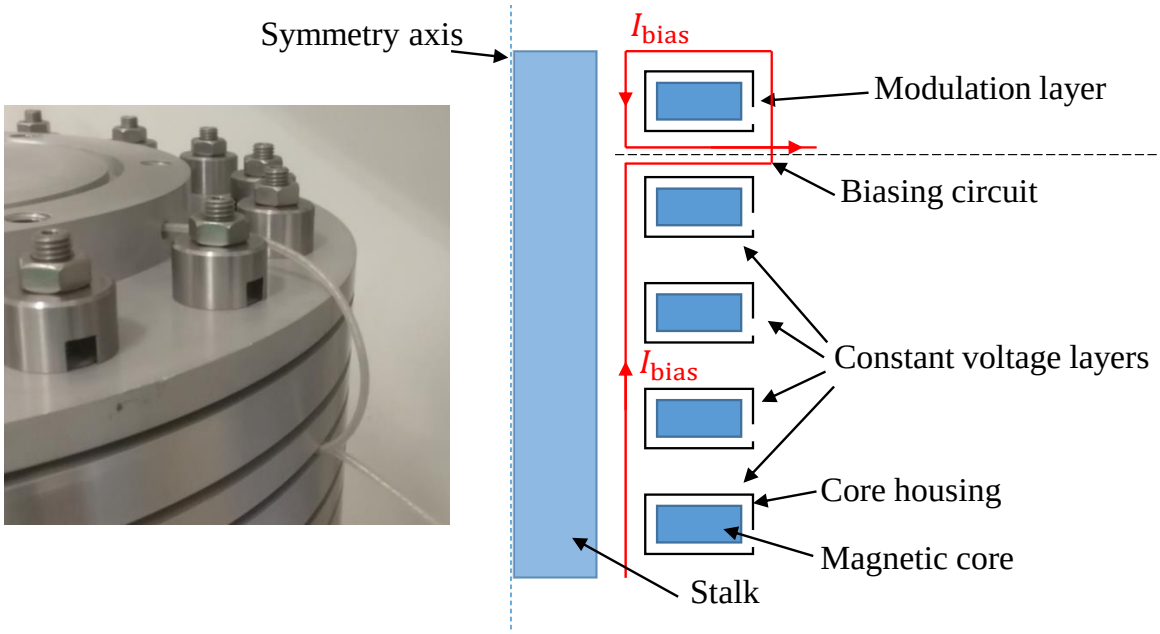

Figure 8.8: The biasing circuit of the modulation layer (left) and a schematic describing the path of the biasing loop

current for both measurements was set to 0.7 A. Since the voltage drop across the modulation layer is different for each measurement the output voltage of the IA was adjusted to be the same for each measurement 0.2µs after turn-on of the output pulse to compare the output waveforms.

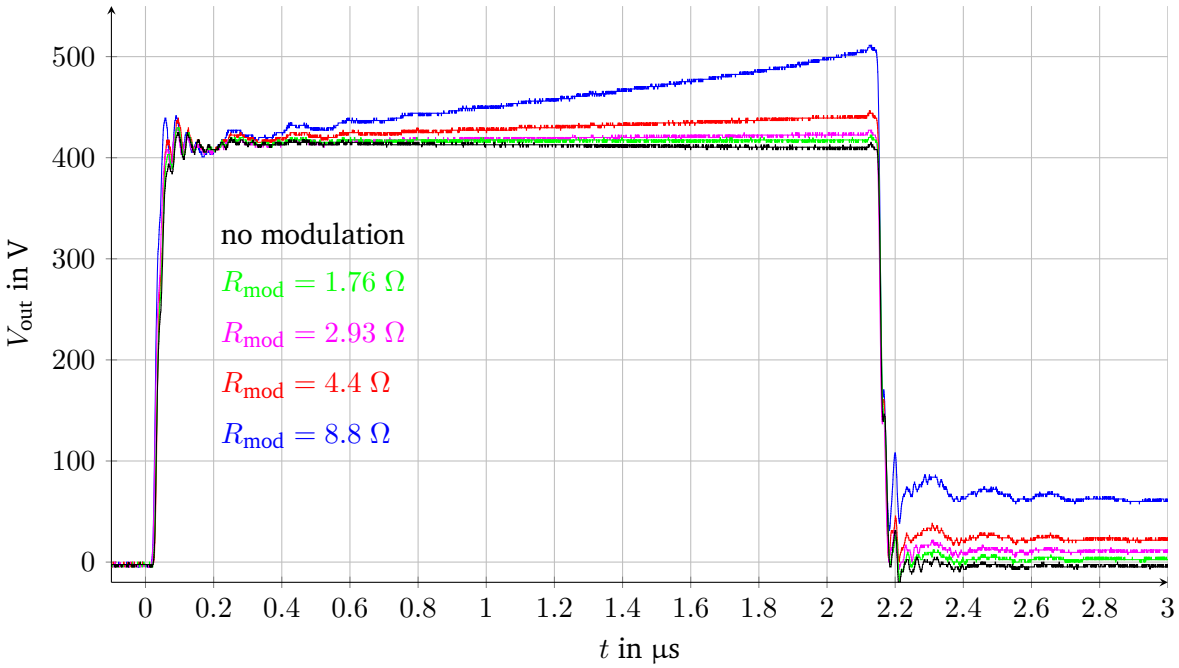

Figure 8.9: Measured output waveform of the IA for different modulation resistors and a given magnetic core with linear BH-characteristics

Figure 8.9 shows the output waveform of the IA with four constant voltage layers and one modulation layer. The modulation resistor of the modulation layer was changed for the different measurements. The load resistor was kept constant for all measurements at $R_{\text{load}} = 8.8\ \Omega$. The output waveform was set to 415 V at $t = 0.2$ µs in all measurements. Depending on the modulation resistor a different capacitor charging voltage was required to reach the 420 V output voltage. The used core was a core of supplier 3 from chapter 6.1 with linear BH-characteristics and a core inductance of $L_{\text{c}} = 28.8$ µH. It can be seen that the output waveform shows a different droop of the flat-top depending on the modulation resistor. The measurement without modulation shows a droop of -10 V from after the turn-on ripple until turn-off. Already with the lowest modulation resistor of $1.76\ \Omega$ the droop can be compensated. If the modulation resistor is increased the droop of the output waveform is over compensated which leads to an increasing output voltage during the flat-top. Table 8.3 shows the measured values for different modulation resistors.

Table 8.3: Measurement results for passive analogue modulation with different modulation resistors and a given magnetic core and for different magnetic cores and a given modulation resistor

R_{mod} in Ω	$V_{\text{out,0.2µs}}$ in V	V_{cap} in V	droop in V	magnetic core
0	415	109	-5	supplier 3
1.76	415	129	+2	supplier 3
2.93	415	142	+8	supplier 3
4.4	415	158	+21	supplier 3
8.8	415	200	+91	supplier 3
0	685	180	-3	no modulation
4.4	685	263	+25	supplier 1 linear
4.4	685	254	-3	supplier 1 square
4.4	685	263	+11	supplier 2
4.4	685	261	+56	supplier 3

The influence of the core inductance on the modulated output waveform can be shown by using different magnetic materials in the modulation layer while keeping the modulation resistor constant. Four different core materials were available to show the effect of the core inductance. The modulation resistor was chosen as $R_{\text{mod}} = 4.4\ \Omega$ and the load resistor as $R_{\text{load}} = 8.8\ \Omega$. Figure 8.10 shows the output waveform of the IA for the different cores. Table 8.3 shows the measured values.

It can be seen that depending on the used magnetic core in the modulation layer the droop of the output waveform is different. With the square shaped core in the modulation layer the modulation effect is not measurable, compared to the waveform without modulation, and the droop of the waveform is -3 V as without modulation. The magnetic cores with a linear BH-curve have a stronger influence on the flat-top and cause an increasing voltage during the flat-top. The effect of the different cores agree with the measurements of the BH-curves in chapter 6.1 where for the core of supplier 3 the flattest BH-curve was measured, followed by the linear core of supplier 1 and the core of supplier 2 showed the steepest BH-curve of the linear cores.

In both, Fig. 8.9 and Fig. 8.10, the output voltage waveform shows a ripple and offset after the pulse is turned off. This offset is caused by the magnetizing current in the modulation layer. In contrary to the constant voltage layers in the modulation layer it is not possible to provide a free wheeling path to the magnetizing current after the pulse is turned off. Therefore the current causes a voltage drop over the

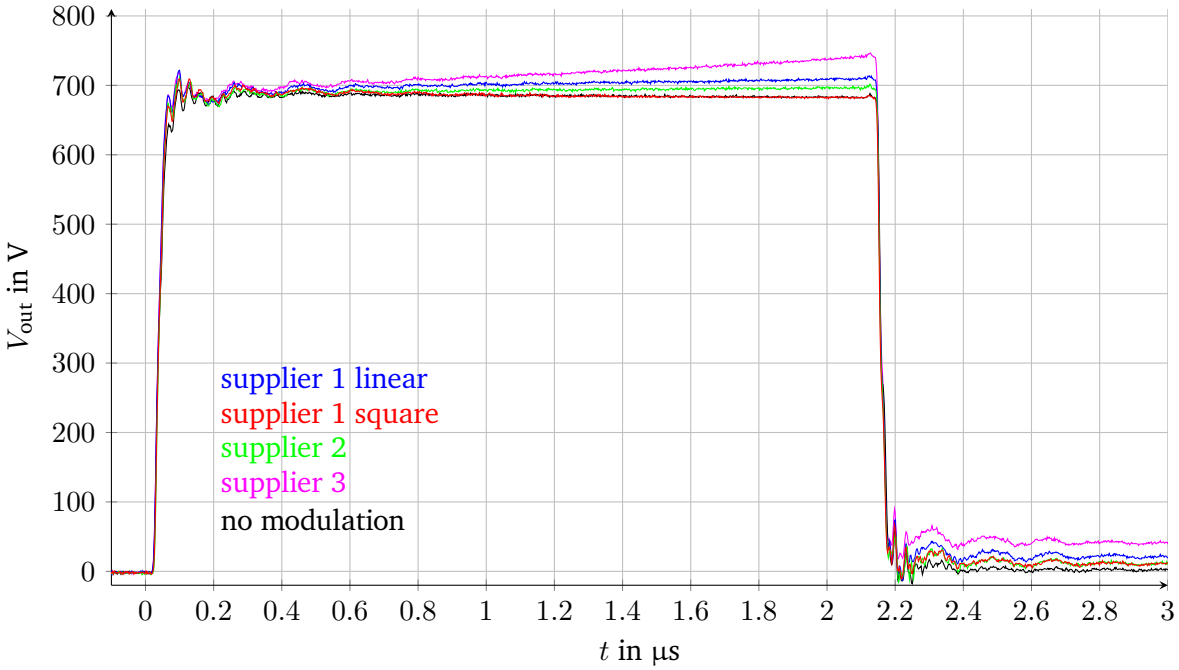

Figure 8.10: Measured output waveform of the IA for different magnetic cores in the modulation layer and a given modulation resistor $R_{\text{mod}} = 4.4\,\Omega$

modulation resistor while it is decaying to zero after the pulse. This voltage is transformed to the secondary winding and causes a voltage drop over the load resistor. For the design of a passive analogue modulation layer this voltage offset needs to be taken into account and the modulation should be designed in such way that the ripple and offset of the voltage after the pulse is within the required specifications. This infers a modulation with the lowest possible voltage drop - this requires a low magnetizing inductance for this layer (see section 4.2). Alternatively the voltage offset after the pulse could be compensated by an additional layer in the stack that generates a pulse to oppose the offset.

9 Inductive adder in short-circuit mode

Although the kicker magnets of the FCC-hh injection system would be terminated with a matched impedance, many pulsed systems are designed to be operated in the short-circuit mode. In the case of a kicker system this means that the kicker magnet is terminated with a short-circuit. The short-circuit causes a negative reflection of the voltage pulse, resulting in a voltage of zero, and a positive reflection of the current pulse, resulting in current doubling [18, 53]. With the double current, the kick strength is also doubled. The advantage of such a system is, that for a given system impedance and length, only half the voltage needs to be provided to generate a certain current. A disadvantage is, for example, that the pulse has to propagate through the magnet twice and the rise time is therefore increased. Thyratron based systems cope well with both matched and short circuit terminations. Since the IA is a possible alternative to thyratron based pulse generators it would be of high interest to use an IA with a load in short-circuit.

9.1 Long connection cables for short-circuit operation

One way to avoid too high currents in the kicker system is to connect the kicker magnet to the IA with a cable having a pulse propagation length of more than half the required flattop length ($t_{\text{prop,cable}} > t_{\text{pulse}}/2$). In this way the reflected pulse from the kicker magnet would arrive at the IA after the required pulse duration i.e. the MOSFETs have been turned off. The cable would need a length of at least $t_{\text{pulse}}/2$ to make sure the MOSFETs are already turned off before the reflected pulse reaches the IA. A disadvantage of this system is the long cables between the IA and the kicker magnet that are costly and cause frequency dependent attenuation. However, the use of long cables to make an IA work with short-circuit terminated loads is a possibility that does not involve any major modifications to the IA.

9.2 Theoretical consideration of changing IA impedance

To achieve a short rise time, the impedance of the IA must be matched with the impedance of the coaxial cable and the kicker magnet. One end of the IA is in short-circuit, the other end is the pulse output. Usually the pulse output of the IA is connected to the kicker magnet via a coaxial cable and the kicker magnet is terminated with a matched resistor, avoiding a reflection of the pulse. For the short-circuit mode, the kicker magnet is terminated with a short-circuit, resulting in a reflection at the end, doubling the current. The reflected pulse travels back through the system towards the short-circuit side of the IA where it would be reflected again causing a further increase of the current - the pulse propagates towards the short-circuit of the kicker magnet again. This process would repeat until the current is too high and destroys the

components; note that the cores do not saturate. One way to avoid that the pulse is reflected at the short-circuit side of the IA is to match the impedance of the IA so that the pulse is terminated. However, this has the disadvantage of requiring an IA with twice the output voltage [9].

A possible way to change the impedance of the IA could be a second switch in the primary circuit which commutes the current into a parallel resistor, just as the first reflection of the pulse arrives at the IA. With a properly designed IA this changes the characteristic impedance of the IA such that it appears as a termination and therefore does not reflect the pulse.

Possible problems of this approach could be caused by the increase of the primary inductance due to the additional semiconductor switch and resistor. A reasonable design needs to be developed to ensure a low inductance which is required for fast current switching. In addition, the resistors must be rated to absorb the required peak power and energy.

9.3 Simulations of a short-circuited IA

The described circuit has been simulated with PSpice. Figure 9.1 shows the schematic of one layer of the IA as it was simulated in PSpice. The primary circuit was extended compared to the PSpice model of chapter 4.3. The characteristic impedance of the IA and the load was changed to $26.33\ \Omega$ which is the impedance of a kicker system at CERN (KFA 45: PS proton injection), used in the proton synchrotron (PS) accelerator, and the IA would consist of 30 layers in total. In series to the pulse capacitor a parallel circuit consisting of an opening switch (U3) and a resistor (Rmatch) was modelled. During the time the switch is closed and the primary current flows through the switch: from the moment the switch is opened the current flows through the resistor in parallel. In this way the impedance of each layer, and thus the entire stack, can be changed by opening the switch. The value of the matching resistor per layer was set to the system impedance divided by the number of layers in the stack $R_{\text{match}} = \frac{26.33\ \Omega}{30} = 0.878\ \Omega$. Figure 9.2 shows a part of the schematic of the entire PSpice simulation of the IA stack with impedance

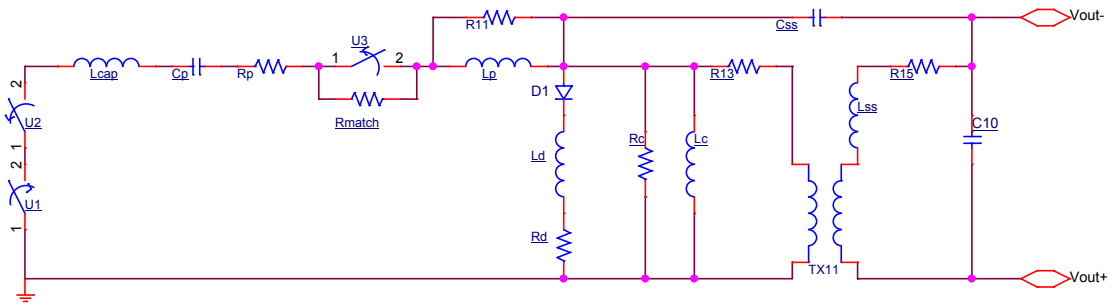

Figure 9.1: PSpice model of an IA layer with additional resistor (Rmatch) and switch (U3) to match the impedance of the stack to the reflected pulse

matching. The constant voltage layers (CV_layer) are sub-circuits and represent the circuit shown in Fig. 9.1.

Figure 9.3 shows the simulated waveform of the current through the MOSFET with and without impedance matching. The waveform without impedance matching (blue) shows that the layer current increases every time the reflected pulse reaches the IA, after being reflected from the short-circuit termination of the load.

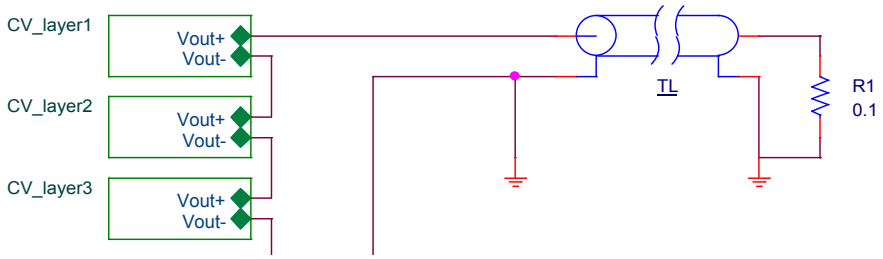

Figure 9.2: PSpice model of an IA stack connected to an ideal transmission line, representing a kicker magnet, with a short-circuit at the output

Since the length of the transmission line to the load was set to 0.4 µs the first increase of the current in the IA happens 0.8 µs after the MOSFET turn-on; i.e. the time for the pulse to travel the load, reflect at the short-circuit termination and travel back to the IA. The second waveform (red) shows the current for the case when the matching switches are opened in the moment the reflected waveform arrives at the IA the first time. A good adjustment of the closing time has a big influence on the current ripple generated at the moment of reflection: for the simulation shown in Fig. 9.3 the turn-on time of the IA was set to 100 ns and the opening time of the matching switch to 885 ns. The opening transition time of both switches in PSpice was set to 135 ns. For this opening time of the matching switch the smallest ripple was obtained.

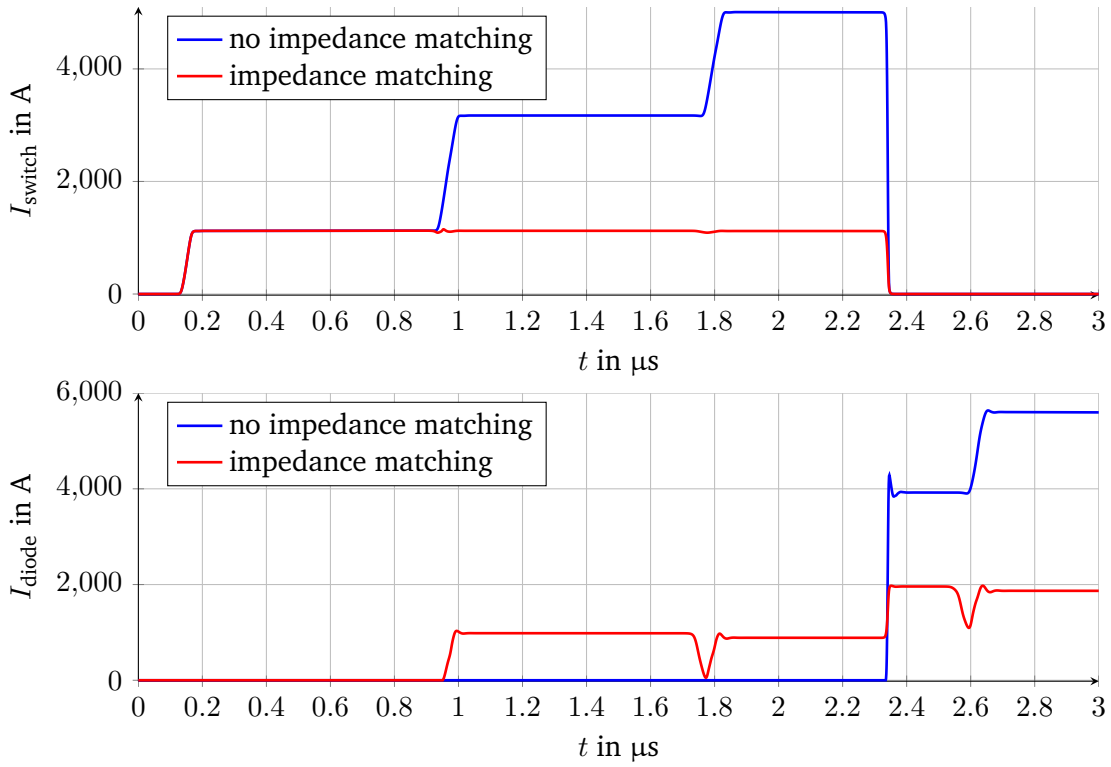

Figure 9.3: Simulated switch current (top) and diode current (bottom) of a IA layer with (red) and without (blue) impedance matching with a short-circuit terminated load

The simulation results show that a change of the system impedance of the IA with an additional switch

and resistor is possible. Thereby a significant increase of the MOSFET current can be avoided. The exact matching time and resistor value are important parameters to reduce ripple and improve matching. However, the reflected current waveform causes the diode to conduct a high current. Figure 9.3 also shows the current through the diode of a layer with and without impedance matching. It can be seen that without impedance matching, after turn-off, the entire current commutes into the diode. In case of impedance matching, the current through the switch does not increase but with every reflection of the current at the IA the current through the diode is increasing. After turn-off of the switch also the current through the switch commutes into the diode. By introducing a resistor in series with the diode the current can be reduced but is still a concern. The output current of the IA shows several unwanted artefacts and effects caused by reflections and switching. Further studies are necessary to improve the technique and investigate the practicability for applications.

10 Conclusions and outlook

This thesis describes the design of a fast rise time pulse generator based on inductive adder (IA) technology. The functionality of the IA is described in the first chapters and an overview of existing inductive adders and the state of the art is given. Based on the demanding requirements of the FCC-hh injection system, an inductive adder was designed. The main challenges of the IA design are the fast pulse rise time, relatively long pulse flattop duration and the low system impedance combined with high output current and voltage. An IA with the required parameters in terms of rise time, flattop duration and system impedance has not yet been reported in the literature. To obtain fast rise times and low system impedance, the PCB was designed with SiC MOSFETs, which have faster rise times and lower on-state resistances than their Si counterparts. After the design was confirmed with PSpice simulations, components for the IA have been selected and tested intensely to select the best components for a prototype IA.

The prototype IA has been designed and built, using the selected components. Detailed tests and measurements were carried out to verify the simulation results. The results showed that the design of the IA was adequate to generate pulses with fast rise time, low system impedance and a flattop duration of up to $2.32\ \mu s$. Nevertheless, to reach the challenging requirements for the FCC-hh injection, further system improvements of the hardware design are necessary, e.g. for ensuring that the impedance of the stack, including connections at both ends, is well matched (see paragraph on Future Work).

To reach fast rise times a short IA stack is required: this was achieved by introducing a biasing circuit that made it possible to bias the magnetic cores and therefore reduce the required volume of magnetic material and in particular the layer and stack height. To reach the flattop stability required for the FCC injection the use of passive analogue modulation is envisaged which reduces the droop of the output waveform. A biasing circuit together with modulation layers in an IA has not been reported previously in the literature. The new studies and measurements reported in this thesis have shown how a passive analogue modulation layer can be used, together with biasing, in an IA. Additionally, it was analytically shown that a low magnetizing inductance for the modulation layers results in a lower voltage drop over the modulation layer and therefore require less constant voltage layers to compensate for the voltage drop. The reduction of layers in the stack is important to reach fast rise times.

Two parallel branches consisting of one pulse capacitor and one SiC MOSFET each were realised on one PCB. Up to 12 PCBs can be connected to increase the number of parallel branches of one layer up to 24 and therefore increase the maximum output current accordingly. Alternatively, the PCBs could also be used in separate layers of the IA prototype to increase the output voltage. This concept with a higher modularity has shown some advantages compared with only two PCBs per layer: a layer consisting of only 2 PCBs is more expensive and gives less freedom for assembly. A disadvantage of many PCBs carrying the primary circuit is the increased complexity of the triggering system, which can become problematic if several hundred PCBs are to be triggered simultaneously.

Oil insulation was used for the 15 kV output to realise the low system impedance and keep the dimensions of the magnetic cores within an acceptable range. This concept was proved to be feasible even though it required additional effort during assembly, disassembly and maintenance.

PSpice simulations have shown that, in case of low system impedance and therefore high parasitic capacitance between primary and secondary, the charging and discharging current of this parasitic capacitance can exceed the load current - especially for high output voltage. Since the free-wheeling diodes have to carry the current it needs to be dimensioned accordingly. A formula has been derived that allows to estimate the parasitic capacitance discharging current analytically.

A failure mode such as saturation of a magnetic core or an electrical flashover in the load could result in a significantly higher output current and potentially destroy many MOSFETs. Hence, an over current protection for the MOSFETs is necessary: such a system is of fundamental importance for an operational IA. An over current protection would protect the MOSFETs not only of failure modes within the IA itself but also of other parts in the kicker system e.g. a short-circuit in the magnet or cable.

Since the IA would be also useful to replace old pulse generators at CERN, which are often operated in short-circuit terminated systems, first studies on using an IA in a short-circuit terminated system were conducted. This configuration has been simulated with PSpice and it has been shown that the operation of an IA in a short-circuit terminated system is, in principle, possible. The simulations show that it is possible to prevent the current through the MOSFET increasing, when the reflection from the short-circuit arrives at the IA, by adopting a novel system of matching the impedance of the IA stack when the reflected waveform reaches the adder. However, further investigations are required before a prototype is built.

Even if only some of the proposed improvements can be realised, and a reliable operation and control of the IA can be guaranteed, the IA is almost an ideal pulse generator for relatively short pulse duration and high reliability kicker systems. In addition, the IA can be easily adapted to different applications (voltage, current and impedance), and could continue operation in case of a faulty layer. Furthermore the layer can be quickly exchanged.

Future Work: The results of this thesis confirm the potential of the IA to deliver high current, high voltage output pulses with short rise time and promise exciting developments of this technology during the coming years. An interesting further step would be to conduct full-scale measurements, upon the prototype constructed during the research and development for this thesis, for which about 250 (500 MOSFETs and pulse capacitors) of additional PCBs would need to be manufactured. This investment would not only make it possible to conduct the full-scale measurements (15 kV, 2.4 kA) but also to use the PCBs in other setups for further research of the IA technology. When all the PCBs for the constant voltage layers are available, it would be interesting to conduct measurements to reach the final pulse requirements for the FCC-hh injection kicker system. For this attempt, additional modulation layers would be necessary.

However, before a larger number of PCBs is manufactured, it is strongly recommended to implement an over current protection in the driver circuit of each MOSFET, as mentioned in chapter 5, to avoid significant damage and thus high costs in case of such a fault. Several over current protection methods could be suitable and the best approach needs to be determined. The trigger system planned for the final 15 kV and 2.4 kA IA is based on the technique of splitting up one trigger signal into over 200 signals to trigger each PCB. A new trigger system that allows to select which layer and branch should be triggered, and an easy adaptation of the pulse duration while still ensuring that the trigger pulse cannot be too long such that the

magnetic cores saturate, together with triggering every branch reliably at the same time, within < 1 ns, is necessary. Together with the triggering system, a general design for a state-of-the-art monitoring and control system could be developed. Such a system should not just be able to control the pulse parameters in a reliable way but also monitor operation of the IA, each layer or even each branch, and could return this information (e.g. charging current, LV power supply, trigger signal health, temperature, etc.) to easily identify failures or possibly even degradation, before a failure occurs.

To further improve the rise time of the output pulse, modifications on the ground end and the high voltage feed-through of the IA can be realised. These modifications are required to reduce the impedance mismatch and, particularly for a low impedance system, reduce the inductance - which presently limits the rise time, especially in case of low Ohmic loads, where the L/R time constant is significant.

Ensuring the continuity of the system impedance through the IA stack turned out to be a challenging task. In particular the short-circuit and high voltage output end connections must be designed with care - ideally the characteristic impedance of both ends of the stack should be matched to the system impedance. The short-circuit end of the IA is easier to deal with than the HV output end, since there are not the HV issues at the short-circuit end and thus this can be a small length. For the HV output end, further investigations for insulation and dimensions are required to match the impedance - if this is not feasible, any impedance mismatch, and its duration, should be minimized since impedance mismatch will cause an increase of pulse rise time at the output waveform.

The consideration of an IA operated without a short-circuit on one end, but rather with an output on both ends, that feed into the same load, could be studied to determine if such a technique would reduce the rise time, since the magnet is filled from both ends. Since, for higher system impedances, achieving faster field rise times is less challenging, it is recommended that the system impedance for the FCC-hh injection kicker system is slightly increased, e.g. to $8.33\ \Omega$ or $10\ \Omega$. The disadvantage is a higher operation voltage, to achieve the same current, which requires more layers in the IA: however, this disadvantage might be acceptable. A higher system impedance will also increase the insulation gap between primary and secondary windings, which makes the hardware manufacturing tolerance and stalk alignment less challenging and increases the insulation strength.

As mentioned in chapter 9, many existing pulse forming lines (PFL) or pulse forming network (PFN) kicker systems are operated in short-circuit mode. The IA would be an option to replace ageing systems at CERN, but operation of an IA with a short-circuit application has not been reported yet in the literature. The design of an IA prototype that can be operated in a short-circuit application, by changing the impedance when the pulse reflected from the short-circuit arrives at the IA, would be of great interest. Based on the theoretical considerations and simulations presented in chapter 9, such an IA should be feasible. Further investigations in this field are required to continue with the initial idea of changing the system impedance of the IA to avoid further reflections.

Long-term measurements on an IA are a very important step towards the daily use of an IA in the accelerator complex. In theory, there are reliability advantages of the IA compared to conventional, thyratron based, pulse generators. To prove this, long-term measurements under various conditions are required to investigate the reliability of the IA under a realistic operating environment.

The biasing of the magnetic cores is currently realised with a single biasing circuit through the entire stack, as described in chapter 3.4.2. Even though the biasing circuit did not show any major problems and served its purpose so far, there are possibilities to improve its design. The fact that all layers of the IA are magnetically coupled to the biasing circuit increases the complexity of the system, as the biasing circuit must be rated for the full output pulse voltage of the IA. It was shown in chapter 6.1 that the biasing

circuit introduces a ripple in the output waveform, which might be avoided by modifying the biasing circuit. An option could be to replace the single biasing circuit for all layers, and instead have a separate biasing circuit for each layer. In this way the layers would be biased independently and the induced voltage in the biasing circuit would be reduced from the full IA output voltage to only the layer voltage. Maybe it is even possible to use the charging current of the pulse capacitor to bias the magnetic core instead of using an additional power supply. A reduction of the pulse flattop ripple, caused by the biasing circuit, using an active modulation layer, is a goal of future studies.

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A Appendix

A.1 Measurement equipment

Table A.1 lists the used equipment to conduct the measurements presented in this thesis. The listed equipment was used for all measurements except the BH-curve measurements.

Table A.1: Equipment used for measurments on the IA components and on the IA prototype

Equipment	Producer	Type	Basic specifications
Oscilloscope	Tektronix	DPO5034	350 MHz, 5 GS/s
LV probe	Rohde & Schwarz	RTM-ZP10	500 MHz, 400 V, 10 : 1
HV probe	Tektronix	P5122	200 MHz, 4 kV, 100 : 1
HV probe	Tektronix	P6015A	75 MHz, 20 kV, 1000 : 1
Signal generator	Aim TTi	TG5012A	50 MHz, 2 channels
LV power supply	HAMEG	HM7042-5	2x 0-32V, 2 A; 5.5 V, 5 A
HV power supply	Heinzinger	PNC 3500-300 ump	3.5 kV, 300 mA
Biasing power supply	Oltronix	B-60-1	0-60 V, 1 A
Network analyzer	Agilent Technologies	E5071C ENA Series	9 kHz-4.5 GHz

A.1.1 BH-curve measurements

Table A.2 lists the measurement equipment used for the BH-curve measurements presented in section 6.1.2.

Table A.2: Equipment used for measurments on the IA components and on the IA prototype

Equipment	Producer	Type	Basic specifications
Oscilloscope	LeCroy	WaveSurfer 64Xs	600 MHz, 2.5 GS/s
Signal generator	Agilent Technologies	33500B Series	20 MHz
LV power supply	Farnell instruments	L30DT	2x 0-30 V, 2 A
RC Integrator	custom made	-	11 kΩ, 10 µF
Amplifier in primary	custom made	-	50 W, 5 Hz − 50 kHz
Shunt in primary	-	-	1 Ω

A.2 Supplier for sample components

Table A.3: Supplier and material information of sample magnetic cores

No.	BH-char.	Supplier	Material
1	linear	Vacuumschmelze	VITROPERM 500 F
1	square	Vacuumschmelze	VITROPERM 500 Z
2	linear	Magnetec	NANOPERM 60000
3	linear	Hitachi metals	FINEMET

Table A.4: Suppliers and product information of sample capacitors

No.	Supplier	Product
Cap1	Leclanché	PPM-4 150-25.0 a (K) 10%
Cap2	WIMA	DC-LINK MKP4 25.0 UF 1300VDC 10% RM52.5
Cap3	WIMA	DC-LINK MKP4 25.0 UF 1100VDC 10% RM37.5
Cap4	WIMA	DC-LINK MKP4 30.0 UF 1100VDC 10% RM52.5
Cap5	WIMA	DC-LINK MKP4 35.0 UF 1100VDC 10% RM52.5

Table A.5: Supplier and product information of sample SiC MOSFETs

Manufacturer	Product	Voltage	Current
CREE	C2M0025120D	1200 V	90 A
CREE	C2M0045170D	1700 V	72 A
Microsemi	APT80SM120B	1200 V	80 A
Rhom	SCT3022KL	1200 V	95 A

A.3 Design of the air coil for the biasing circuit

The inductance in the biasing circuit L_b is important to prevent a destruction of the biasing power supply by the HV output of the IA. The flux density swing of the magnetic core of L_b needs to be large enough to not saturate during the pulse. Since the biasing current has the same orientation through L_b as the load current resulting in the magnetic field strength adding up in the magnetic core of L_b: $H_{tot} = H_b + H_p$. H_b is the magnetic field strength induced by the biasing current and H_p is the magnetic field strength induced by the current from the generated pulse. Figure A.1 shows an example for a BH-characterisic with the total magnetic field strength and the resulting flux density with a BH-curve of a ferromagnetic material.

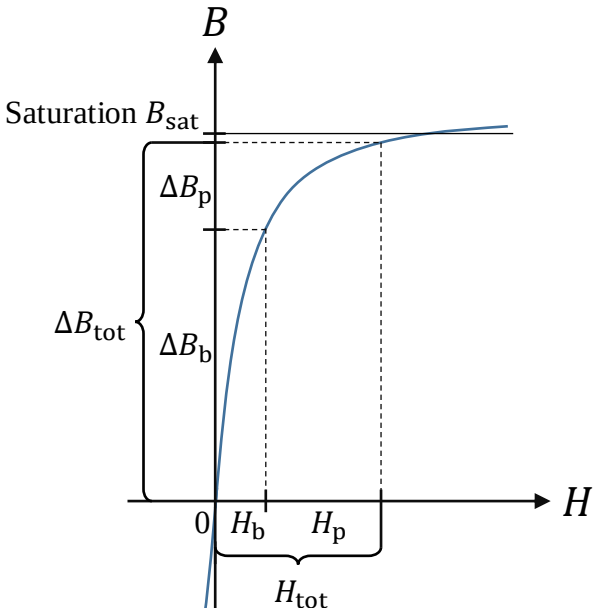

Figure A.1: Required flux density swing in biasing inductance resulting from biasing current and current induced by the output pulse

If the biasing inductance is realised with a magnetic core the number of turns can be kept low but the core requires a large cross sectional area to avoid saturation. A saturated biasing inductance would behave as a short circuit in parallel to the load of the IA and result in a current increase and rapid capacitor discharge. Therefore the biasing inductance was realised as an air coil. The inductance of a cylindrical coil can be calculated with:

$$L_{cyl} = \mu_0 \mu_r \cdot N^2 \frac{A}{l}, \tag{A.1}$$

where $\mu_0\mu_r$ is the permeability of the magnetic material in the cylindrical coil, N the number of coil turns, A the cross sectional area of the cylinder and l the axial length of the coil [107]. For an air coil the permeability becomes: $\mu_0\mu_r = \mu_0 = 4\pi \cdot 10^{-7}\ \frac{\mathrm{Vs}}{\mathrm{Am}}$. The coil was wound on a spool body with an inner diameter of 15 cm and a axial length of 25 cm. The 300 turns were wound in layers of 10 turns on the spool body, starting at one side of the axial length and finishing on the opposite axial side to reduce the maximum voltage between two neighbouring cable turns to a minimum. Considering 30 layers with 10 turns in each layer, a maximum voltage of 500 V would appear between two neighbouring turns. This linear consideration neglects the effect of the parasitic capacitance of the windings. Therefore a higher voltage

between two neighbouring turns is expected. The used cable had a rated insulation of 1 kV resulting in a breakdown voltage of 2 kV between two neighbouring turns. The winding scheme of the air coil is shown in Fig. A.2.

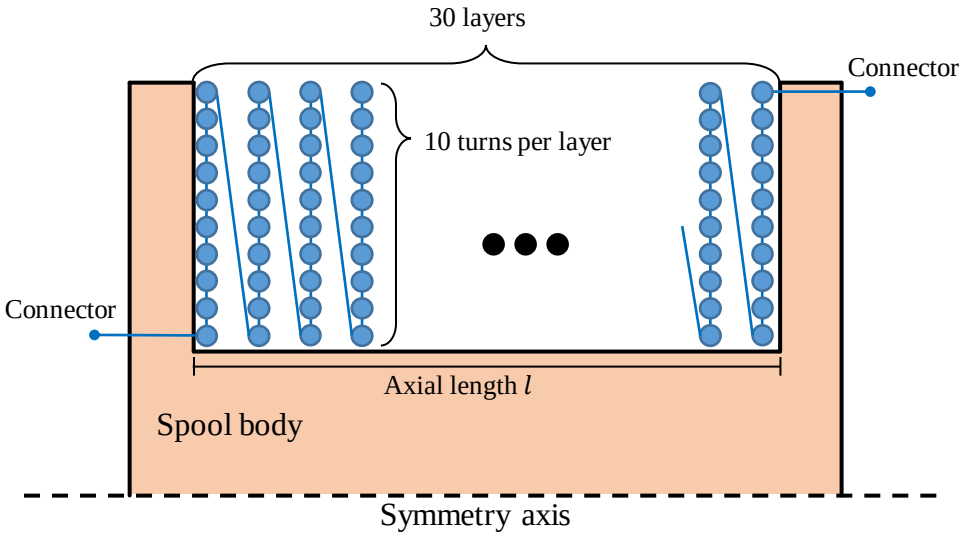

Figure A.2: Winding scheme of the air coil for the biasing inductance

The resulting inductance of the air coil can be calculated with equation A.1 to be $L_\mathrm{b} = 2.5$ mH. The increase of the current in the biasing circuit during a 2.5 µs long pulse of 15 kV can be calculated to be $\Delta I = \frac{U \cdot \Delta t}{L_\mathrm{b}} = 15$ A. The resulting 15 A turned out to be an acceptable value to safely protect the biasing circuit power supply. The 2 kV of breakdown voltage between two neighbouring turns are sufficient to safely operate the air coil in the biasing circuit with pulses up to 15 kV of output voltage. As shown in Fig. 3.4.2, a diode in parallel to the power supply is additionally protecting it against excess currents.

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