Operational Experience and Performance with the ATLAS Pixel detector at the Large Hadron Collider

Gabriele Balbi, on behalf of the ATLAS Pixel Collaboration

I.N.F.N. Bologna Italy

Abstract–The Pixel detector is a crucial component of the ATLAS detector. The tracking performance of the ATLAS detector relies critically on its 4-layer Pixel detector. It has undergone significant hardware and readout upgrades to meet the challenges imposed by the higher collision energy, pileup and luminosity that are being delivered by the Large Hadron Collider (LHC), with record breaking instantaneous luminosities of 2×10^{34} cm^{-2} s^{-1} recently exceeded. The key status and the performance metrics of the ATLAS Pixel Detector are summarized, and the operational experience and requirements to ensure optimum data quality and data taking efficiency will be described, with special emphasis on radiation damage experience.

I. Introduction

ATLAS [1] is a general-purpose particle physics experiment at the Large Hadron Collider (LHC), built to investigate the Standard Model (SM) and physics at the TeV scale. One of the main parts of ATLAS is the Inner Detector, which is composed of the Pixel Detector [2], the Silicon Strip detector (SCT) and the Transition Radiation Tracker (TRT). The Pixel detector is the innermost of them and consists of 4 layers (Insertable B-Layer, B-Layer or L-0, Layer 1 and Layer 2) of pixel modules in the barrel region with 3 pixel disks on each endcap side.

During Run 2 (2015-2018) the ATLAS experiment has experienced a challenging period. The LHC collision energy reached 13 TeV and the LHC peak luminosity was doubled with respect to its foreseen design value, reaching instantaneous peak luminosity $L \approx 2 \times 10^{34}$ cm^{-2}s^{-1}. During Run 2, the LHC delivered an integrated luminosity of about 150 fb^{-1} (see Fig.1), about 5 times larger than in Run 1. This impressive result was achieved in particular due to the average pile-up value $<\mu>$, the number of proton-proton collisions per bunch crossing, ranging from 20 to 60 (see Fig.2), while its design value was $<\mu_{nom}>\sim$ 25.

Fig. 2 Evolution of average pile-up $<\mu>$ during 4 years of Run2 data taking [3].

TABLE I. SPECIFICATIONS OF THE 4 LAYERS AND DISKS

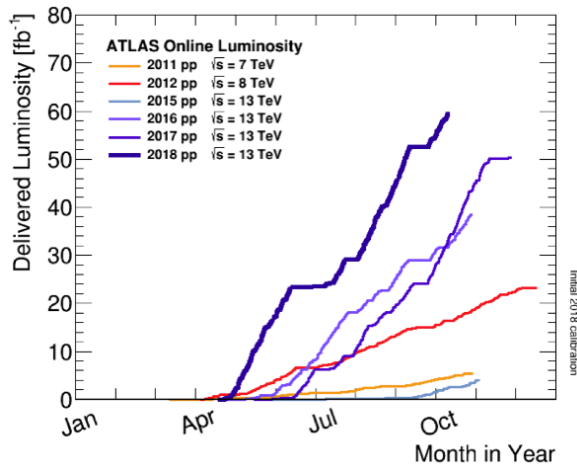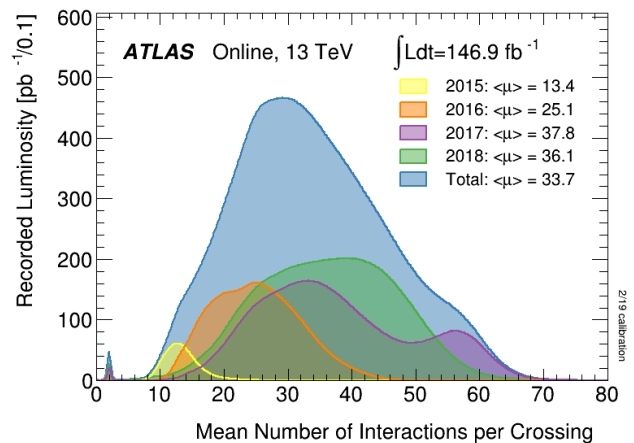|	Outer Layers/Disks (B-Layer, L-1, L-2)	Inner Layer (IBL)
Sensor Technology	n-in-n	n-in-n/n-in-p
Sensor Thickness [μm]	250	200/230
Front-End Technology	FEI3 (250nm)	FEI4 (130nm)
Pixel size [μm^2]	50×400	50×250
Radiation Hardness	50 Mrad	250 Mrad
Chip Size [mm^2]	7.6×10.8	20.2×19.0
Radius [mm]	50.5/88.5/122.5	33

Fig. 1 Integrated luminosity delivered by the LHC during Run 1 and Run 2 data taking. During Run 2, the LHC delivered a cumulative luminosity of 156 fb^{-1} [3].

II. EVOLUTION OF THE PIXEL DETECTOR

The Pixel detector was built with different technologies. The outer layers B-Layer, Layer 1 and Layer 2 and the endcap disks installed in 2007 are built with hybrid pixel modules. Each module is composed of 16 front-end chips FEI3 (250 nm CMOS technology) and a planar n-in-n sensor (see Tab.1).

In 2010 it was decided to add a new innermost layer called the Insertable B-Layer (IBL) [4] with 12 million channels in addition to the existing ~80 million, in order to increase the vertexing capabilities and also in order to provide a redundancy in case of failures of the other pixel layers due to radiation damage.

The IBL, added during LS1 in 2014, is built by modules made of a front-end chip FEI4 [5] (130 nm CMOS technology) and a planar n-in-n sensor in the central region (or 3D n-in-p sensor in the outmost, larger $|\eta|$, module). The detector covers the range of $|\eta| < 2.5$.
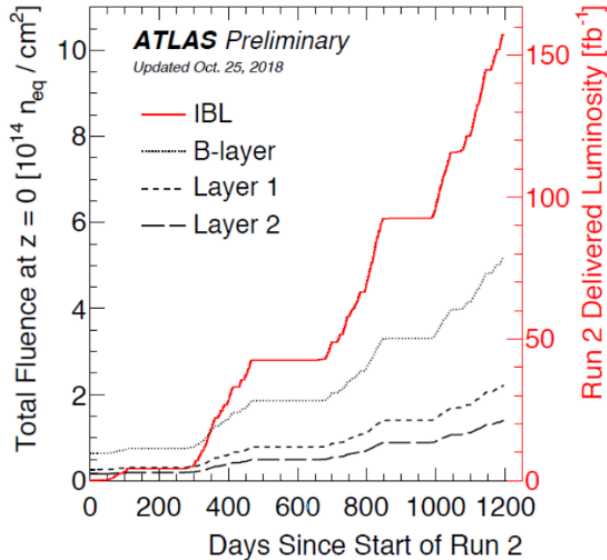

Fig. 3 Simulated 1 MeV equivalent neutron fluence absorbed by the layers of the Pixel detector during Run 2 at $\eta = 0$ [6].

The radiation level is very challenging. The accumulated fluence at the end of Run 2 (see Fig.3), depending on the layer, ranges from 4.5 to 9×10 ^{14} [n_{eq} /cm^2] corresponding to 40-50 % of the total fluence that can nominally be tolerated by the modules.

The new working conditions, dictated by the LHC overperforming with a trigger rate of about 100kHz and pile-up stably above $<\mu> \sim 25$, has necessitated an upgrade also to the Pixel Data Acquisition readout system (DAQ) in terms of hardware, firmware and software. The main limitation for the old readout system was the total bandwidth available of the Pixel SiROD/BOC (Silicon Read Out Driver/ Back Of Crate) boards. A pair of SiROD/BOC constitutes the basic unit of the off-detector electronic. The bandwidth usage increases with rising pile-up, so it was clear that during Run 2, with higher luminosities, the SiROD/BOC pair would have become the bottleneck for the DAQ, increasing the total busy time of the system. A good candidate to overcome this situation was the

pair IBL-ROD/BOC [7]. The IBL-ROD/BOCs were designed for the acquisition system of the IBL in order to sustain higher data throughputs. As of 2015 all the boards (SiROD/BOC) of the readout system for Layer 2, Layer 1, B-Layer and disks were replaced by the newer IBL-ROD/BOCs [8]. The upgrade started in the 2015-2016 LHC Shutdown with Layer 2, whose module readout speed was doubled from 40 Mbps to 80 Mbps. At the end of the replacement the bandwidth limitations were solved (see Fig.4).

Furthermore, the dead time and desynchronization issues were reduced since the beginning of Run 2 through the continuous improvements of the firmware and the software of the readout system (see Fig.5). Further progress is foreseen in terms of data recovery/quality with the deployment of a ROD PowerPC (PPC) equipped with a custom Linux version in Run 3.
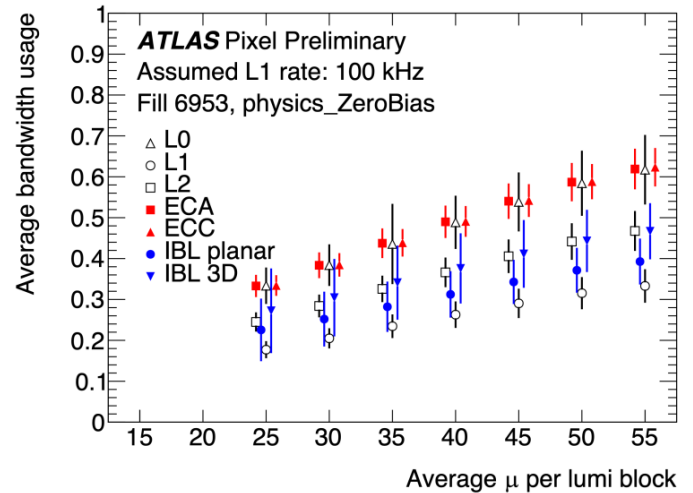

Fig.4 Average usage of the output bandwidth for the four barrel layers (L0, L1, L2, IBL) and the end-caps (ECA, ECC) of the ATLAS pixel detector. The bandwidth usage increases with rising pile-up, so particular attention has been paid in order to avoid saturation and buffer overflow [6].

III. EFFECTS OF RADIATION

Mainly two kinds of radiation damage affect the Pixel Detector: non ionizing damage to the sensor bulk and ionizing damage to the front-end chip [9].

Radiation damage in the sensor bulk affects the electric field profile, which changes the charge collection capabilities. This effect is stronger closer to beam pipe, so it is stronger for the IBL.

In order to partially recover the depletion region and the charge collection efficiency, the bias voltages of the pixel modules were increased several times. Also the analog and the
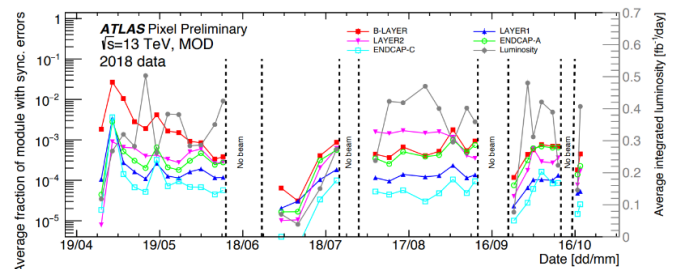

Fig.5 Average fraction of Pixel modules with synchronization errors at the module level per event in 2018 runs [6].

digital thresholds were reduced in order to compensate the loss of charge collection.

ATLAS measured a leakage current (see Fig.6 and Fig.7) that grows linearly with delivered luminosity: this can be described quite well by the Hamburg Model [10], but a scaling factor is required.
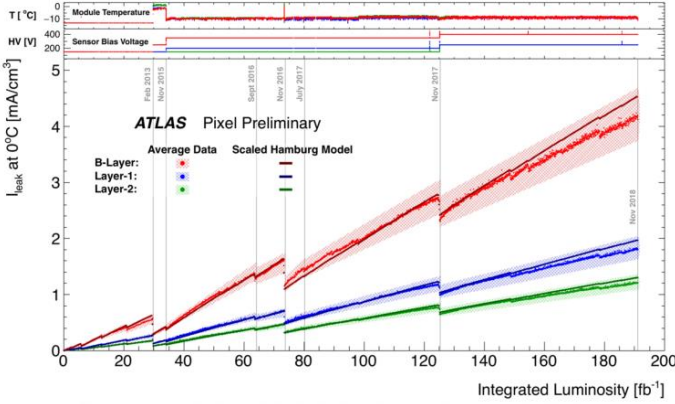

Fig.6 Leakage current in Pixel layers B-Layer, Layer 1 and Layer 2 as a function of the integrated luminosity [11].
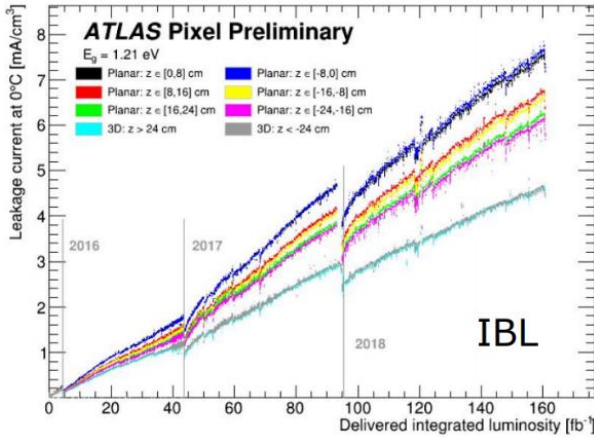

Fig.7 Leakage current in the IBL as a function of the integrated luminosity [11].

Front-end chips of the ATLAS innermost pixel layer (IBL) experienced single event upsets (SEU) in local or global configuration registers (see Fig.8). A misconfiguration in an FEI4 global register leads to a step on LV current consumption of the FE chip, a drop of the module occupancy and a lowering of the data taking efficiency due to the timeout mechanism. Whereas a misconfiguration in a single pixel register can increase the noisy pixels, increase broken clusters and quiet pixels, no major impact is visible on tracking performance. During 2017 a periodic reconfiguration of global registers was implemented (sent every ~5 s). This action counteracts efficiently the dead time induced by the SEU. In addition, in Run 2 a periodic pixel register full reconfiguration was successfully tested (every 11 minutes) and it will be deployed in Run 3.

IV. DETECTOR PERFORMANCE

Although radiation damage is steadily increasing, adjusting the thresholds, (lowering and optimizing depending on the η position), the efficiency of the whole detector is preserved. In particular, since the B-layer (the one that is most affected by the radiation damage) was operating since the start of the LHC at a radius of ~5 cm from the beam, the hit-on-tracks efficiency was kept above 98% (see Fig.9).

The spatial resolution is found to slightly degrade over the Run 2 period as a result of the lower collected charge and the change in Lorentz angle (see Fig.10).
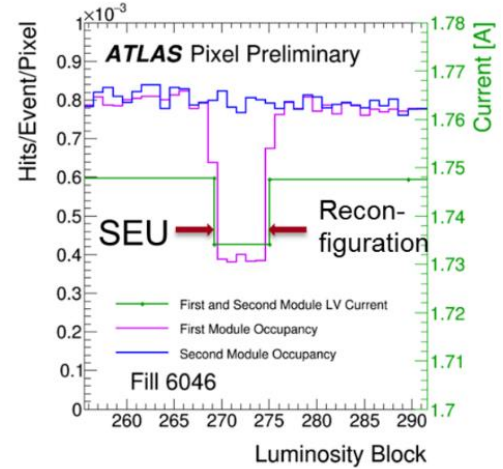

Fig.8 SEU on a FEI4 global register. One ATLAS luminosity block corresponds to typically 60 seconds of data-taking [12].
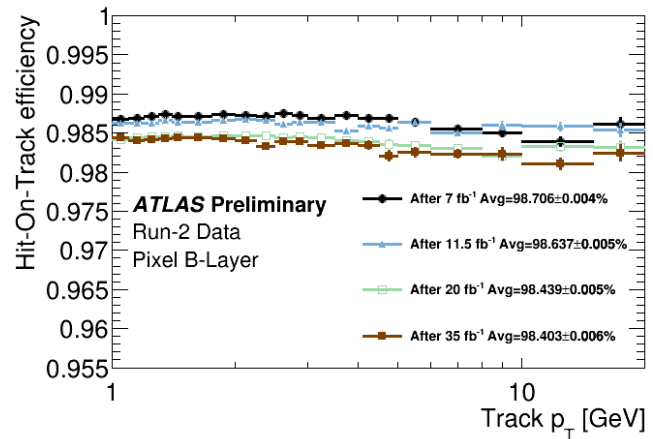

Fig.9 B-Layer Hit-on-track efficiency as a function of track pt, at difference stages of data taking period [6].

The ATLAS Collaboration has presented a new paper on the radiation damage modelling of the Pixel Detector [9]. This document will help the community to understand and prepare the detector for Run 3.

V. CONCLUSIONS

The ATLAS Pixel detector during Run 2 has operated at LHC luminosities and pile-up which exceeded the nominal design values. Nevertheless, the Pixel Detector delivered excellent efficiency and spatial resolution, resulting in an excellent ATLAS global tracking performance. The insertion of the IBL and continuous improvements of the IBL-ROD firmware and software have allowed a better performance to be reached than in Run 1.
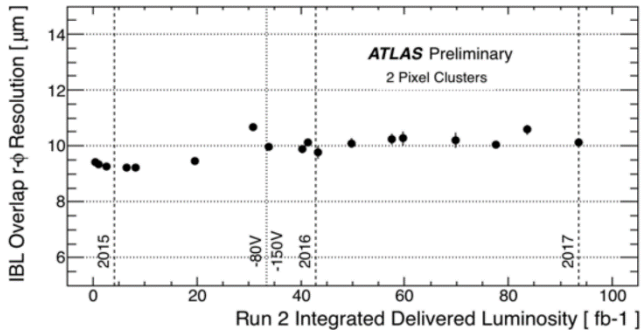

Fig.10 Spatial resolution of the IBL hits associated to reconstructed particle tracks in di-jet events as a function of integrated luminosity [7].

By the end of Run 2 the radiation damage has become perceptible. In order to counteract the performance degradation, bias voltage and thresholds have been optimized. More than 11 years after its first installation in ATLAS and at twice the LHC design luminosity, the Pixel Detector is performing well. By the end of Run 3, the expected delivered luminosity will reach ~ 400 fb^{-1}, a very impressive and challenging scenario for the Pixel detector.

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