Back-end firmware for the LHCb VELO upgrade phase I

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LHCb and VELO Upgrade

LHCb is a dedicated experiment searching for new physics by studying CP violation and rare decays of b and c quarks located in the LHC ring. The LHCb collaboration plans to change key features of the present detectors for Run III, moving to a full detector readout at 40MHz and operating at a luminosity of $2x10^{33}cm^{-2}s^{-1}$. The new readout scheme and operation conditions will require the replacement of many sub-detectors among which is the VErtex LOcator (VELO).
VELO (Figure 1) is the primary tracking and vertex detector that surrounds the interaction point. It will use hybrid pixel detectors (55x55 μm pitch) composed of silicon sensors bump-bonded to new VeloPix CMOS readout chips designed for running at the LHC clock rate, this gives a readout rate around 2.9 Tb/s. The whole VELO will be composed by 52 modules that will have 4 sensors, each one being readout by 3 VeloPix ASICs, mounted in a mechanical frame capable of moving the sensors away from the beams when LHC is not in stable colliding beam mode.

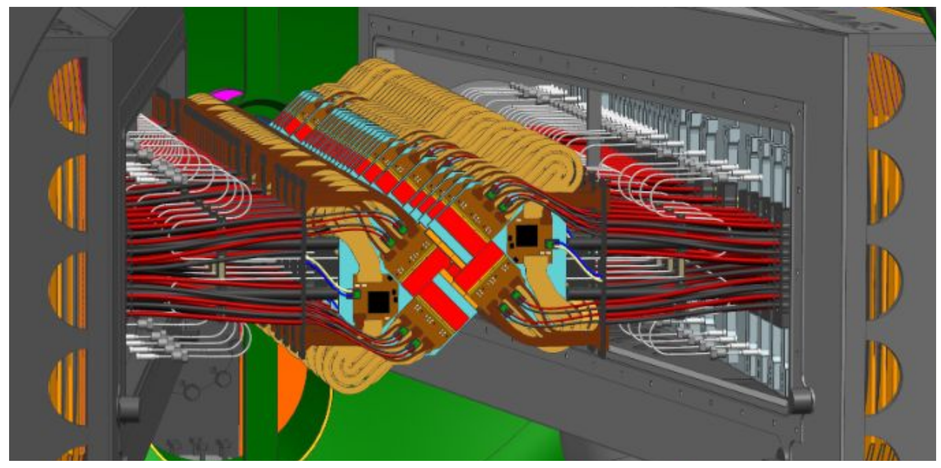

Figure 1: The VELO Upgrade. Each module has four sensors (in red) on a microchannel cooling silicon substrate (blue) and controlled and read out via low mass hybrids and flexible tapes tapes (brown).

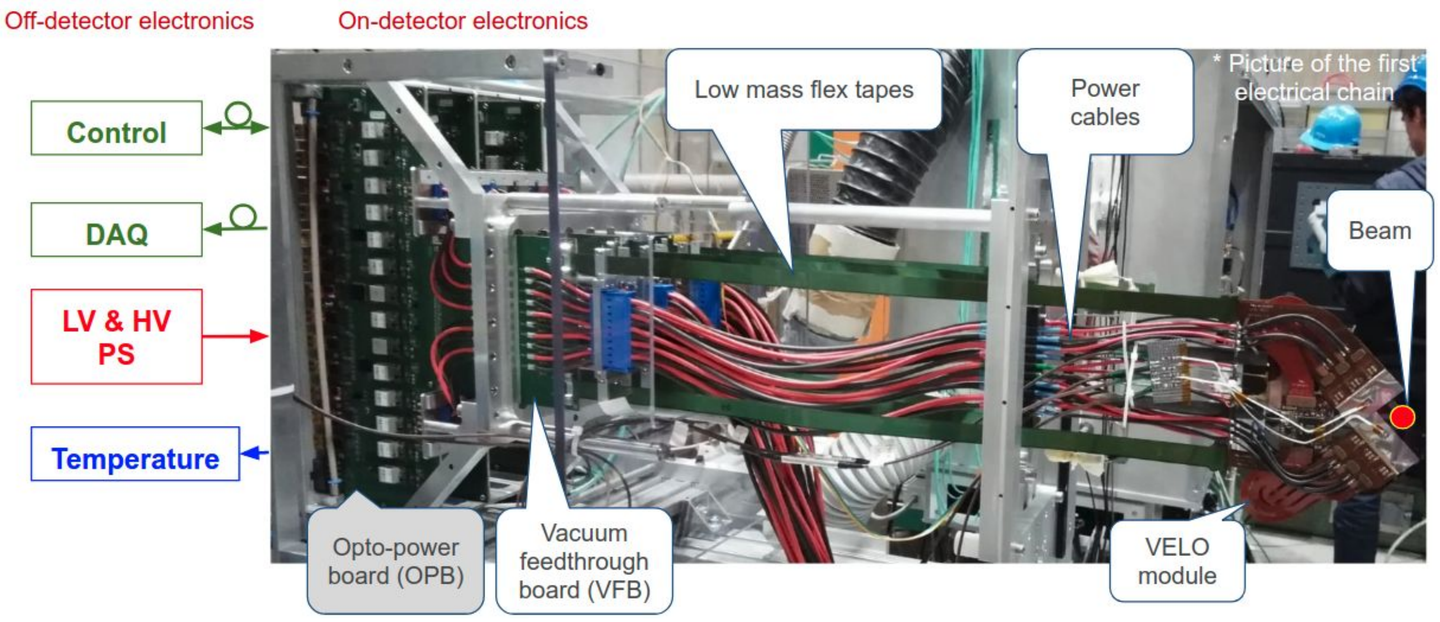

Figure 2: Slice view of a VELO upgrade.

VELO Upgrade electronics

LHCb VELO slice (Figure 2) is composed by a module with 12 VeloPix ASICs controlled over two multipurpose radiation tolerant bidirectional link ASIC (GBTx). Data acquisition links are driven from the VeloPix ASIC over almost a meter of copper transmission lines, converted into optical and send out to the back-end readout boards.

PCIe40

A common back-end board is design to act as supervisor, control and readout board, which is called PCIe40, based on the Intel Arria 10 FPGA and which function is defined by the firmware flavour. PCIe40 board will be controlled and read out from a PCI express slot in a server placed in the surface of LHCb.

VELO control and timing firmware

LHCb sub detector front-ends are controlled in a centralized way. In order to control the front-end electronics, a series of read/write registers in the PCIe40 boards that controls the hardware are accessed from a server that interfaces with the different SCADAs. In the case of VELO front-end ASICs the communication with the server is done by a FIFO memory with 32b bus. The interface between the previously mentioned FIFO and the front-end is done by serializing the word at 80Mb/s and encapsulating it in a GBT frame that goes directly to the GBTx ASIC in the module.
Maintaining the front-end ASICs synchronous with the rest of the LHCb experiment is a key part of this firmware, and it is done with the timing commands. VELO's firmware receives timing commands from the centralized LHCb readout supervisor board (SODIN) and encapsulate it in the same GBT word shared with the control signals and send it to the front-end GBTx ASIC and therefore to the consequent VeloPix ASIC.

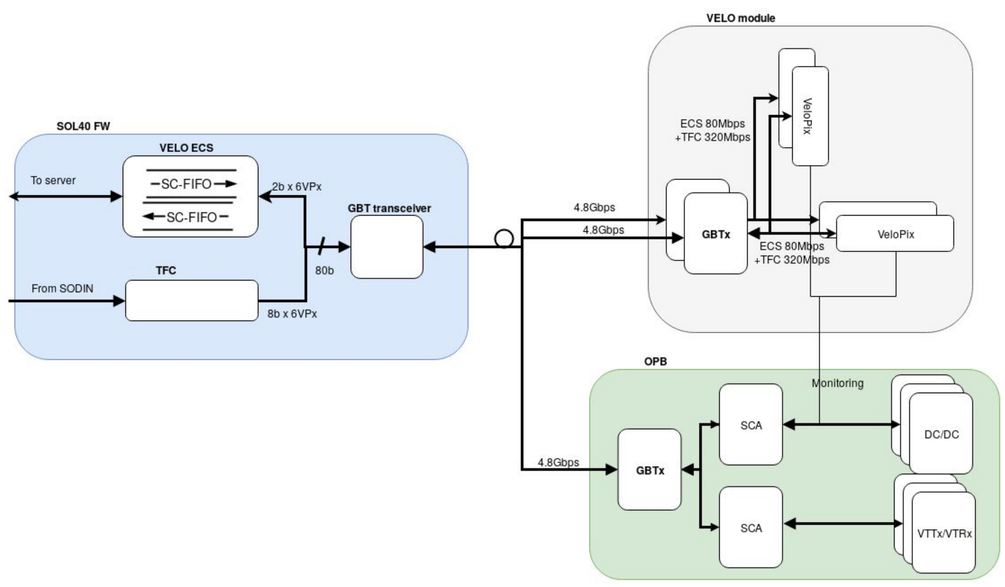

Figure 3: Schematic view of the control firmware for the VELO Interface boards (SOL40) that distributes the control and timing signals to the front-end.

VELO Readout firmware

The VELO readout board firmware is almost a full modification of the common LHCb framework as the VeloPix ASIC is the only LHCb front-end reading out unsorted data over a specific protocol (GWT) created to reduce the power consumption in the front-end ASIC. Hence, this requires a different design separated for the readout board that only shares with the rest of LHCb collaboration the event generation and the PCIe interface. Below you can see the different components of the VELO specific firmware:

- LLI is the first layer of the firmware and is responsible for recover the data from the optical fibers, which is a customised and more extended version of the physical layer (PHY) of the OSI model. As the VELO Front-End ASIC uses its own serializer and protocol, GWT, a VELO LLI needs to be developed by customizing the Intel standard physical medium attachment and creating a new GWT physical coding sublayer.
- Data Processing
  - Pre-router main function is trigger the data taking mechanism, change the clock domain from the 40 MHz of the system to the main data processing clock of 160 MHz and also decode the gray BXID from the VeloPix. The data that is propagated to the rest of the data processing is identified with an ID according to the ASIC of origin.
  - Router, The main processing function of the back-end readout boards for VELO is performed in the router and consists in sorting the VeloPix data by its timestamp in real time. This is forced by the fact that the VeloPix sends unsorted data.
  - Post-router reads the data from the router RAMs, format it with the intel avalon streaming interface (Avalon-ST) with the LHCb run 3 data format that will be fed into the event construction block. Nonetheless, this is not the only function of the post-router, It is also responsible for processing the TFC information associated to the BE board and either discard or accept the right events propagating the valid data synchronously with the event TFC information.
  - ICF (Isolated Cluster Flagging) search to determine if a SuperPixel has a neighbour or is completely isolated. A bit is asserted on the output of each SuperPixel to indicate if It is isolated. The ICF is shown to have a positive impact on the CPU processing of the data in the high-level trigger farm.
  - A real time cluster algorithm for FPGA is being implemented, releasing the computing resources and time from the CPU farm. The design of the clustering is being made keeping a relatively small amount of FPGA resources to make it fit in the PCIe40 board.
  - Back-end board receives the timing information per buch cross from the readout supervisor board and stores it in a RAM memory (TFC RAM). VELO's timing mechanism triggers the data acquisition when the pre-router receives a certain number of synch commands from the front-end, this information is propagated to the post-router where the core of the sync mechanism is implemented. The Post-router sync mechanism reads the information per event from the TFC RAM starting from the synch buch cross and propagates the data according to the content of the RAM.

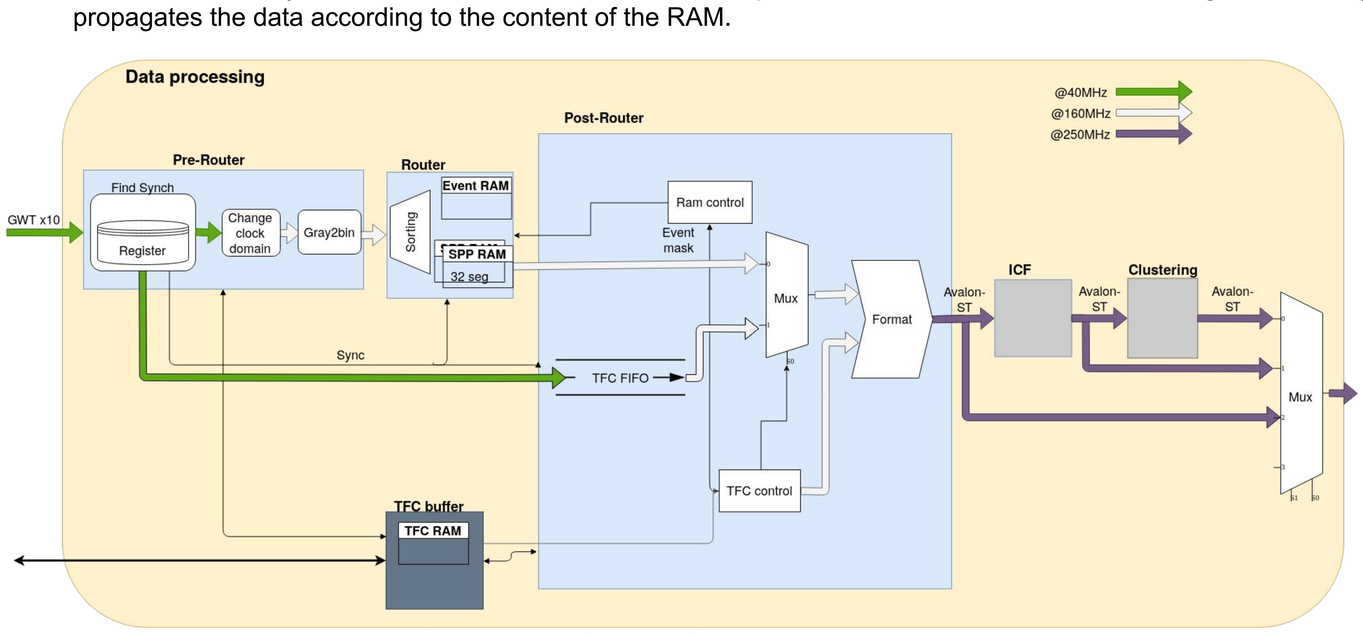

Figure 4: VELO back-end firmware processing scheme.

VELO Bypass firmware

A parallel design to the data acquisition firmware was developed with the aim of having a reliable way of adquire raw front-end data synchronously with the TimePix 3 telescope in a testbeam, besides that this firmware will be used in the module production sites (University of Manchester and Nikhef).
Figure 5 shows the structure of the bypass firmware. It only shares with the final design the VELO upgrade LLI and the standard transceiver for the PCIe40.
The data processing's code is a completely new design. It triggers the reading mechanism of a link in the moment when a TFC sync command is received, packet the frame with the format and store it in a FIFO. The data stored on individual FIFO per link is readed whenever one of the links is receiving data, and the output multiplex the link with higher priority to the link with greater occupancy sending the output data directly to the PCIe interface.
In order to work in the test beam a synchronization mechanism is included. It takes the command that triggers the data acquisition and sent it out from an LVDS output to the Telescope.

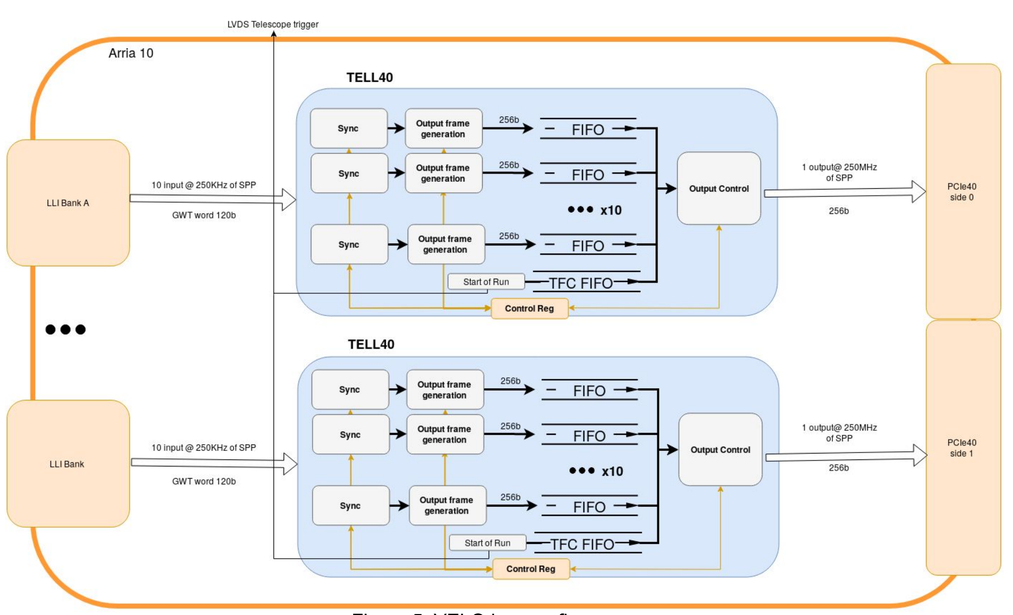

Figure 5: VELO bypass firmware.

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Research project:
-FPA2017-89204-C2-1-P. Búsquedas de nueva Física con el experimento mejorado LHCb del CERN.
-FPA2014-57896-C4-1-R. Desafíos presentes y futuros del experimento LHCb del CERN.