

The challenges faced during the design of the board are summarised below:

- signal integrity
- FPGA power consumption
- FPGA power dissipation

III. jFEX PROTOTYPE

The first jFEX prototype was delivered at the end of 2016 and it was equipped with one Xilinx Ultrascale, XCVU190-2FLGA2577 (pin compatible with the Xilinx Ultrascale+ XCVU9P-2FLGA2577) and the six closest opto-electrical devices. The final jFEX prototype, see Fig. 2 was delivered in November 2017. It is fully equipped with four Xilinx Ultrascale+ XCVU9P-2FLGA2577.

The prototype characterisation was performed in two different test campaigns: at Mainz University and in the integrated test at CERN.

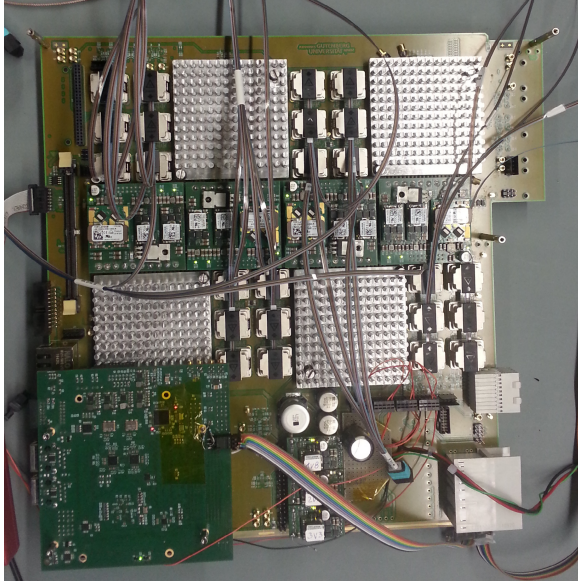


Fig. 2. Picture of the final jFEX prototype.

IV. TEST RESULTS

Once the final prototype board was received, basic tests were immediately performed at the Mainz University Laboratory. A first validation of all the optical and electrical links was done. In February 2018, a full board validation has been performed at the integrated test at CERN where the measurement conditions are very close to the final ones.

To exercise all the jFEX inputs two FEX Test Modules (FTM) [2] were used and the readout links were also verified using the HUB+ROD modules.

Fig. 3 shows the open areas of the eye diagrams for the duplicated data links taken by Xilinx IBERT IPCore. PRBS31 data was sent on optical fibres from FTM (48 links) and from a jFEX transmitter (10 links) to a first jFEX processor, where it was duplicated inside the MGTs (far-end PMA loopback), and sent electrically to a second processor, where the eye

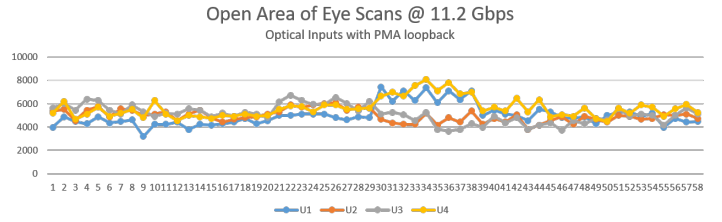


Fig. 3. Open Area of Eye Diagram of all the jFEX input links duplicated via PMA loopback for the four processors. On the x axis the number of the channels per processor are reported while on the y axes the area of the eye diagram in a.u..

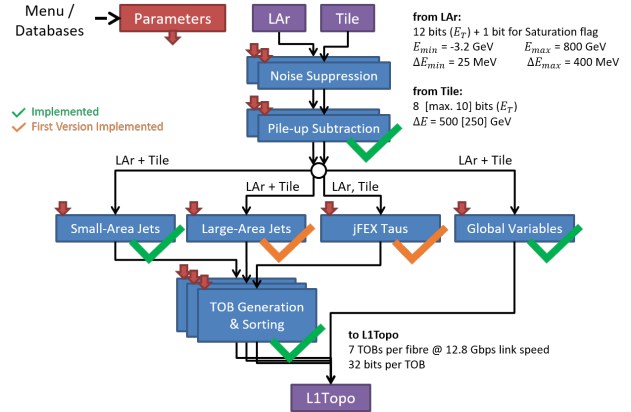


Fig. 4. jFEX Algorithm Block Diagram.

diagrams were measured. In this measurement all input links were running concurrently and a Bit Error Rate (BER) of 10^{-15} was reached.

A dedicated test to assess the quality of the clock on board was performed. A spectrum analyser was used for the clock jitter measurement as the Ultrascale+ clock jitter is specified in the frequency domain.

The proper thermal behaviour of the regulators and of the FPGAs was checked by monitoring them in several conditions of FPGA load and with thermal camera measurements.

V. FIRMWARE

The jFEX will identify jets, taus and global variable with a full calorimeter coverage ($|\eta| < 4.9$). The baseline algorithms shown in Fig. 4 are already implemented (a preliminary one in the forward region) and the FPGA resource usage are 18% LUT in the central region and 47% in the forward region. The forward region, namely for $3.1 < |\eta| < 4.9$, has an irregular mapping in (η, ϕ) therefore more FPGA resources are needed.

The output of the algorithms are sorted internally on the FPGA before being sent to L1Topo.

VI. CONCLUSIONS

The jFEX system is part of the Phase-I upgrade to the ATLAS Level-1 Calorimeter Trigger. The jFEX final prototype has been extensively tested and validated during two test campaigns at Mainz and CERN. The jFEX processes the

data in real-time and without any buffering within a latency budget of <390 ns with fixed MGTs latency including the data duplication on board via PMA loopback.

The jFEX pre-production is imminent and the full production will be completed at the end of the current year. The jFEX system will be installed and commissioned within the ATLAS detector during LS2 before the restart of the LHC for Run 3.

REFERENCES

- [1] ATLAS Collaboration, The ATLAS Detector, JINST 3 (2008) S08003
- [2] "Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System", CERN-LHCC-2013-018. <https://cds.cern.ch/record/1602235>
- [3] "Design and test performance of the ATLAS Feature Extractor trigger boards for the Phase-I Upgrade", W. Qian *et al.*, under press in JINST Proceeding section for the TWEPP 2016 conference.
- [4] "The Prototype of Global Calorimetric Hardware Trigger for ATLAS at High Luminosity LHC", H. Chen *et al.* contribution to the IEEE NSS and MIC 2016 conference Strasbourg.
- [5] www.avagotech.com
- [6] "Upgrade of the ATLAS Level-1 Trigger with event topology information", E. Simioni *et al.* J.Phys.: Conf. Ser. (JPCS), Volume 664, 2015
- [7] <https://www.picmg.org/openstandards/advancedtca/>
- [8] www.xilinx.com