FATALIC: a fully integrated electronics readout for the ATLAS tile calorimeter at the HL-LHC

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Abstract

The ATLAS Collaboration has started a vast program of upgrades in the context of high-luminosity LHC (HL-LHC) foreseen in 2024. The current readout electronics of every sub-detector, including the Tile Calorimeter, must be upgraded to comply with the extreme HL-LHC operating conditions. The ASIC described in this document, named Front-end ATlAs tiLe Integrated Circuit (FATALIC), has been developed to fulfill these requirements. FATALIC is based on a 130 nm CMOS technology and performs the complete signal processing (amplification, shaping and digitization) over a large dynamic range. A dedicated channel for low current is also designed to perform the detector calibration with a radioactive cesium source. The design and performances of FATALIC are described including test beam data analysis.

Keywords: Calorimetery, High luminosity LHC, ATLAS, front-end electronics, ASIC

1. Introduction

In the ATLAS experiment [1], the hadronic calorimeter (TileCal) [2] is crucial to measure the energy of jets produced during high energy proton-proton collisions performed at the LHC at CERN. Indeed, jets with a transverse momentum around 2 TeV will deposit in average 40% of their energy in this sub-detector. This sampling calorimeter consist of approximately 500 000 scintillating plastic tiles and steel plates. About 5500 cells are formed and the light produced in each of them is readout by two photo-multipliers. In the context of the high luminosity LHC, the readout electronics has to be upgraded because of the level of radiations and the high collision rate.

2. Principle of the detection chain

The light produced by the tiles is transported to the photo-multipliers using optical fibers. A current $i(t)$ will be then delivered by the photo-multipliers which have to be readout, shaped and digitized before being sent to the off-detector electronics. In this upgraded scheme, each photo-multiplier has its own front-end card hosting the FATALIC chip which performs the signal processing as well as power supplies and controls. The photo-multiplier together with its front-end board are fit in a tube, called photo-multiplier tube (PMT). As shown in Figure 1, the smallest mechanical structure contains 12 PMTs and the two associated on-detector electronic boards which allow to prepare the 12 FATALIC outputs to be sent to the off-detector electronics, where the signal reconstruction is performed.

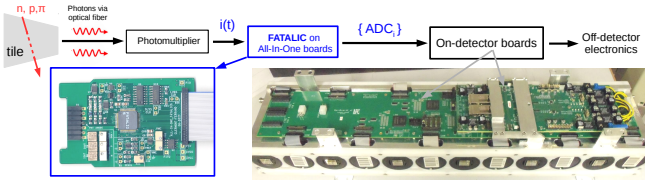

Figure 1: Schematic view of the detection chain. Each of the 12 circles is a tube containing a photo-multiplier and its front-end board with the FATALIC chip.

3. Overview of FATALIC readout

FATALIC architecture is based on CMOS technology and is graphically depicted in Figure 2. The signal is distributed to the fast channel (20%) and the slow channel (80%). In the fast channel, the signal is read by 3 current conveyors with relative input impedance 1/8/64, each followed by a 25 ns shaper and a 12-bits pipelined ADC with a 40 MHz sampling rate. Due to bandwidth limitation, FATALIC can only deliver two of the three gains (the medium and either the low or high gain, based on gain saturation). This sample-by-sample gain selection is made in the digital block of Figure 2. The above design establishes an effective 18-bits output range, over the whole dynamic range of the input charge: 12 fC - 1.2 nC. The slow channel is designed to read low current signal, produced by the ^{137}Cs source used for the absolute calibration [3] of the TileCal. The input charge range (0.5 nA - 1 μA) is handled by a current conveyor followed by a 100 μs shaper and a 12-bits ADC of with 833 kHz sampling rate.

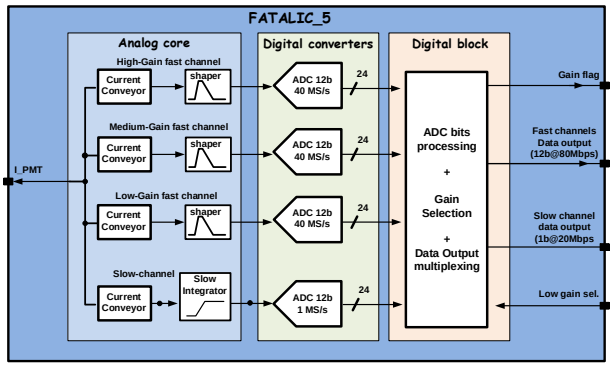

Figure 2: Schematic of FATALIC.

4. Results and performances

The intrinsic properties of FATALIC were measured in a lab test bench. The noise is found to be 6.2 ± 0.2 fC and the non-linearity corresponds to $-0.03 \pm 0.02\%$ for an injected charge of 800 pC, fitting well the specifications for physics signal processing (noise lower than 12 fC, non-linearity below 1% at 800 pC). However, the noise of the integrator dedicated to the calibration is 6.5 nA, being larger than the required precision of 0.5 nA which is due to the flicker noise of CMOS technology.

FATALIC was also tested using beam of electrons, pions and muons of energies ranging from 20 to 100 GeV. The energy deposited in each cell is reconstructed using an optimal filtering. Figure 3 shows the distribution of the reconstructed energy for beam of 50 GeV electrons of a limited purity. The electronic noise (pedestal) is well separated from the smallest signal coming from muons.

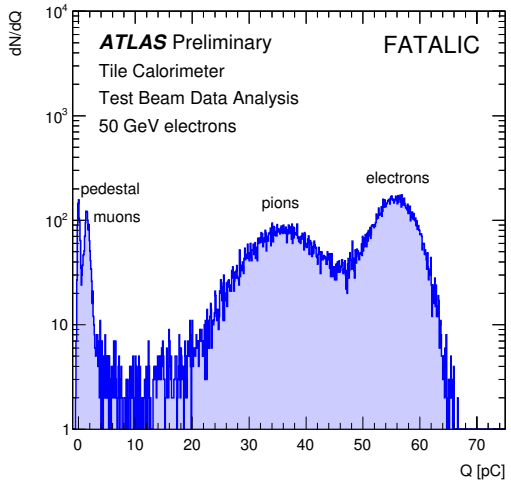

Figure 3: Energy distribution measured by FATALIC in test beam conditions at CERN. The charge Q is the sum of energies measured by two cells (four PMTs), corresponding to a retro-projective tower with $0.3 < |\eta| < 0.4$. The scale is approximately 1 GeV for 1 pC [4].

A simulation study was performed to assess the impact of additional interactions per bunch crossing (pile-up μ). Energy deposits from pile-up are added at the cell level on top of the in-time signal, changing the pulse shape. The energy reconstruction is then applied on the distorted pulse and the energy resolution (RMS of $E^{\text{cell}}_{\text{Reco}} - E^{\text{cell}}_{\text{True}}$) is studied as a function of the true cell energy from 100 MeV to 1 TeV for different pile-up benchmarks, as shown in Figure 4.

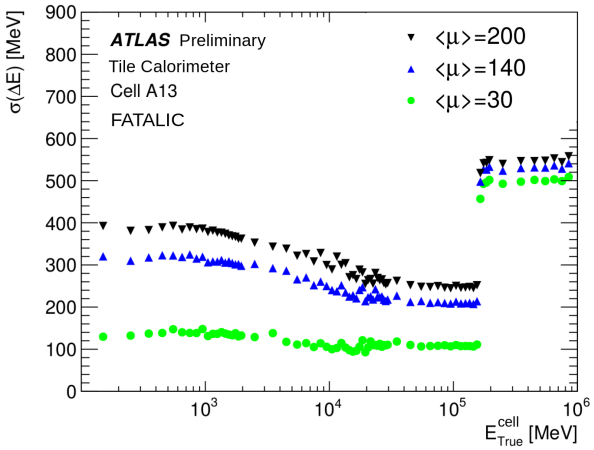

Figure 4: Simulated energy resolution at the cell level for different pile-up scenarios. The cell energy $E^{\text{cell}}_{\text{True}}$ is the true energy deposited in the cell by in-time particles (not from pile-up). The jump at 200 GeV corresponds to low gain samples, mostly dominated by electronic noise [4].

5. Conclusions

FATALIC is an integrated circuit able to perform the entire physics signal processing for the ATLAS hadronic calorimeter. The measured performances in lab and during test beam are well within specifications except for precision on the calibration signal due to intrinsic limitations of the CMOS technology.

References

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