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A 20 cm² CCD Mosaic Camera
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1 Introduction

As explained in the companion paper [1], our aim is the search for Massive Astrophysical Compact Halo objects (MACHOs) in the halo of our Galaxy. A method to detect such objects was suggested by Paczyński in 1986 [2] using the gravitational microlensing effect, a brightening of stars when a MACHO passes near their line of sight. For this purpose one monitors for several months a large number of stars ($\sim 10^5$) in the LMC, in the outer reaches of the halo of our Galaxy, with a frequent sampling of their brightness. This is achieved by placing a large area sensitive detector at the focal plane of a telescope. As such a detector was not available, we decided to build a large CCD camera.

We first present briefly the whole set up before describing in detail the read-out and control system of this camera (Fig. 1). The detector itself is made of a mosaic of 16 Thomson THX 31157 CCDs. Each CCD has 579×400 square pixels, of $23 \mu m$. These CCDs are three side buttable and are disposed on 2 rows of 8, giving a sensitive area of $73 \times 27 mm^2$. This detector is placed at the focal plane of a F/10 catadioptric reflector with 40 cm of clear aperture. This instrument is supported by a dual 40 cm refractor (GPO) used as guiding telescope by means of a second, intensified, CCD camera. In order to minimize the weight of cables and avoid problems of ground loops all the read-out and command system of the CCDs is located near the focal plane. All the parameters of CCDs are computer-controlled, as are the shutter and filter system, focus control, temperature and position monitoring. The link between the telescope and the VME based 68030 computer is made by two optical fiber pairs. All CCDs are read in parallel by two DSP processors (MC 56001), one per group of 8 CCD. A readout time of 42 seconds is achieved by this system for the acquisition of nearly 8 Mbytes of data.

2 Analog CCD signal processing

The Thomson THX31157 CCDs are glued on a ceramic substrate and have all their connection pins located on one side (the other 3 are buttable). The electrical connection is made by a 10 cm long kapton flexible printed circuit terminated by a 14 pins connector. This connector plugs directly in a small printed circuit board located below the CCD cooling plate. This PC board, one per CCD, supports low-pass filters on all powering and control CCD electrodes, and the first stage of the amplifier.

A dual AC coupled amplifier with differential output ensures a gain of 20 for the CCD output signal (Fig. 2). Amplifiers are very low noise chips, $5 nV/\sqrt{Hz}$ at 10 kHz, in military grade (NE 5532 A) for a large working temperature range. A specific DC/DC converter is used to power these amplifiers in a very quiet manner. A second connector, vacuum resistant, ensures the liaison with the control base, one per 8 CCDs, located outside of the cryostat vessel. On the first prototype, a sensor

was glued on amplifier chips to monitor its temperature; it was found that due to the good vacuum in the cryostat and the metallized nylon "super insulating aluminized mylar" the case temperature never fell below -10°C despite the proximity of the copper thermal link driving heat from the CCDs to the LN2 vessel. We chose to use a differential output amplifier in order to protect the signal against noise from other CCDs and the environment (fig 2).

Outside the cryostat vessel, a small box contains all the signal processing equipment as well as driving and control electronics for 8 CCDs.

The differential signal issued by the in-cryostat amplifier is received by a two stage NE 5532 amplifier with gain and offset control. One stage provides a variable 1.5 gain in order to adjust the gain of all CCDs at roughly the same value despite device dispersion. Offset control places the DC level at the input of an ADC, near the middle of the conversion range. This allows keeping a sufficient dynamic range to eliminate false coding due to DC fluctuation introduced by the AC coupling of the amplifier, mainly at high illumination levels of a large number of pixels (i.e. for field exposures).

The output of the amplifier goes to a 16 bit ADC with embedded sample and hold circuit (AD 1380 KD). The conversion time is $15\ \mu\text{s}$, and the method to extract signal from CCD is dual digital sampling. After resetting the CCD read-out diode, a first Analog to Digital Conversion is made, and the result is read by the DSP which stores it as reference level in one of its internal memories. The pixel content is shifted out, the CCD is read again, a second A/D conversion is made; the DSP subtracts the first read from this value and sends the result to the storing device as the content of pixel n after checking the validity of the result ($0 > C_n > 65535$).

3 Driving and control electronics

The Thomson THX31157 CCD has a frame transfer organization using 4 clocks for the image zone (line transfer) and 2 clocks for read out register (pixel transfer), and a reset clock. In addition a total of 6 power supplies or biases are needed to run the device. As we use 16 CCDs at the same time we chose to have all these computer controlled. Each CCD is driven by a PCB, $80 \times 109\ \text{mm}^2$ in size, supporting both analog devices (amplifier and ADC previously described) and all the control circuits. These 8 PCBs are plugged on a mother board supporting also a DSP card and a card with DC/DC converters for powering amplifiers and ADC. Special care was taken in the design of the different cards to separate well analog and digital ground planes. We manage also some shielding facilities to protect the analog section from pickup. The MC56001 controls all the functions for the 8 CCDs. It receives orders from the VME control computer and returns results by the optical link at the speed of 70 Megabit/sec. Fig. 3 shows the block diagram of a CCD driving card, and fig 4 is a photographic representation of such a card.

Power supplies and Biases

For each CCD there are two octal DAC (8 bits) with internal latch (one for positive only biases and one for positive or negative voltages) followed by buffers with the adequate gain. A voltage reference automatically switched off at power up, is enabled by the DSP after writing data in all the DAC registers. This is to protect CCDs against dangerous voltages at power-up time and to manage the possibility of disabling one or more CCD for test purposes. Two 8 bits ADC can read all these voltages and report readings to VME. There is a total of 10 voltages generated and monitored in this way : 4 for biases and 6 for High and Low level of clocks.

Clock generation and timing

In the CCD control card there is a "pattern Register" of 8 bits. Each clock is associated to one bit of the register. When a bit is "true" the corresponding clock is at High Level, when the bit is "false" the clock is at Low Level. This is done using an analog switch receiving on one side High Level voltage and Low Level on the other side and driven by the Pattern register bit state. All the clock levels are generated by DACs like the biases. The slope of each clock can be adjusted by a RC circuit (with the Thomson THX31157 -2 phases transfert device-, we have to adjust the cross-point between two consecutive clocks). Each clock uses 2/4 of Hi 201 HS quad SPST analog switch with a series ON-channel resistor of 30 ohms and a fast switching time of 50 ns. As the clock speed of the DSP is 10 MHz, the system can modify clock states every 125 ns. Faster clock rates are incompatible with low noise readouts. Configuration sequences are stored in a FIFO memory and each byte is transferred from this FIFO to pattern registers by a read cycle of DSP which is seen as a write cycle by pattern registers.

A part of the software on the VME computer allows the operator to modify and to "draw" directly the clock patterns on the control terminal. Each control sequence can be stored in a file on the control computer and can be called at any time and loaded in the DSP FIFO. In normal operation one uses three such sequences, one acquisition sequence, one cleaning sequence used before each exposure and one sweeping sequence running automatically during camera inactivity periods to prevent saturation of CCD wells.

In the same way, "voltage files" can be stored and loaded for each CCD. This facility is very useful during the CCD optimization period. The remaining bit of the "Pattern Register" is used to generate the start conversion signal for the ADC. To minimize the risk of noise induced from DSP bus activity to the ADC, this start conversion signal is delayed by 2 μ s to avoid any logic activity during CCD signal sample and hold, and conversion.

4 Data acquisition

4.1 System architecture and organization

The core of the read-out system is a VME crate located in a counting room 25 meters away from the telescope. All the computing power in this crate is provided by a Motorola 147 VME card. This card includes a 68030 processor chip, 4 Megabytes of memory and interface for RS232, Centronics, SCSI and Ethernet LAN. The VME crate is connected to the two DSPs through optical fiber links.

Especially made "Host" modules, one per DSP, plugged in the VME crate, allow the VME CPU to write or read the DSP registers through the optical fiber link. Moreover, the VME CPU can load programs in the DSP and control the execution.

In addition, during the CCDs readout, the DSP writes directly in picture memory through the optical fiber link thanks to this "Host" module. The processing power of the DSP 56001 allows to compute the address of each pixel in order to unscramble the picture. Being done in software, this operation is easily modifiable to fit all or any part of the CCDs mosaic. It has the disadvantage of transmitting on the optical fiber link not only the 2 data bytes but also the 3 address bytes for each pixel ; however the DSP is powerful enough to allow this scheme which increases the safety of the link.

In order to eliminate bus arbitration problems on VME crate, the transfer "Host" module/picture memory is made by the VSB bus. There are two VSB local buses, one per group of CCDs which ensure the parallel readout of both CCDs groups.

Each picture memory is a 16 Megabytes dual port (VME/VSB) board able to store 4 pictures (fig.5). The VME CPU reads these memory boards through the VME bus and writes the processed data in FITS format to SCSI devices (1 Gigabyte hard disk and DAT). Pictures are displayed on a 1280 × 1040 pixels high resolution color display.

In addition, other VME cards allow the acquisition system to drive motors (focal plane, filters, shutter), and to check the temperatures of some critical points in the cryostat. A DEC 5000 workstation is connected to the VME through Ethernet for image processing (bias subtraction and flat-fielding).

4.2 Control software

Thanks to the operating system OS9 installed in the M147 CPU, the software has the following features:

- it is developed and maintained directly with the Acquisition hardware itself (no cross-compilation),
- multitasked: control dialog, camera acquisition, visualisation, archiving, ... may run simultaneously with their own schedule. Multitasking is transparent for the user.

The main characteristics of the software developed for this experiment are:

- user friendly interface : menus for any user action, panels of input-controlled variables, on-line subject-related help,
- wide range and levels of domains accessed: from the debugging of the camera electronics and mechanics to the automatic fully-integrated calibration and data acquisition and the normal simple operation (snapshots, individual archiving, survey of hardware parameters ...) including the pre-analysis features (histograms, profiles and image treatment).

Domains and levels of operations

The menus, panels and message library (called OPIUM) involve a modular and simple way of programming, and allows a dialogue by pull-down menus. Hence this allows any extension of the software whatever its previous state. Consequently, all the actual possible operations about the Acquisition System (hardware and software) are accessed from a unique general control task (called CONTROL in figure 6): the user has a unique "work station" and not a multiple computer system; every information, as entered once by a user, is internally shared between all the other tasks which need it. At the lower debugging level, the domains accessed through CONTROL are:

- the DSPs: programs, control, checks,
- the CCDs: definition of the signals used to drive them (timings and voltages) , control,
- the setup for the software itself (files for default timings, voltages and DSP programs, definitions of the filters, common header for the FITS files,...).

At the level of normal manual operation the domains are:

- status (and if necessary start) of the camera electronics (not including commands for debugging),
- display of hardware parameters,
- visualisation: parametrisation for automatic mode, requests for individual pictures,
- control at the picture level: parametrisation (filter, exposure time, type of picture), start of a picture, suspend/restart, abort/stop the current picture,

- analysis of the picture : histograms, profiles, statistics about parts of pictures, star fitting, seeing control and whatever the operator may want to add to the existing set of commands,
- archiving: parametrisation, read/write of one archive, management of the archive supports (mainly the menu-driven cleaning of the disk and DAT),
- the higher level of the control is the "fully automatic integrated operation",
- calibration of CCDs noise and gain computation,
- focus fitting (integrated but user-controlled),
- data taking.

Hence the Software covers the debugging, the slow-control, the data acquisition and some analysis tools.

The user interface

A specific user interface has been developed according to the following conditions:

- a low-cost hardware: although the full CCD mosaics has to be displayed with a large high-resolution specific display, only one VT200-type terminal (with a graphic window emulating a Tektronix 4014) is used to drive the user dialogue; note that this interface has been slightly modified in order to use indifferently a high resolution display or a X terminal.
- a system easy to use for non-specialists,
- a library easy to use by an overloaded programmer.

The multitasking

The multitasking of the acquisition system has been implemented in order to allow the user to start commands and keep control for other requests during the execution time of the previous command. Synchronisation of the tasks is done internally through global system data (implemented in OS9 by data Modules). A particular task (SYNCHRO in fig 6) is devoted to achieve the various combinations of connections between tasks. From the user's point of view the status of the tasks is simply reported in the control display. A user command issued from the CONTROL task is generally transmitted directly to the appropriate task. At completion time, this task generates a report message to the SYNCHRO task, which in turn may generate one or more new command messages to the same or to other tasks, depending on the different control parameters as set by the user with the menus and the panels. Since a particular layer of the software is dedicated to communication between tasks, the software may be used with other communication protocols, allowing it to run in a multicrate environment.

5 Performance

A first quantitative test was performed at La Silla Observatory (ESO) in December 1990 with a single CCD camera borrowed from the Observatoire de Haute Provence. The camera was equipped with a Thomson CCD with similar characteristics to those of the THX 31157 used for the final camera. Minimal requirements for the performance of the camera mosaics were deduced from this first test. As the available time to optimize 16 CCDs was very short, the tests were generally stopped when the minimal requirements were reached.

CCD noise

The shot noise due to sky photons for an image of the LMC bar is quite large (8 to 35 electrons). The total CCD readout noise for an image is due to several contributions : on-chip and off-chip preamplifier noise, noise induced by clock signal and DC voltages and noise of poorly understood origin. The dark current of a room temperature CCD is of the order of 10^6 electrons/sec per pixel; its contribution becomes negligible if the CCD is cooled at -100°C .

A method based on image subtraction on n pixels allowed to compute the variance of the noise distribution under the ergodic hypothesis. Images taken without illumination give directly the noise. Images taken with a fixed amount of light at different exposure times allow to extract, for the entire electronic chain, the gain (i.e. the number of electrons per ADC unit), the output noise in electrons, and the linearity of each of the 16 CCDs.

To measure the gain, we use, for an average signal on the CCD, the relation :

$$\sigma^2 = \frac{1}{g}\bar{S} + \sigma_{noise}^2 \quad (1)$$

where \bar{S} is the average signal level in ADU, σ^2 is the variance of the signal noise in ADU, σ_{noise}^2 the variance of the noise in ADU and g , the gain in electrons per ADC unit. Relation (1) assumes that photo-electrons obey Poisson statistics, i.e. the variance of the distribution is equal to its mean. The variance plotted versus \bar{S} for different exposure times is linear, the slope giving the gain and the extrapolated intercept giving the noise.

A logarithmic expression deduced from (1),

$$\text{Log} \frac{\sigma^2}{\bar{S}} = \text{Log} \left(\frac{1}{g} \right) + \text{Log} \left(1 + \frac{\sigma_{noise}^2 \cdot g}{\bar{S}} \right) \quad (2)$$

should behave as a constant ($\text{log} \frac{1}{g}$) when \bar{S} is not too small.

Several measurements were performed in the laboratory using a uniform lighting of the CCD array, after bias level and cosmic ray events have been subtracted on the frames. After some optimisation of CCD DC voltages and of filtering cells on those voltages, a global readout noise of 12 electrons was obtained in an experimental configuration using a single CCD. The full array of 16 CCDs was then tested. The

average readout noise was found to be higher ($\simeq 20$ electrons) than for the single CCD experiment (12 electrons) (fig 7a).

Cross-talk

As the 16 CCDs run synchronously, saturated columns or pixels on any CCD can induce cross-talk on the other channels by some coupling between signal lines. Some care was taken to shield the signal lines from the CCDs to their preamplifier, and shielded twisted pair cables were used between the preamplifiers and their associated A/D card located outside of the cryostat. Cross-talk has been observed at a negligible level (10^{-4}) between the 8 channels whose A/D cards are located on the same side of the cryostat.

CCD gain and linearity

The average gain in ADU per electron has been computed from relation (2). The inverse of the gain is about 6.4 e/ADC count, in average. The photometric response of the CCD remains linear (fig. 7b) in the measured range (0-130000 electrons per pixel) at the level of 10^{-3} , as given by linear fits. At the beginning of data taking on the sky, linearity tests were performed using samples of image stars taken at different exposures.

Transfer and quantum efficiencies

When the readout is performed, the last pixel in a 580 x 400 CCD undergoes 980 transfers. A fraction of the original charge could be left behind during transfer. A systematic measurement has not been performed. It has been checked by over-scanning a CCD, both on rows and columns that the transfert inefficiency effects were negligible at the level of the required photometric accuracy. The optimum full well capacity was tested using images of very bright stars. The quantum efficiency has been measured on one CCD by the Laboratoire d'Astrophysique de Toulouse [3] Fig. 8 shows the results of the measurement.

CCD defects

The Thomson THX31157 CCD delivered were quite free of defects like hot or inefficient pixels. During the initial phases of cooling to -100°C , saturated columns (1 to 6) appeared on some of the CCD without illumination. Several tests were performed, the amount of charges stored in the saturated columns showed a small dependence on the relative levels of parallel and serial clocks used to transfer the charge. The effect could be explained by an injection of charges during the parallel transfer to the output register due to some dislocations in the Si crystal made during the first coolings.

6 Conclusion

To summarize, the readout and the control system of the CCD mosaic camera are running since December 1991 at the La Silla Observatory (ESO). The overall performance of the camera has been good. About 12000 pictures (data and flat-fields) have been successfully registered up to now. We will report in the near future preliminary scientific results of the EROS experiment.

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Figure captions

Figure 1 - Overview of the instrumental system.

Figure 2 - Scheme of the analog signal processing chain.

Figure 3 - Block diagram of a CCD driving card.

Figure 4 - Photographic representation of a CCD driving card.

Figure 5 - Block diagram of the data acquisition.

Figure 6 - Diagram of the acquisition system tasks.

Figure 7 - a) readout noise in electrons for the 16 CCDs.
b) photometric response in ADU of all the CCDs as a function of exposure time.

Figure 8 - quantum efficiency of a CCD THX31157 as a function of wavelength.

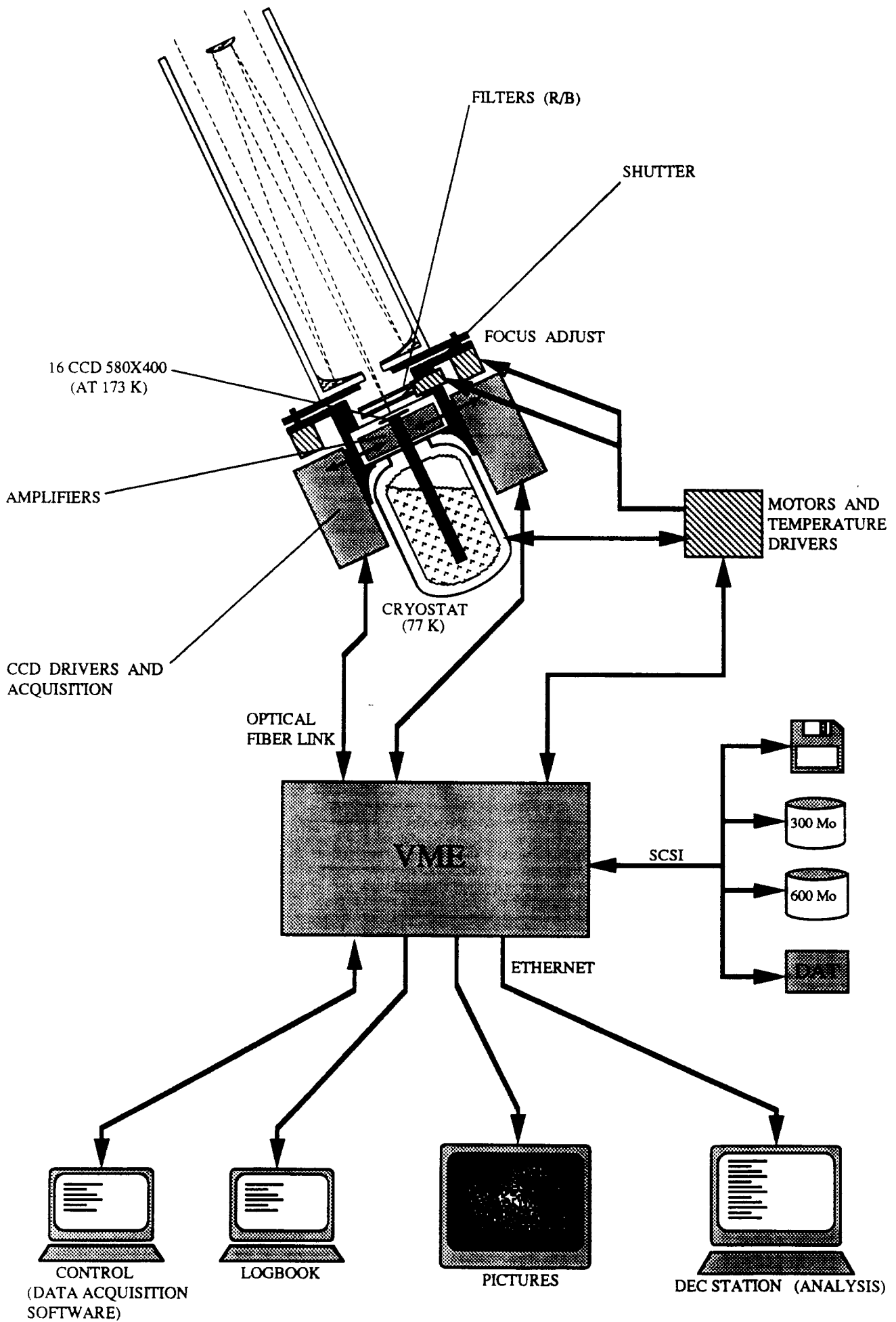


Fig. 1

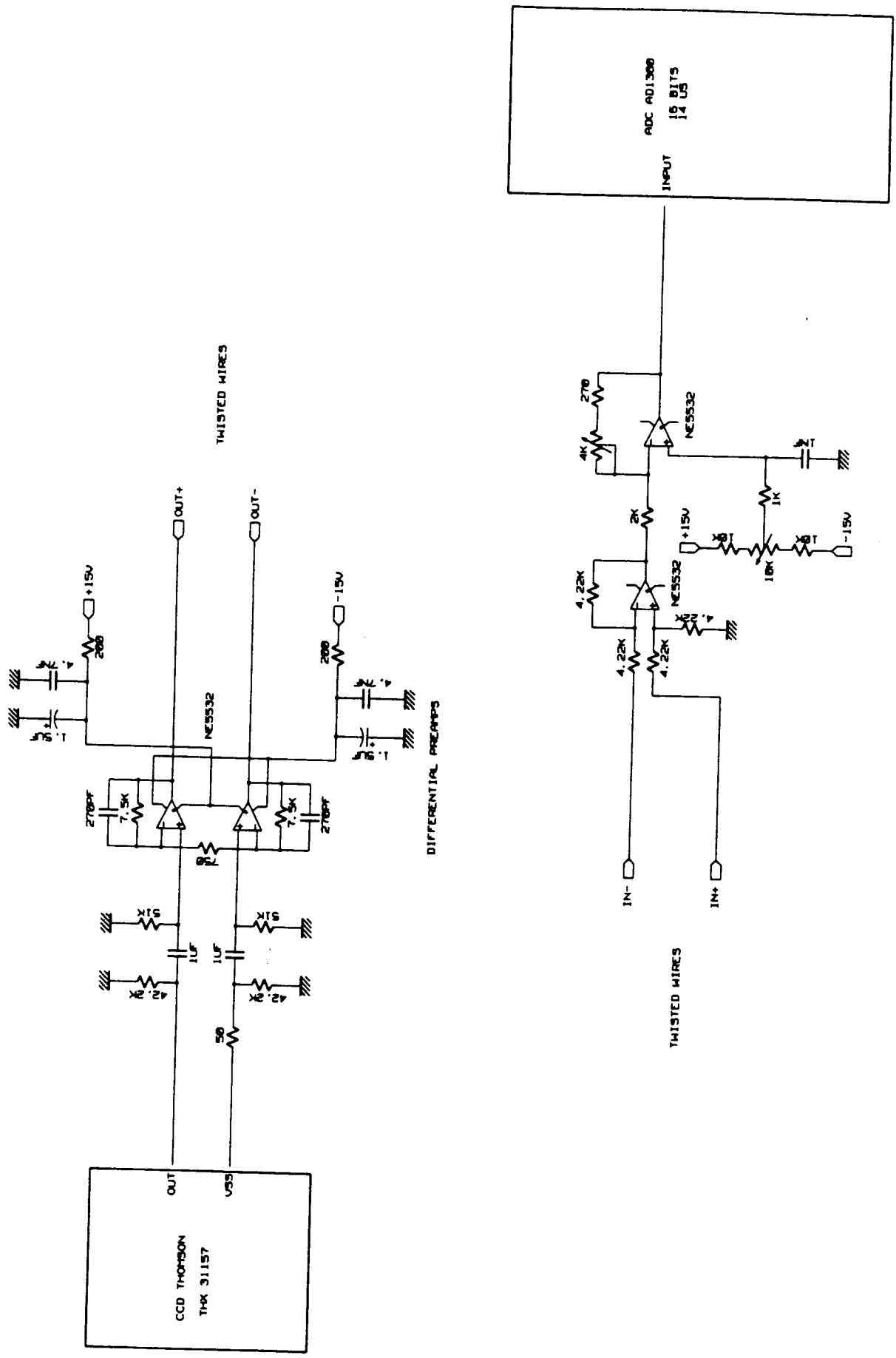


Fig. 2

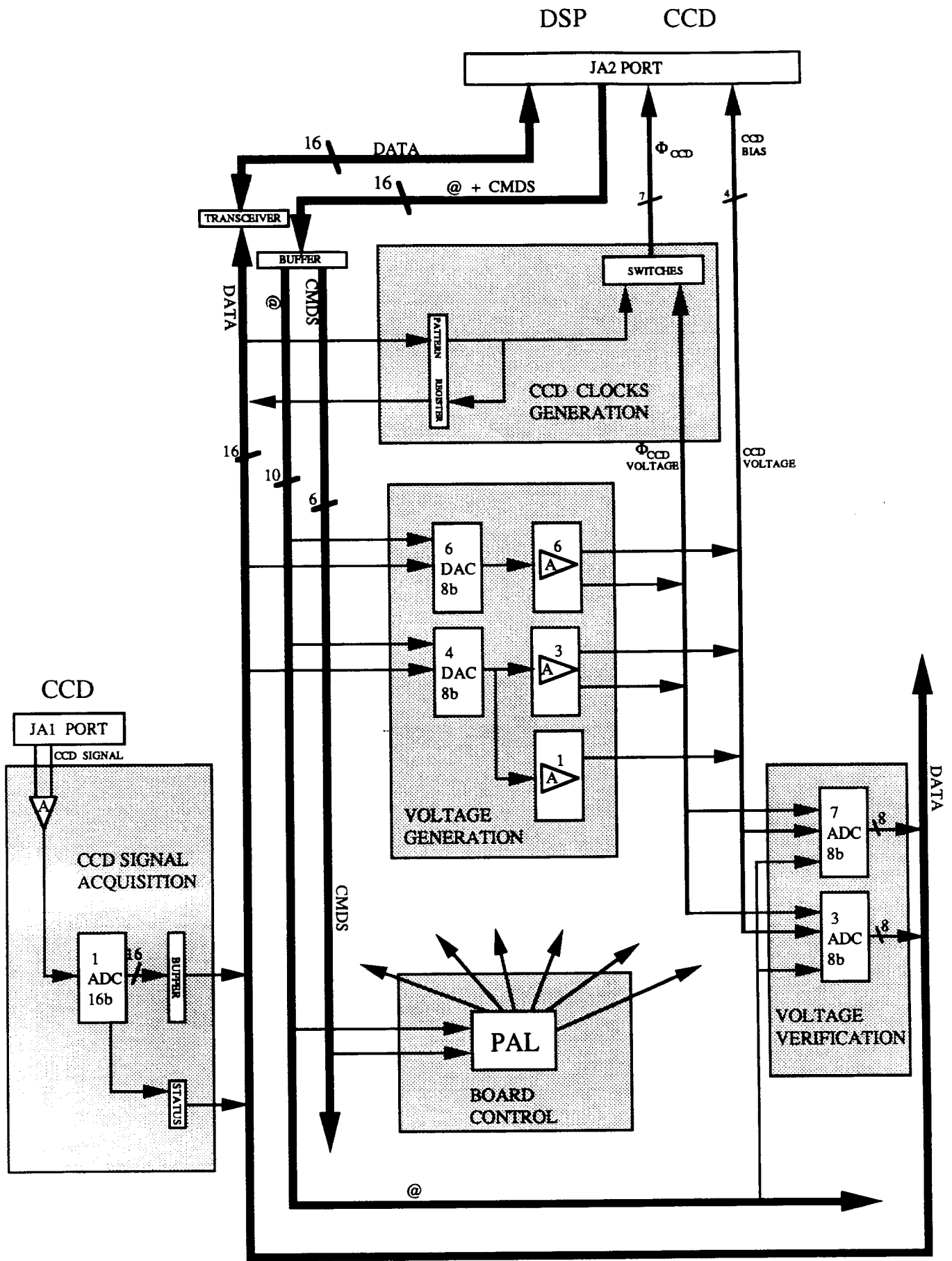


Fig. 3

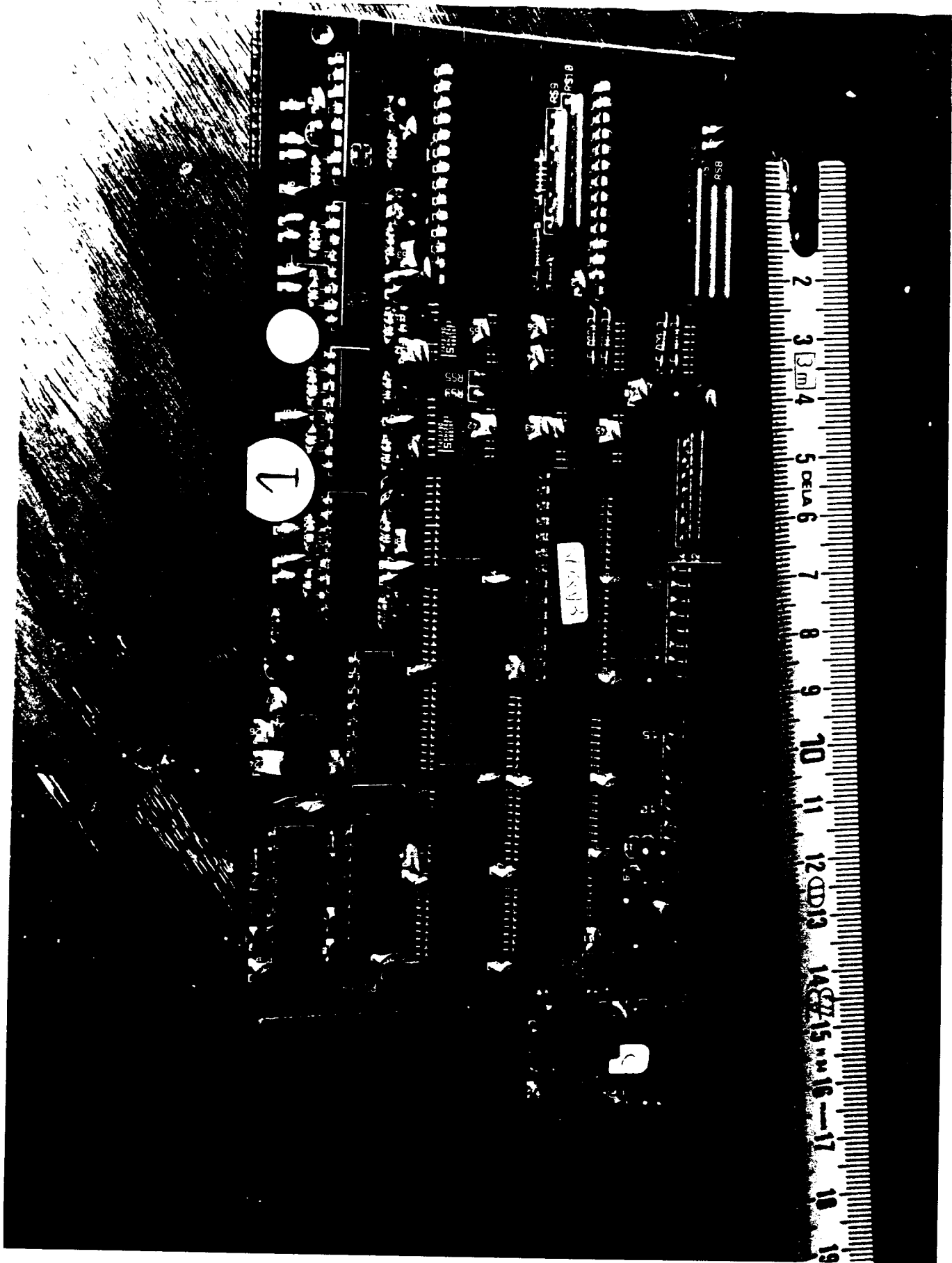


Fig. 4

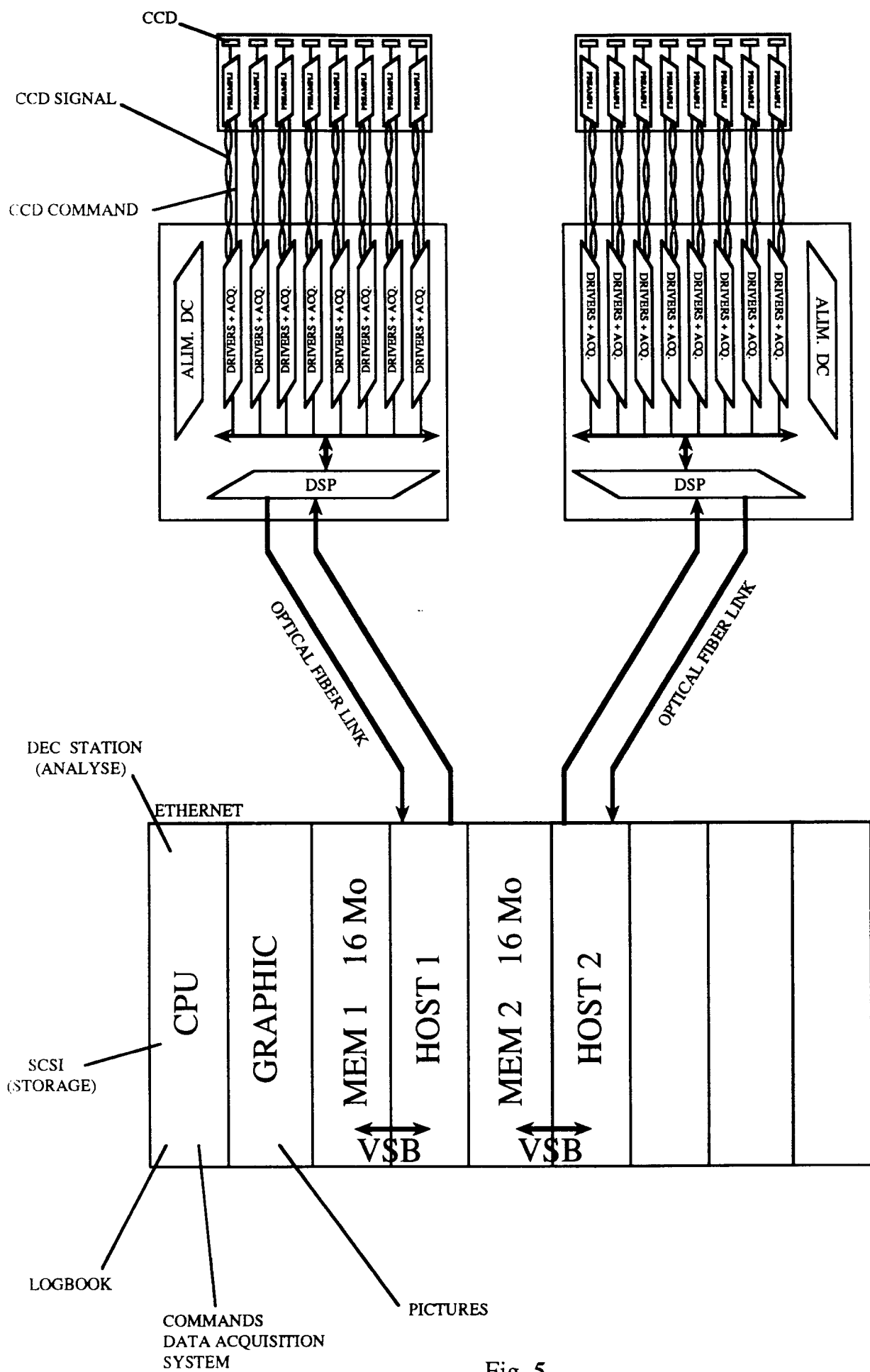


Fig. 5

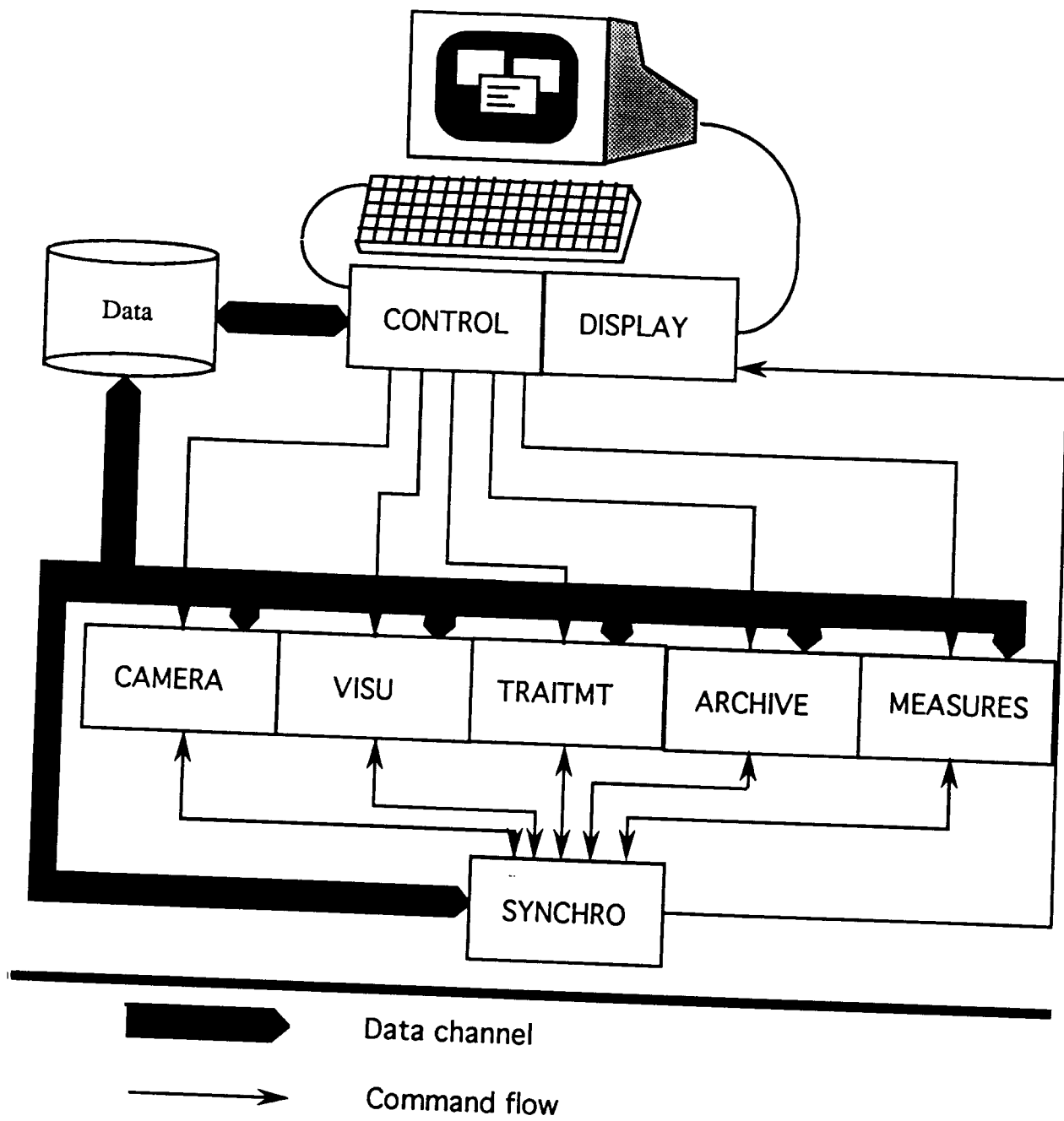


Fig. 6

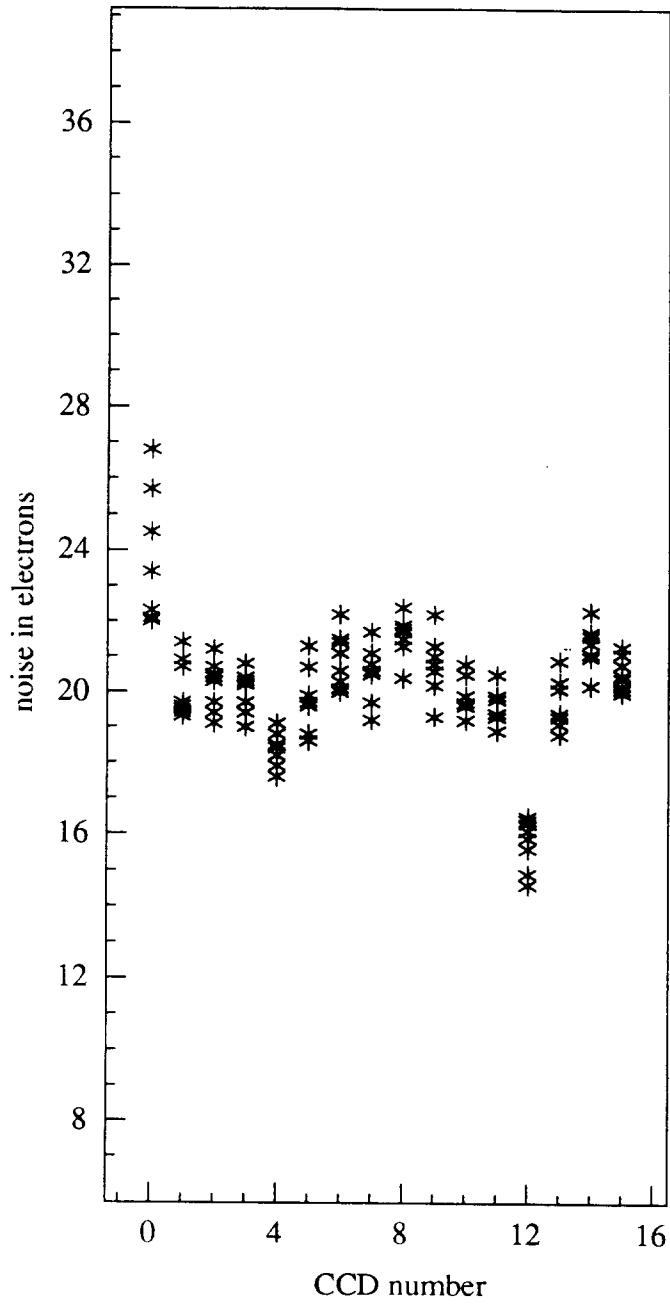


Fig. 7a

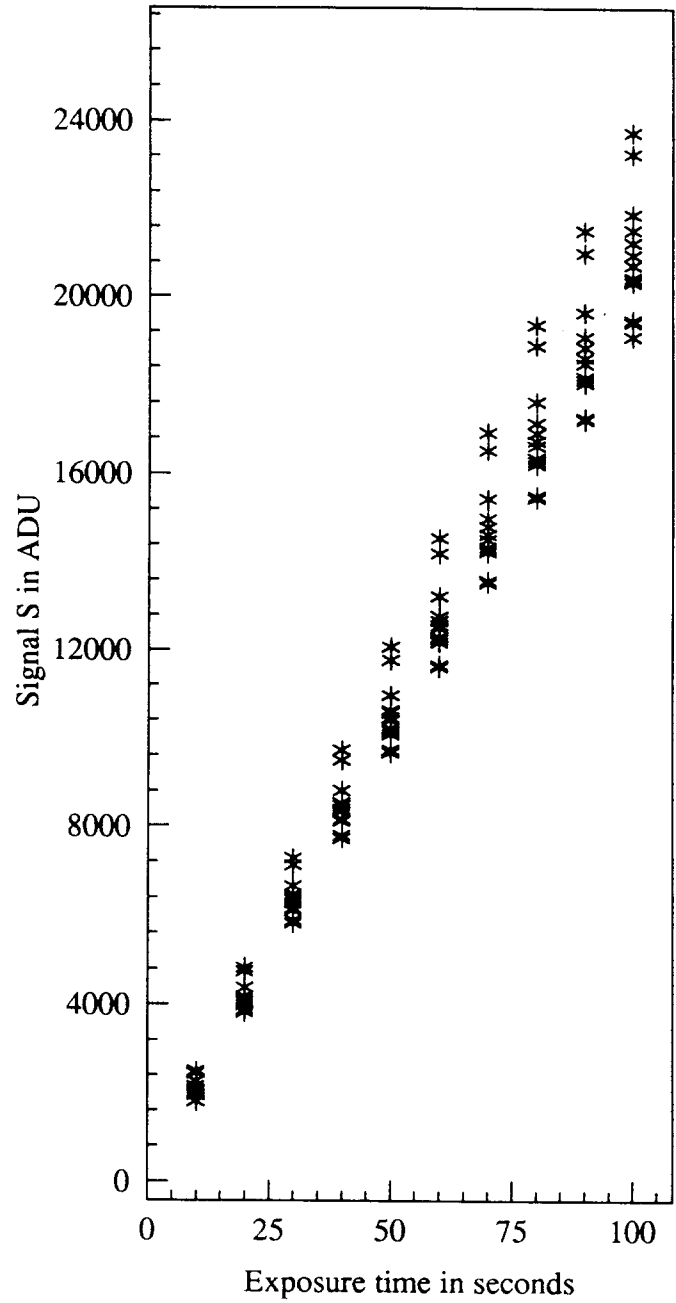


Fig. 7b

Fig. 7

Quantum efficiency CCD THX 31157 N°20

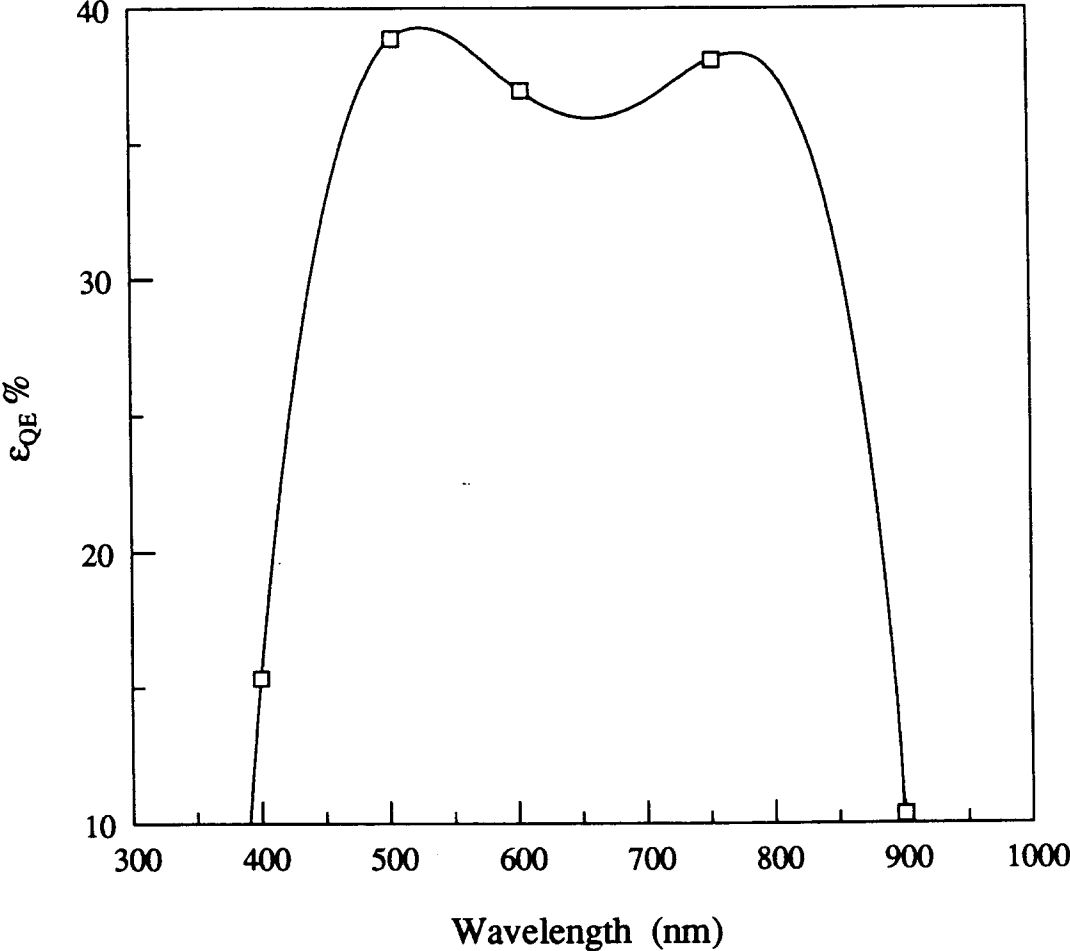


Fig. 8

