SITP NOTE TR-101
December 21, 1993

The ADC Chip (CRIAD) Test Result for RD2 Detector Application

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1. Introduction

The CRIAD (Charge Redistribution Interleaved Analog to Digital converter) test chip has been designed and fabricated for the RD2 detector development towards LHC. This piece-wise linear Analog to Digital Converter (ADC) has a conversion architecture which consists of 2 bits of flash followed by 6 bits of linear ADC, covering 11 bits of dynamic range. The advantage of this structure is the low power consumption at moderate speed, although the trade off between the speed, accuracy, and power consumption has to be studied in detail, according to the application involved. This report shows the evaluation results and analysis of the first prototype of this ADC chip, tested at CERN within the RD2 collaboration. We discuss the architecture of the chip, followed by a brief explanation of the ADC measurement technique. The various measurement results are presented, concentrating on an evaluation of the offsets, noise, Track and Hold, and Auto Zero function on the ADC performances.

2. The CRIAD chip and test set up

2.1 The CRIAD architecture

The CRIAD chip consists of two parts: a flash part with 2 bits for the segment specification, and seven 6-bit Successive Approximation ADC (SADC) placed in sequence. The block diagram is shown in Figure 1.

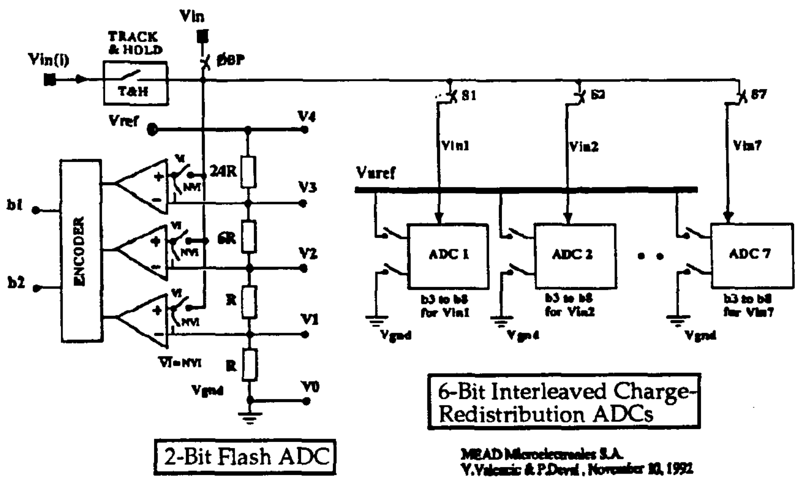

Figure 1: Block diagram of the non-linear ADC.

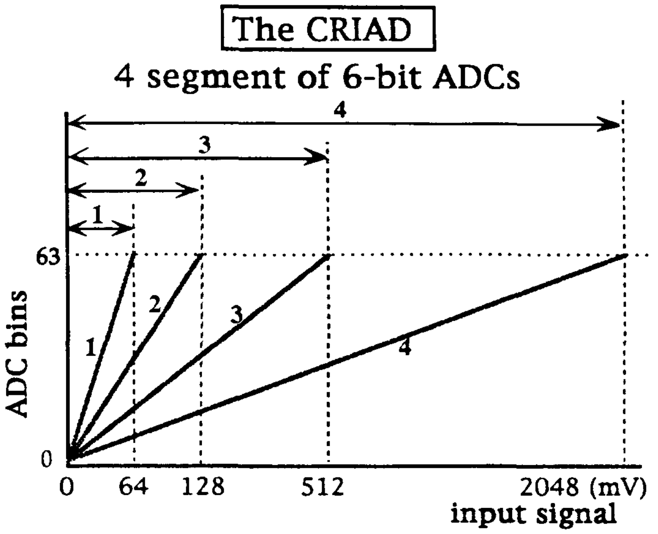

Figure 2 : The CRIAD segment structure.

The input signal is first investigated by the flash part to determine the range of the input signal. SADCs then digitizes the input signal with the reference voltage previously specified by the flash section. Figure 2 shows the 4 range choices of the CRIAD, in its present design.

Each segment has 64 steps. The minimum step (LSB in segment 1) is 1.0 mV. The dynamic range of the last segment (4) is 2048 mV, which is equivalent to 11 bits for the ADC dynamic range.

The CRIAD output data consists of

2 bits of segment specification,

6 bits of SADC data,

3 bits of the SADC address.

Another important characteristic of the CRIAD is that the independent SADCs are placed in sequence, and operated consecutively. Each SADCs make one comparison per one clock cycle, requiring 6 clock cycles for full 6-bit digitization, and 1 additional clock is needed for the input sampling. The total digitization time for one SADC is thus 7 clock cycles. Having 7 SADC running in sequence provides a full 6-bit digitized output at each clock cycle.

2.2 The CRIAD chip test board

To measure the CRIAD chip, the ADC test board was built[1] , with an interface to the VME bus. The ports provided by the board are:

- Input port for the sample signal with coaxial connection.
- Input port for the clock signal with coaxial connection.
- Input port for the power supply for the ADC chip and board itself.
- Two 32-pin flat cable port for VME interface.

The board also provides several controls. They are:

- Timing for the advanced clock, at the precision of 5 ns.
- The adjustment of the input power supply voltage for ADC.
- The adjustment for the reference voltage.

The Board has an 8 kbyte FIFO memory where the data read out from the ADC is temporary stored, prior to access by the DAQ system via VME bus. The FIFO is able to store maximum of

[1] Built at University of Geneve, by A. Leger and JP Richeux.

8000 events, where each event consists of 8 bits of ADC value, the address of the ADC, and the flag for the Auto Zero NVI signal. The Auto Zero function for the ADC is controlled through the VME interface and the board, enabling any modification of the length and period of the Auto Zero signal.

2.3 The test set up

Figure 3 shows the schematics of the test bench set up. The test bench was built using a VME driven by a Macintosh running a DAQ and analysis programs written with LabVIEW[4] software, with . First, a block of data is read out to the pipeline on the board from the ADC chip. Then, the VME interface controlled by the Macintosh reads a block of digitized data at a time from the on-board pipeline and transfers it to the Macintosh for further on-line analysis. The sample input signal and the sampling clock signal were generated externally.

With this set up, the speed of the DAQ was limited not by the digitizing process of the ADC itself, but the speed of the soft ware. A typical readout speed was approximately 10^3 events in a readout block of several seconds.

The chip requires an external voltage source for the power supplies and reference voltages. The power input for the ADC is supplied from an external power source, nominally at + 6 and - 6 volts. The ADC chip power supplies are normally + 3 and - 3 volts, which can also be adjusted externally, hence permitting the study of the chip power consumption and performance with different input and reference voltages. The reference voltage to the ADC is generated on the board, with a manual adjustment.

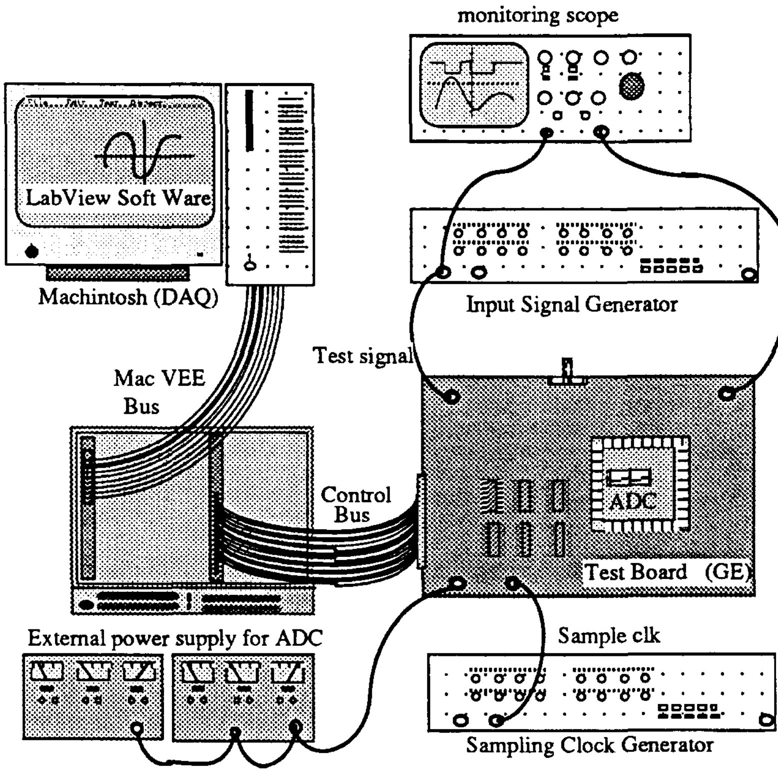

Figure 3: ADC evaluation system set up.

3. ADC Evaluation Methods

Several methods exist for evaluating the performance of an Analog to Digital Converter. We used differential and integrated non-linearity measurements, together with the estimation of the number of effective bits, in this analysis .

3.1 Non-Linearity

A Least Significant Bit (LSB) is defined as the range of the ADC divided by the number of ADC bins. The width of all bins are ideally equal, and also equal to one LSB. However, the real ADC dynamics will not be perfect, generating non-linearities in the response.

The Differential Non-Linearity (DNL) is defined as the difference between the measured bin width of an ADC and the theoretical width, or one LSB. The DNL is measured for all bins. The maximum value of the DNL is used to evaluate the performance of the ADC.

The Integral Non-Linearity (INL) for a given bin n is calculated by summing the DNL from the first bin to the n^{th} bin, or mathematically,

$$INL(n) = \sum_{i=0}^{n} DNL(i) .$$

As with DNL, INL is calculated for all bins of the ADC and the maximum value is normally taken for the evaluation of the ADC performance. Figure 4 shows the ideal transfer curve (left) and a typical transfer curve of a real ADC.

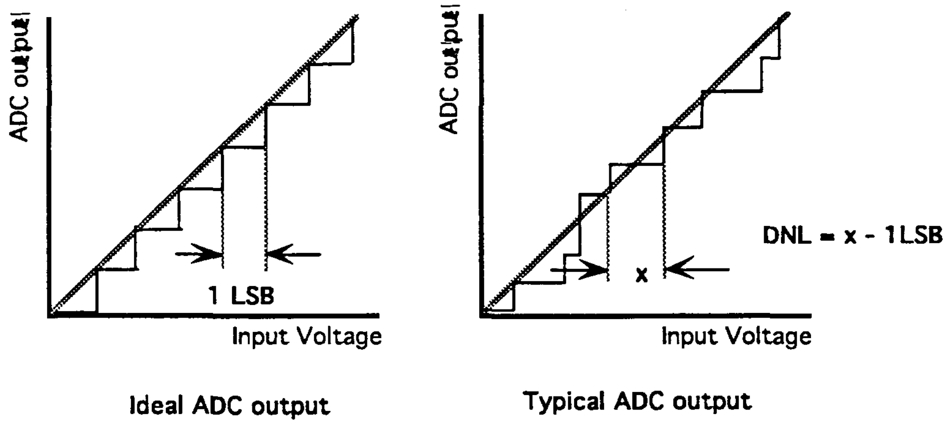

Figure 4: The ideal and real ADC output.

3.2 Number of the effective bits

The Signal to Noise Ratio (SNR) for the ADC is obtained by calculating the quantization error of the ADC and the actual noise produced by digitization process. The quantization error is the statistical error of the ADC which is added by the ADC to the reconstructed signal. The ideal RMS of the quantization error is given by

$$RMS = \frac{LSB}{\sqrt{12}},$$

where the denominator constant is from the gaussian distribution of the rectangular gate of the ADC bins.

The noise, the rms of the error, of the ADC is calculated by following method. The ADC is operated with a sinusoidal input, and the output value of the ADC is fitted with an ideal curve. For each sampling (event) the error on the digitizing process by the ADC is calculated. From this measurement the noise of the ADC can be calculated.

A real ADC will always produce more noise than the theoretical quantization noise, and therefore by taking the theoretical and measured noise value, the SNR can be calculated.

The Number of the effective bits (NoEB) is given by

$$NoEB = N - \log_2\left(\frac{\text{Actual RMS error}}{\text{Ideal Quantization error}}\right) ,$$

where N is the number of bits used by ADC[2].

[2] See reference [2] for more details

4. Response and Speed of the ADC

The ADC was tested for its response as a function of the clock speed. Figure 5 below shows the output of the ADC data for segment 1[3]. The sampling frequency was increased from 2 MHz up to 12 MHz, with the input signal kept at constant frequency and amplitude.

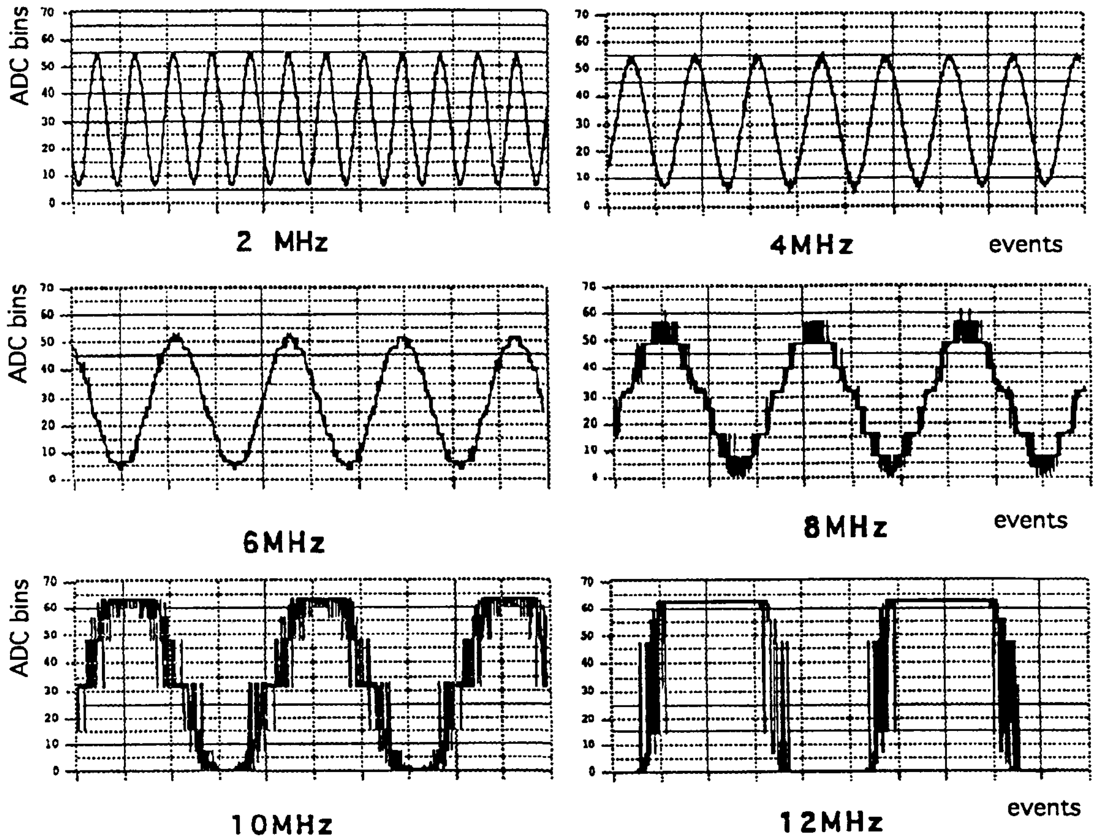

Figure 5: ADC response to the sampling clock frequency.

The response of the CRIAD for this segment shows that the digitized signal was acceptable up to a speed of 6MHz. Beyond this point, a non-monotonic transition at the output of the ADC was observed. This is clearly due to exceeding the maximum speed of the comparators.

Table 2 shows the operational speed of the ADC, determined by measurements of the digitized output from the ADC. This is obtained by finding the starting point of the non-monotonic response of the output.

Segment number	1	2	3	4
Max. Frequency (MHz)	6.0	6.5	7.5	12.0

Table 2: Maximum speed by observing the multiple translations.

This result shows that the performance limit of first three segments is quite different from that of the last segment.

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[3] The highest sensitivity (segment 1) is presented here, because of maximum resolution..

5. Power Consumption

One of the most important criteria of the ADC for RD2 detector applications is the low power consumption required to avoid the heat dissipation, in order to minimize the required cooling. The two bit flash part of the CRIAD consists of a resistor string and 3 comparators. The resistor string uses a provided DC current which is indicated as Vref in Figure 6. The SADC part of the chip has the charge-redistributed architecture, each SADC containing only one comparator and one 6-bit binary-weighted capacitor array .

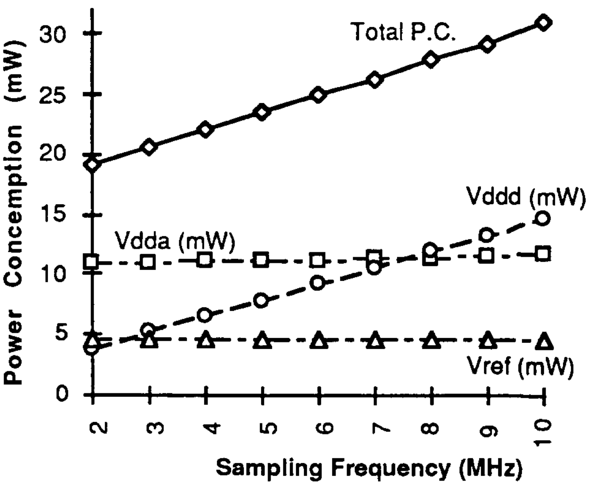


Figure 6: Total power consumption of the ADC. The measurement was taken with the bias current at 25 mA, and V_{DD} at 5 volts..

A measurement of the power consumption of the CRIAD under various conditions was made, and the result of the sampling frequency dependency is presented in Figure 6. The analog power consumption shows a linear dependence in the operational speed of the ADC, as expected.

A similar result was observed with a different input voltage supply (Vdd) and bias currents to the chip. Table 1 shows the analog and total power consumption of the chip, for the sets of input voltage supply, the bias voltage, and ADC speed, compared with the expected value[1].

ADC speed	Bias current	Analog power consumption [mW] V_{DD}=5V	V_{DD}=6V	Total power consumption [mW] V_{DD}=5V	V_{DD}=6V
5MHz	25μA	11.2 (14.0)*	17.1 (15.5)	23.5	32.0
	50μA	16.6	22.3	31.4	39.7
10MHz	25μA	11.9	17.3	31.2	40.1
	50μA	17.2 (26.5)	23.2 (31.0)	40.9	51.3

*( ) value is the expected value.

Table 1: Power consumption of ADC.

We observed the obtained value were less than the expected value, from design. This result satisfies the ADC's low power consumption required by the LHC detector application at this stage of the development.

6. Offset Measurement and Adjustment

The 7 SADCs of the CRIAD are independent in the chip and they must have the same common zero point reference when the digitization takes place. An Auto Zero function has been installed within the chip to compensate the offset of all comparators periodically. A Non-Valid Input (NVI) signal is sent to the ADC for this period. The digitization of the input signal is interrupted by Auto Zero function. The Auto Zero functionality will be discussed in detail with measurement results in later sections. In this section, the offset compensation studies of the ADC units and related measurements are presented.

6.1 Offset of the 7 SADC

First, we observed the offset values of the 7 different SADCs on one chip. In Figure 7, the output of the ADC for a constant input is shown. The x-axis is the event number obtained in sequence, where the sampling frequency is at 3 MHz. The ADC was set at Segment 1, T/H on, and an Auto Zero signal was sent at every 25 sampling periods.

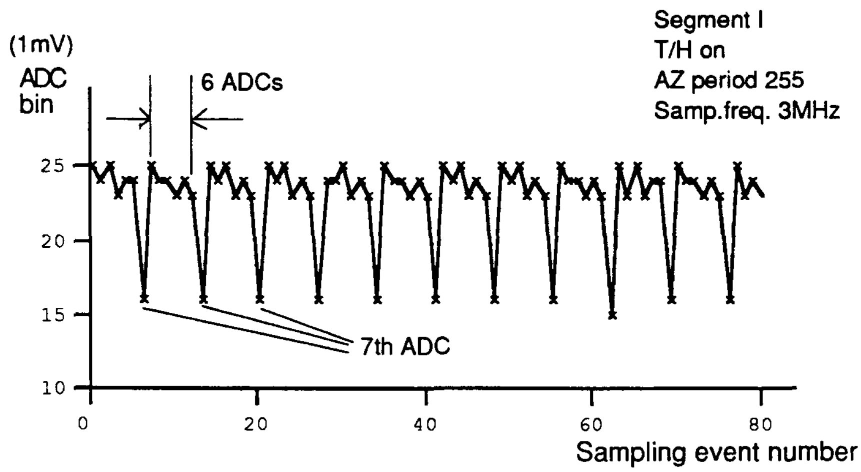


Figure 7: Difference of the offset value of 7 ADCs.

From the figure above, we have determined that the ADC 7 (or the last SADC in the sequence) has the pedestal value approximately 8 bins less than others, or 8 mV in this case. The other 6 SADCs also have a small offset difference, which is consistent through out the different samplings. However, this peak-to-peak variation of the first 6 SADCs is a few LSB, which corresponds to a few mill-volts[4]. Figure 7 shows the result for the most sensitive segments. The offset values of other segments were independent of the LSB of each segment. That is, the offset difference between the last SADC to the preceding 6 SADCs was measured to be around 8 milli-volts regardless of the LSB value or the segments specified by the comparator.

To solve this problem for the existing design, pedestals must be subtracted from the acquired SADC value for each SADCs. The pedestal has been calculated and the offset values of the ADCs are measured. We measured the dependence of the offset on various settings and we find that it depends on two elements: One is the decoupling of the power supply to the ADC chip and other is the timing of the master clock and the advance clock.

[4] This result was obtained from the segment 1 (LSB is 1 mV).

6.2 Decoupling Capacitor

One of the factors affecting the offset of the SADCs was determined to be the high frequency noise that enters from the power supply into the ADC. From observations on the oscilloscope, we observed some spikes and kinks on the clock and other various signals which we define as High Frequency Noise (HFN). To filter HFN, we connected two decoupling capacitors to the power supply of the ADC chip, shown in the figure 8 presented below. The capacitance values were adjusted, and a 0.1 µF capacitance was determined to be the best.

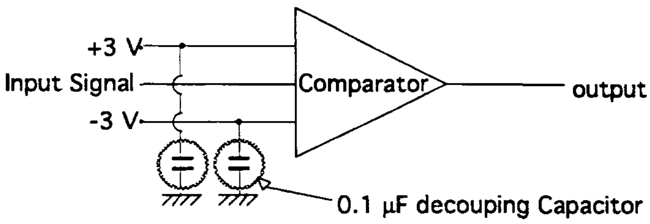


Figure 8: Decoupling capacitors to the power supply.

As a result of the decoupling capacitors, the offset on SADC #7 moved to the same level of the other SADCs. Only the offset of the SADC #7, which is the last SADC of the sequence, is affected by the decoupling capacitors. This last SADC located is just before the logic sequencer of the chip. A further detailed analysis is needed to understand the HFN effect on the ADC offsets. The results of this analysis will be considered in the next ADC design phase.

6.3 Timing adjustment

The SADCs require two input clock signals for the digitization function. The master clock is used to run the sequencer of the SADCs. The decision of the internal comparator in each SADC is made at the falling edge of this clock, and the comparison voltage is applied at the rising edge. Another clock, the advanced clock, is used to sample the input value in each SADC. This sampling has to be done just prior to the application of the cooperator voltage for the SADC of first bit of conversion.

By adjusting the relative timing (Δt) of the two clocks, we observe that it changes the pedestal value of the SADC #7, while leaving the rest of the 6 SADCs pedestal values constant. When Δt was set to 5 nano-seconds[5] the offset of the ADC 7 increased by 10 bins, and at 10 ns it was decreased by several bins. A linearity dependency was not observed between the pedestal of the ADC 7 and the Δt of the clocks. The ADC did not operate when Δt was increased over 15 ns.

The Δt adjustment does change the offset value of the 7th SADC, though finer adjustment is required to achieve a better agreement with pedestal of the rest of the SADCs. This problem must also be investigated further to understand the non-linear dependency of the pedestal on the SADC #7, as a function of the timing delay of two clocks.

To enable further testing of the full ADC, we have optimized the system to obtain the same offset values for all 7 ADCs, by the decoupling capacitor and clock timing adjustment.

[5] The relative timing can be adjusted on-board, with a resolution of 5 ns.

6.4 Bias Resistance

An important criteria of this ADC design is to characterize the trade off between the resolution and the speed. The ADC was designed to operate at 5 MHz to 10 MHz, though we found that the performance of the ADC degrades at 5 MHz when the LSB was set at the finest setting, at 1 mV. To achieve a better operational performance, the bias resistance on the input power supply to the chip was decreased to 32 kΩ from 16 kΩ on the board, changing the bias current to the chip from 25 μA to 50 μA, hence putting more power into the ADC. The effect of the bias current to the power consumption has been presented in the earlier section. The effect of the bias current in the resolution has been measured both with linearity and noise measurements.

Noise measurement

We measured noise values with different bias resistance to observe the dependence between the input power supply and the sampling frequency. Figure 9 shows the measured rms noise for two values of the bias resistance. Here, the measurement was done on the ADC segment 1 with the T/H operational.

By examining the noise level, it is clear that the it extends the operational range of the ADC, approximately by 1 MHz.

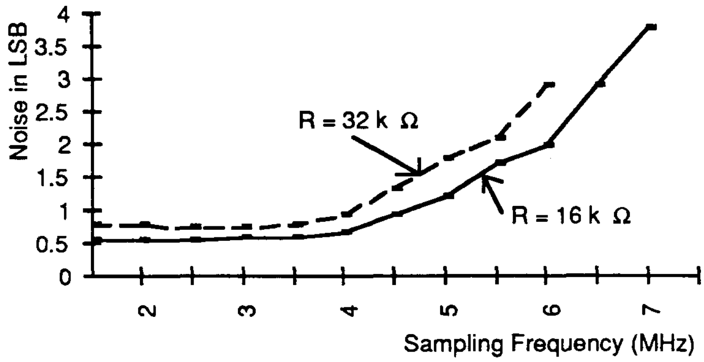


Figure 9: Noise comparison on the bias resistance (seg. 1).

Non-Linearity measurement

Another method of testing the ADC performance is to measure the non-linearity, as explained in a previous section. Non-linearity measurements for two different bias resistance are presented in Figure 10, showing an clear improvement. The measurement was taken with the segment 1.

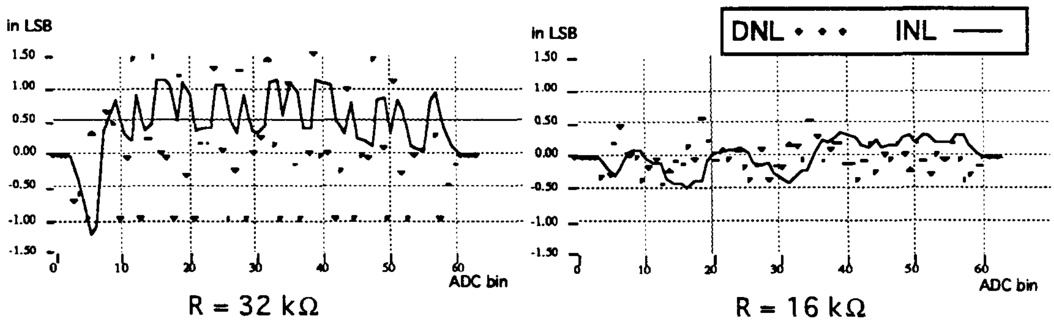


Figure 10: Bias resistance effect on non-linearity at 5MHz.

6.5 Resistor string -- layout problem

The ADC is designed to have a range from 0 to - 2048 mV, covered by 4 different segments. The reference voltage was taken from the external source, adjustable on the board, enabling a detailed measurement and study of the calibration of the ADC. Initial measurements showed that the upper limit of the ADC range is approximately at - 20 mV, while it is expected to be at zero, or ground. The measurement showed the ADC reading gives zero for any input voltage above - 20 mV.

The cause to this problem was found when the ADC chip was examined at the probe station. The reference voltage for the specified segment is generated within the chip with the resistor strings. It consists of 32 resistor pads, connected to the external upper reference voltage (ground) and lower reference voltage inputs. Figure 11 shows the flash part of the CRIAD chip with resistor strings which provides the reference voltage. With a close observation, we found that the connection between this resistor string and the input pad of the high reference voltage (ground) carries some resistance equivalent to 1% of the total resistance of the resistor string. The reference voltage is normally set to - 2048 mV, so that the 1% error on the resistance at the upper limit produced a - 20 mV error. This value agrees with the error value observed by the measurement from the digitized output of the ADC. This layout design error is understood, and it will be corrected for the next design phase.

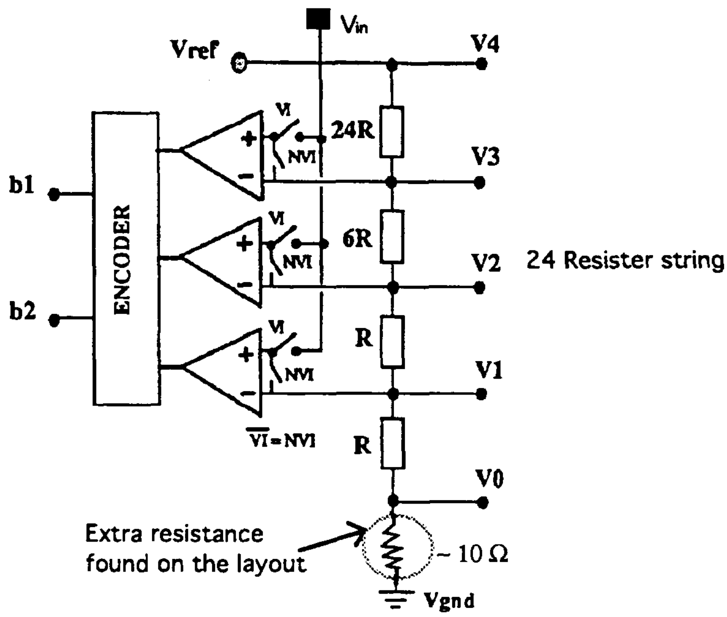


Figure 11: Layout problem of the reference voltage.

7. The Auto Zero function

The Auto Zero function was designed to cancel the offset and charge injection errors for all comparators. It should allow a decision level of the comparator exactly at the reference voltage level, with an error of less than one LSB. The Auto Zero function increases the accuracy to the ADC.

7.1 Offset drifts without Auto Zero

There are 2 modes to the Auto Zero operation. They are:

1). Auto Zero ON: The decision level of the comparator is dynamically adjusted, so that the difference with the reference voltage is less than 1 LSB. Any internal drift is compensated. The period and frequency of the Auto Zero can be adjusted.

2). Auto Zero OFF: The compensation of the offset is no longer in operation, so that the error in the decision level of the comparator can be larger (up to a few LSB) than in the case (1).

Figure 12 shows the difference of the ADC operation , with Auto Zero On (1) and Auto Zero Off (2).

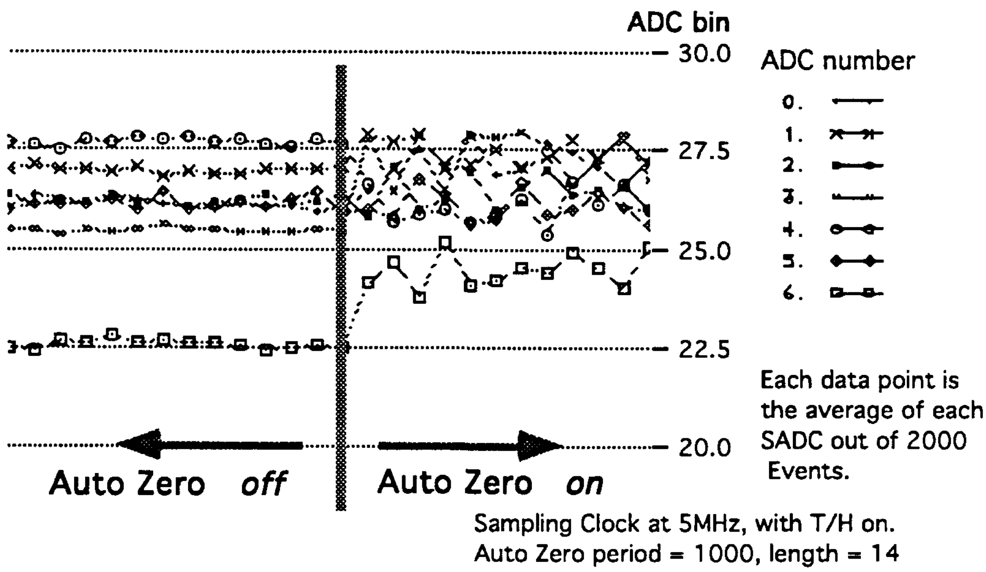


Figure 12: Auto Zero functionality. Mode 1) and 2).

The 7 SADCs had small differences in their offsets, which were suppressed with the Auto Zero function. However, the Auto Zero operation introduces a larger noise to the system, which can be observed from the Figure 12. The pedestal fluctuation of individual SADC elements is much larger in the operational mode 1 (Auto Zero on) then in the mode 2.

Figure 13 shows the ADC output with Auto Zero being fixed for 8000 events. The input signal was constant, and the sampling frequency was at 1.0 MHz. It shows a good stability of the ADC for 8 milliseconds.

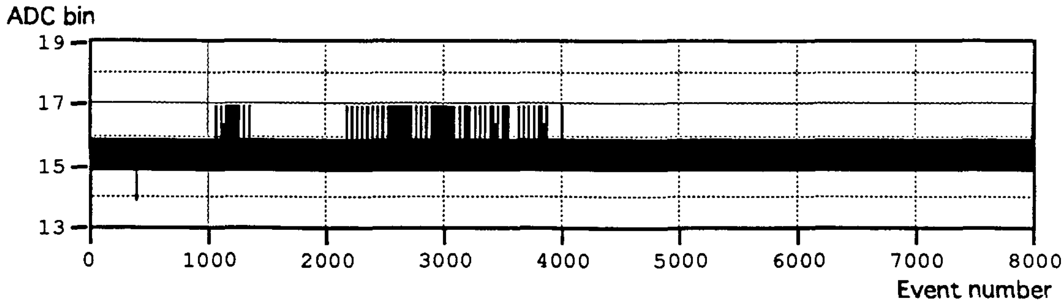


Figure 13: ADC stability with fixed Auto Zero.

7.2 Non-linearity measurement

Differential and Integral Non-Linearity was measured with different frequency of the Auto Zero settings. The noise values for different Auto Zero frequency showed definitive dependencies, as mentioned, yet it was not a case with Non-Linearity measurement. We have measured the INL/DNL for the function of Auto Zero frequency and its period, and the result shows little sign of the dependency on the Auto Zero function.

7.3 Noise and Auto Zero relation

We measured the relation between the pedestal of the 7 SADCs and noise around the pedestals, scanning through the Auto Zero frequency. Figure 14 below shows the result for the variation of the pedestal and noise level.

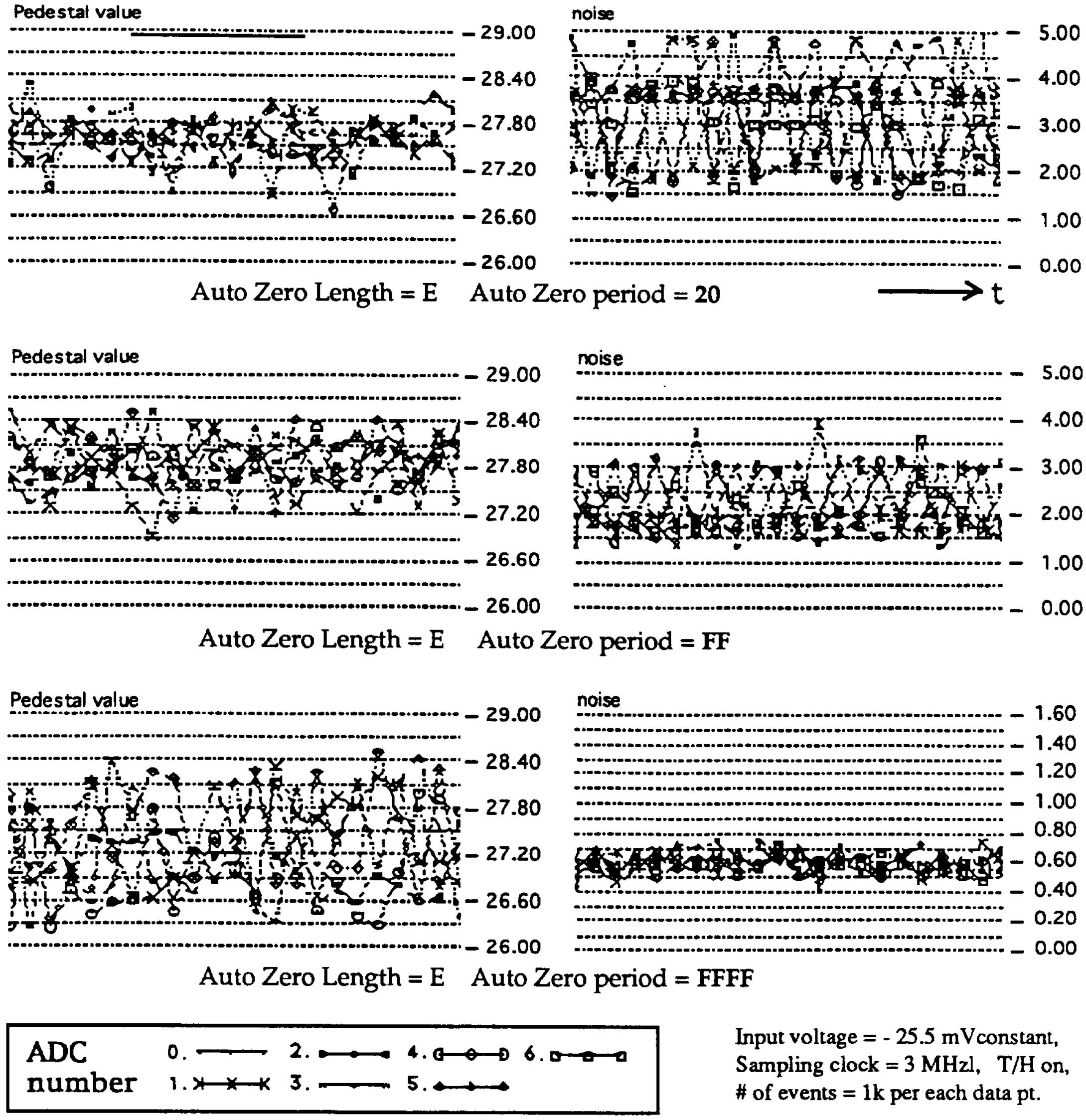
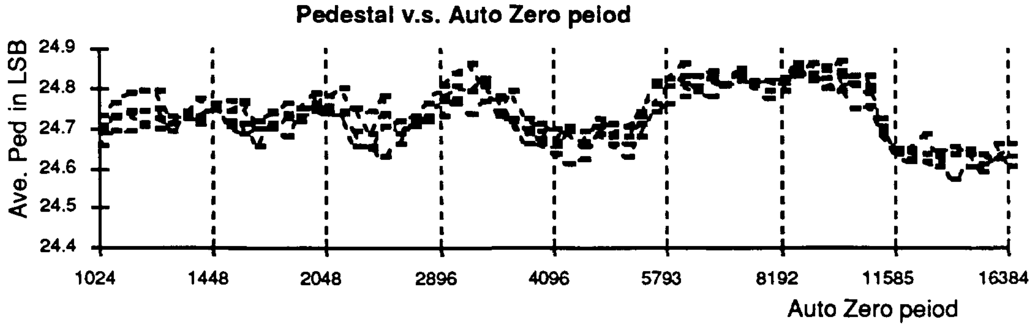


Figure 14: Pedestal and noise dependency on Auto Zero frequency.

The noise, or the r.m.s. out of 2000 events, presented above is calculated once par block, which can be translated as a *high* frequency noise. On the other hand, the *low* frequency noise can be determined by observing the r.m.s. of the pedestal values. The variation of the pedestal value for different blocks of data is interpreted as a low frequency fluctuation of the SADCs.

From the result presented above, we can conclude that the high frequency noise increases when the Auto Zero is frequent, while the low frequency noise is suppressed. The decrease in the Auto Zero frequency results different effects on the high and low frequency noise. A period of FF with a length of E is the optimum setup.

Figure 15 shows the pedestal and noise result, scanning the Auto Zero period up to every 16k events. The measurement was repeated several times, and it shows the dependence of the frequency of the Auto Zero.



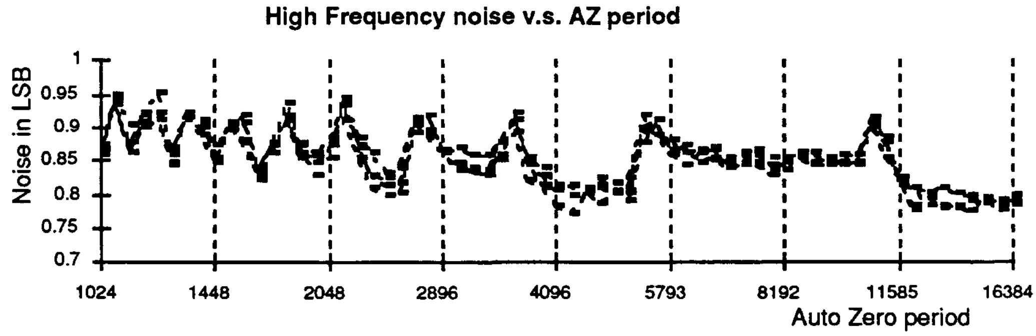


Figure 15: Pedestal and noise dependency at large Auto Zero frequency.

From above measurements, it was observed that Auto Zero functionality improves the uniformity of the offsets of SADCs. We have observed the relation between Auto Zero period and noise. The system must be optimized for the next design phase.

8. Track and Hold

8.1 Track and Hold functionality

The Track and Hold (T/H) function was designed to improve the ADC functionality for high frequency variations of the input signal, as compared to the sampling clock speed. The T/H timing is derived from the sampling clock. The first half clock cycle is held and the other half of the clock cycle tracks. The ADC reads the input signal while the input signal is being held, and thus the signal is stable while the comparator is in operation. Figure 16 shows the relation of track and hold with the sampling clock.

The question relating to the Track and Hold characteristics was the speed-to-accuracy trade off. We measured the non-linearity of the ADC with and without Track and Hold functionality at various sampling frequencies and for other input conditions.

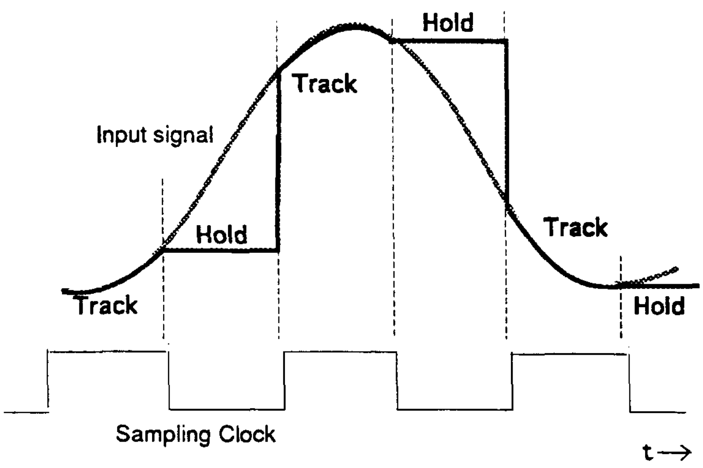


Figure 16: The Track and Hold.

8.2 Non-linearity measurement

We measured the non-linearity as a function of the operational speed of the ADC to evaluate the performance of the ADC with Track and Hold. Figure 17 shows the maximum value of the Differential Non-Linearity (DNL) and Integrated Non-Linearity (INL) for the ADC sampling speed from 2 MHz to 7 MHz.

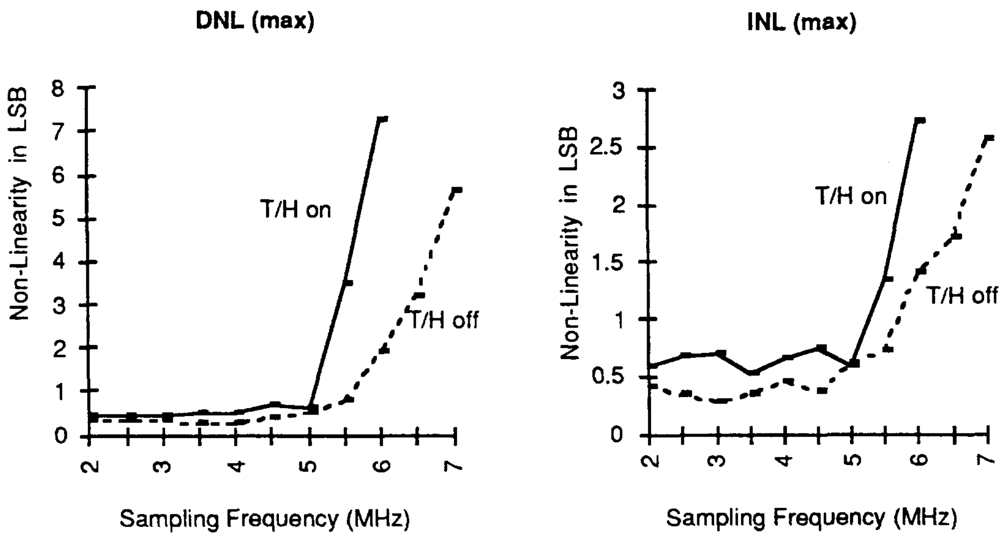


Figure 17: Non-linearity comparison with Track and Hold.

As we require high sensitivity, segment 1 was used to measure the non-linearity. It shows that the T/H functionality does not improve the non-linearity of the ADC, especially at the higher clock frequency. The limit of the operational speed was 6 MHz and 7 MHz for T/H on and off, respectively. This result was obtained with the lowest segment which is most sensitive to the speed of the sampling clock. We have repeated the same measurement for other segments of the ADC. For segment 1 and 2 (LSB 1.0 mV and 2.0 mV respectively), the T/H dependence was similar. The non-linearity with the T/H on is higher, and the limit of the sampling frequency is lower, as shown in the Figure 17.

For the largest segment with LSB, at 32 mV, the maximum non-linearity observed was less than 10 % of the LSB. Although the difference of the non-linearity for T/H on and off was much smaller, we observe a better performance when T/H is off. The maximum clock frequency is reaches 12 MHz for segment 4.

Figure 18 shows the Integrated Non-Linearity for the all bins of the ADC. Here, the data was taken from the most sensitive segment as before (the segment 1), with the sampling frequency at 5 MHz.

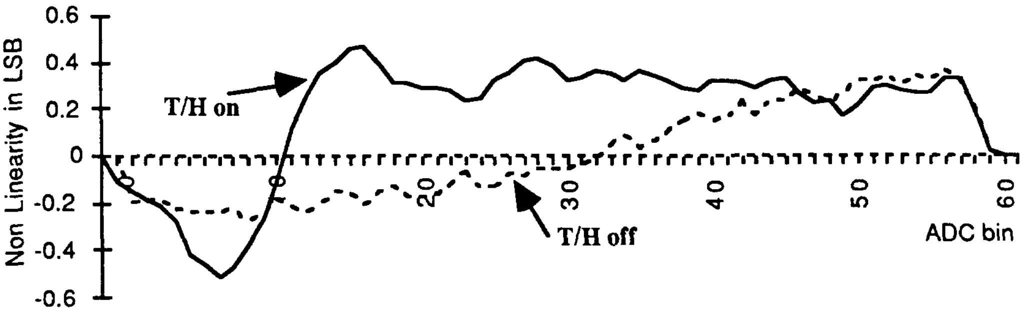


Figure 18: Integrated Non-Linearity for all Bins.

The T/H effects on the lower bins of the ADC, INL being maximum at the bin number 8. This was observed only for segment 1. Other segments showed better non-linearity results without T/H, but the difference was much smaller.

8.3 Number of effective bits measurement

The Number of effective bits (NoEB) was measured for a range of sampling frequencies, with the T/H on and T/H off, and the result is presented in the Figure 19. The measurement was made for all 4 segments of the ADC. Figure 19 shows the result for segment 4. This result also shows that adding the T/H functionality will deteriorate the performance of the ADC. When the sampling frequency was increased beyond 10 MHz, the ADC did not respond with T/H on. However, the result shows the good performance of the ADC at expected operational speed.

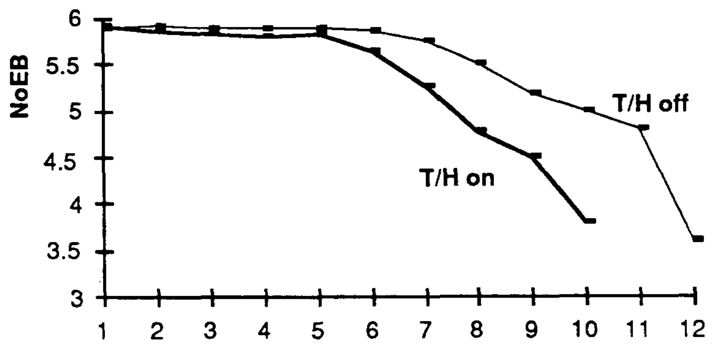


Figure 19: Number of Effective Bits on Segment 4.

8.4 Track and Hold signal

The Figure 20 shows the actual signal of the T/H observed directly from the chip itself using a probe station, at two different operational speeds. Because of the probe itself has some impedance capacitance, the output of the probe signal is quite distorted at higher frequencies. Here signals from operational speed of 500 kHz and 2.0 MHz are presented.

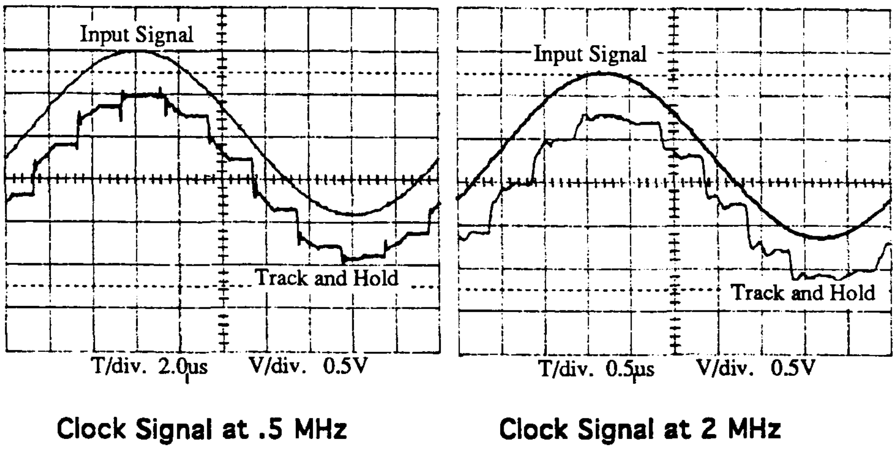
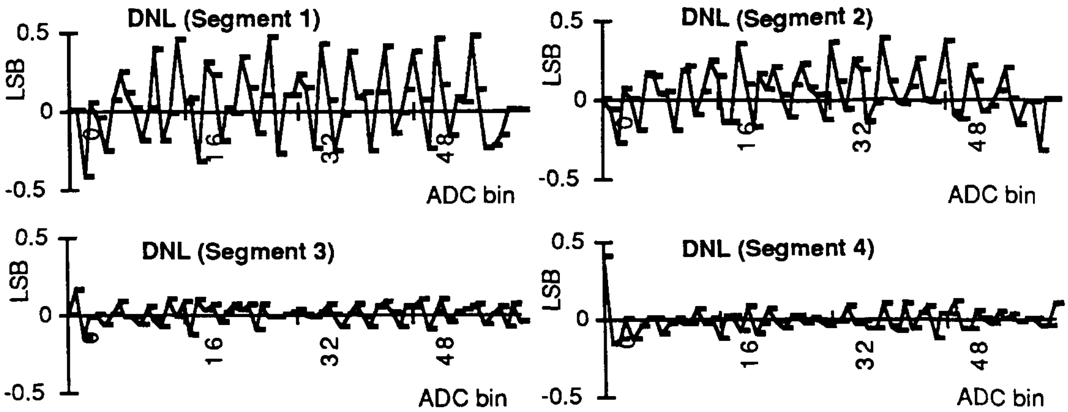


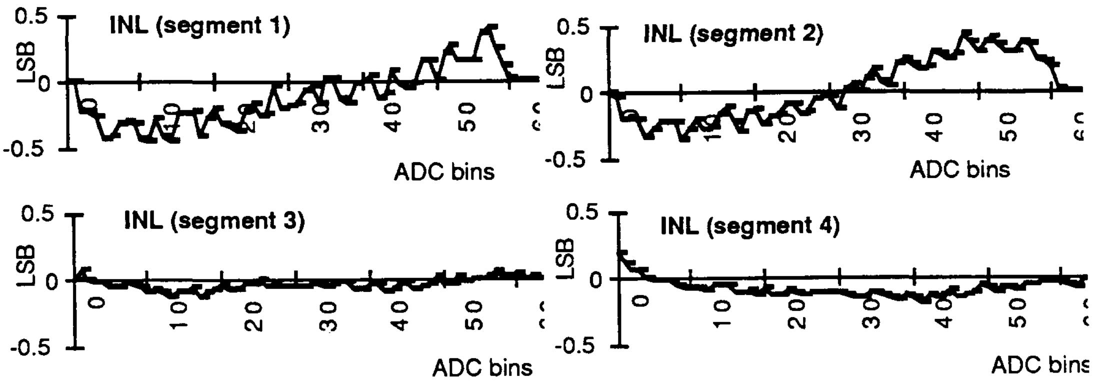
Figure 20: Track and Hold signal observed through a probe station.

Further measurement with T/H has been done, and we have found out that T/H function depends largely on its relative timing of the master clock and the advanced clock (as described in Section 6.2). Further note of the characteristics of this ADC with T/H is underway.

9. Non-Linearity Measurement Results

Following figures show the non-linearity measurements having understood the detailed functionality characteristics of the CRIAD ADC chip, explained in the preceding sections. Sampling frequency was at 5 MHz, T/H on, and the Auto Zero frequency at 255.





10. Conclusion

The CRIAD chip for the RD2 detector application has been fabricated and tested for its functionality. Expected functionality was achieved with good performance measurements at speed up to 5MHz. The operational speed was tested up to 10 MHz, but the ADC did not function with full quantitative design performance at this sampling frequency. An excellent result was obtained from the non-linearity measurement, which shows that with an ideal operational condition, the ADC response has error much less than 1 LSB both in INL and DNL, in all 4 segments of the dynamic range.

The ADC power consumption has been measured, and the result shows the measured value is lower then the expected value in high speed operation. The total power consumption is within 25 mW at 5 MHz.

References

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