Prototype board development for the validation of the VMM ASICs for the New Small Wheel ATLAS upgrade project

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***Abstract*—The VMM is a custom Application Specific Integrated Circuit (ASIC) which was designed to be used in the front-end readout electronics of both micromegas (MM) and small Thin Gap Chambers (sTGC) detectors of the New Small Wheel (NSW) Phase-I upgrade project of the ATLAS experiment. A new version of the VMM was recently fabricated and for that reason various prototype boards, the micromegas Front-End (MMFE1) and the General Purpose VMM (GPVMM), have been fabricated and extensively tested in order to validate the functionality of the ASIC. These boards use commercial Field Programmable Gate Arrays (FPGAs) for direct communication with computers which is achieved through 10/100/1000 Mbps Ethernet and UDP/IP protocols. The low noise performance of these boards gave the opportunity to be used in various test beams with micromegas detectors for validating the VMM and for performance studies of the sTGC detectors. A detailed description of the boards along with the results of the test beam and the detector studies will be described.**

I. Introduction

The ATLAS NSW upgrade [1] is motivated primarily by the high background radiation that is expected during Run-3 (2021 - 2023) and ultimately luminosity of $7 \times 10^{34}\,\mathrm{cm^{-2}s^{-1}}$ in HL-LHC (after 2026). In the ATLAS experiment [2] the present muon Small Wheels will be replaced by the NSW. The NSW is a set of precision tracking and trigger detectors able to work at high rates with excellent real-time spatial and time resolution. The new detectors consist of the resistive Micromegas (MM) and the small-strip Thin Gap Chambers (sTGC) [1].

The challenging detector requirements must be coupled with appropriate readout electronics, which must provide pulse amplitude, timing measurements, and trigger information for more than two million channels ($\sim 2.1\,\mathrm{milions}$ for the micromegas and $\sim 0.3\,\mathrm{milions}$ for the sTGC). In addition, for reliable operation, radiation tolerance and correction mechanisms for Single Event Upsets (SEU - this is a change of state caused by a high-energy particle strike to a micro-electronic device) must be implemented.

Various prototypes of electronic boards should be designed and fabricated to house the new VMM3 ASICs. The ASICs should undergo over a series of tests and measurements before being validate.

II. VMM3 ASIC description

VMM3 [3] is a mixed signal (analogue and digital) radiation tolerant ASIC numbering about 5.2 milion transistors in an area of $8384\,\mu\mathrm{m} \times 15\,308\,\mu\mathrm{m}$. The ASIC is designed at Brookhaven National Laboratory and fabricated in the 130 nm Global Foundries 8RF-DM process. It is composed of 64 front-end channels each providing a low-noise charge amplifier (CA) with adaptive feedback, a shaper with baseline stabilizer, a discriminator with trimmer, a peak detector, a time detector, some logic and a dedicated digital output for Time-over-Threshold (ToT) or Time-to-Peak (TtP) measurements. Shared among channels are the bias circuits, a temperature sensor, a test pulse generator, two 10-bit DACs for adjusting the threshold and test pulse amplitudes, a mixed-signal multiplexer, the control logic and the Address in Real Time (ART) which consists of dedicated digital outputs (flag and address) for the first above-threshold event. The peak detector measures the peak amplitude and stores it in an analogue memory. The time detector measures the peak timing using a time-to-amplitude converter (TAC). The TAC value is stored in an analogue memory and the ramp duration is adjustable. The peak and time detectors are followed by a set of three low-power ADCs (a 6-bit, a 10-bit, and a 8-bit). The block diagram of a channel and the common blocks of the VMM3 is shown in Fig. 1.

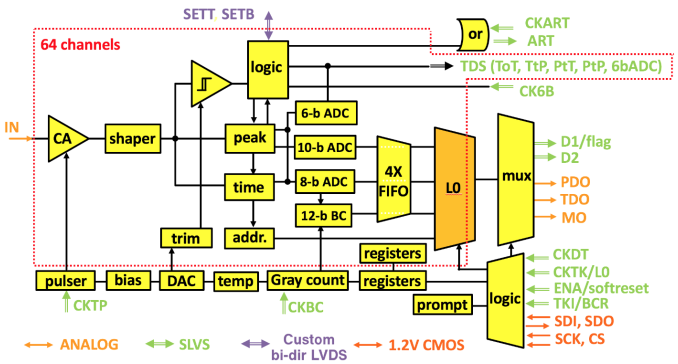

Fig. 1: Architecture of VMM3

A. *MMFE1 board description and functionality*

To validate the functionality of VMM3 ASIC the MMFE1 board, shown in Fig. 2, was fabricated. The board was designed to be compatible with the $10 \times 10\,\mathrm{cm}^2$ micromegas prototype chambers. For that reason the 130 pin Panasonic female connector (Part Number: AXK5SA3277YG) was used. Five LEMO connectors provide access to: Monitoring Output (MO), Peak Detector Output (PDO), Time Detector Output (TDO), a LVTTL output signal for the ART, a Transistor Transistor Logic (TTL) input signal for the trigger.

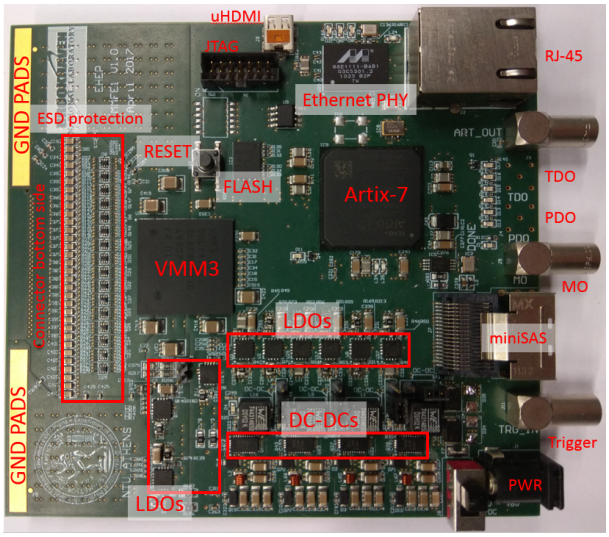

Fig. 2: The MMFE1 board.

For the power distribution a set of DC-DC converters and LDOs was used. The LT8612 Step-Down regulator has a wide input voltage range from $3.4\,\mathrm{V}$ up to $42\,\mathrm{V}$ and an output ripple of less than $10\,\mathrm{mV p-p}$. A diode network can be used as an alternative way to power on the MMFE1 and is possible to eliminate any noise introduced by the switching frequency of the DC-DC converters. In this case the input voltage must be $3.5\,\mathrm{V}$ and the selection is made by a two-point switch.

Xilinx's XC7A100T-2FGG484C FPGA proved to be the ideal solution balancing cost and functionality as it is relatively inexpensive and has enough resources, fulfilling the requirements of the board. The new version of the VMM (VMM3) uses the Scalable Low Voltage Signaling for 400 mV (SLVS-400) specified in JEDEC JESD8-13 [5]. Artix-7 FPGA does not support SLVS and for that reason the DIFF_HSUL_12 Xilin's differential standard was used. This standard provides the lower common mode voltage comparing to all other standards and proved to be fully compatible with the SLVS. For that reason the corresponding banks of the FPGA were powered on with the required $1.2\,\mathrm{V}$. The FPGA is accessible through a standard Join Test Action Group (JTAG) connector for programming and monitoring. To store the configuration file for the FPGA, a non-volatile Micron $256\,\mathrm{Mb}$ Serial NOR FLASH was used. The Quand Serial Peripheral Interface Bus (SPI) is used to access the read/write commands of the FLASH memory. A second $32\,\mathrm{kb}$ Electrically Erasable Programmable Read-Only Memory (EEPROM) was used for storing the media access control address (MAC) and Internet Protocol (IP) addresses of the board. This gives the capability of the dynamically reconfiguration of the board which is useful if multiple boards are used over the same network. The access to the specific EEPROM is implemented through the $\mathrm{I^2C}$ protocol. The power consumption of the board is about $6.5\,\mathrm{W}$ on full operation and the board dimensions are $117.73\,\mathrm{mm} \times 109.47\,\mathrm{mm}$.

The board was designed with eight layers and special layout rules were followed in order to minimize the noise on the input channels of the ASIC. Analogue and digital ground planes were split to avoid any digital noise interference with the sensitive analogue electronics. Special consideration was given also to avoid any overlapping of digital and analogue planes between the layers. The different ground planes were interconnected in a single point by using jumpers. For the VMM ASIC the via to pad technique was used and the Low Equivalent Series (ESR) bypassing capacitors were placed directly to the pads of the VMM. Moreover pi-filters were used at the outputs of the DC-DC converters and the LDOs in order to minimize any potential unwanted noise.

An Electro-Static Discharge (ESD) protection circuit was implemented at the input of each channel of the VMM. This circuitry includes the SP3004 diode array along with two $10\,\mathrm{Ohm}$ resistors as shown in Fig. 3.

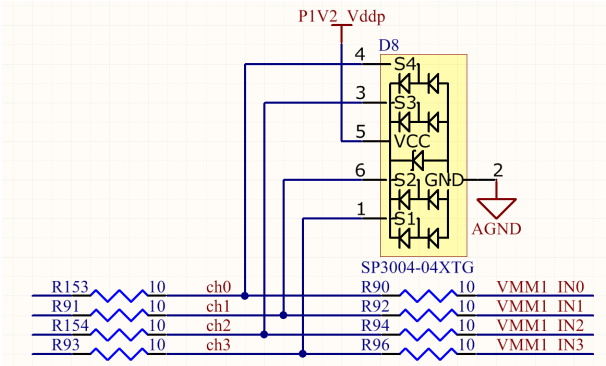

Fig. 3: Initial protection scheme using the SP3004 series diodes. Later, was proved that this circuitry is not enough to protect the inputs of the VMM channels.

Later the SP6003 diodes and the protection circuitry of the MMFE1 proved to be inefficient to protect the channel inputs of the VMM. For that reason a more robust protection scheme was used on the new version of the board as it is described in the next section.

For the Ethernet interface Marvell's 88E1111-B2-BAB1C000 was used which achieves a 10/100/1000 Mbps Ethernet. Communication with the software is established by using the UDP protocol and all configuration parameters for both VMM and FPGA are set by the corresponding Graphical User Interface (GUI). Moreover seven user Light Emitting Diodes (LED) and a six position dual in-line package (DIP) switch are used. An extra uHDMI connector was used as

alternative interface for the clock, trigger and reset signals. A mini Serial Attached Small Computer System Interface (SCSI) (miniSAS) connector is also used for interfacing with the Level-1 Data Driver Card (L1DDC) aggregator board [4]. By using the L1DDC board it is possible to utilize the exact readout scheme thas was designed for the upgrade of the NSW.

B. Test beam

The MMFE1 boards were tested with two ($10\,\mathrm{cm} \times 10\,\mathrm{cm}$ resistive strip micromegas prototypes with 1D readout at the CERN beam facilities. Main goal was to evaluate VMM3 with the use of micromegas detectors and find any potential issues that need to be corrected before the submission of the next version. Small micromegas T and TLP chambers were used at that time. T chambers are prototype micromegas with strip width of $300\,\mathrm{um}$ and strip pitch of $400\,\mathrm{um}$. The TLP chamber is a T-type detector with a strip pitch of $400\,\mathrm{m}$ and strip width of $320\,\mathrm{m}$, split in two parts with different pillar shapes. Three scintillator coincidence was used to provide the trigger to the boards. The setup of the test beam is shown in Fig. 4.

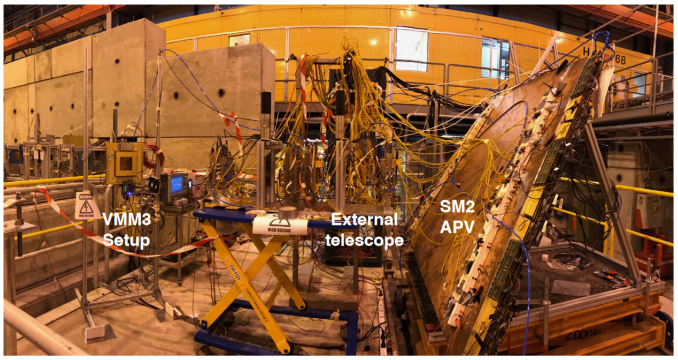

Fig. 4: Setup of the test beam area. On the left side of the picture the MMFE1 boards mount on the T and TLP detectors are visible along with the GEM telescope on the center and the Small Module prototype-0 (SM2) micromegas on the right.

A readout of about $25\,\mathrm{KHz/channel}$ was achieved which corresponds to $100\,\mathrm{K}$ events / spill or more. A spatial resolution of $65\,\mathrm{um}$ has been measured for perpendicular to the detector plane tracks, as shown in Fig. 5.

III. GPVMM BOARD DESCRIPTION

A second board, more handy and robust to the chamber discharges, the GPVMM, was design and fabricated. To keep the same low noise levels with the MMFE1 board, the same design, layout rules and stackups were used. Board was extended by a few milimiters (new dimensions: $132.84\,\mathrm{mm} \times 117.35\,\mathrm{mm}$) in order to house the new protection scheme. A more flexible, three row connector (9-1393644-1) with a standard $2.54\,\mathrm{mm}$ pitch was used for interfacing with various type of detectors. GPVMM board is shown in Fig. 6.

Furthermore a series of tests for the protection of the input circuitry of the VMM showed that an additional Transient Voltage Suppression (TVS) diode should be used. The

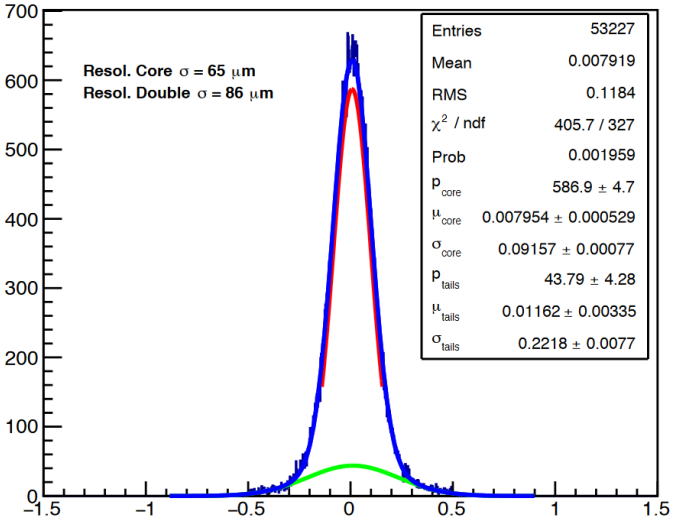

Fig. 5: Residual distribution of two micromegas (T and TLP) chambers with $400\,\mathrm{um}$ strip pitch obtained with charge centroid method. The distribution is fitted with a double Gaussian function. The resolution is demonstrated to be $65\,\mathrm{um}$ from the core of the gaussian fit.

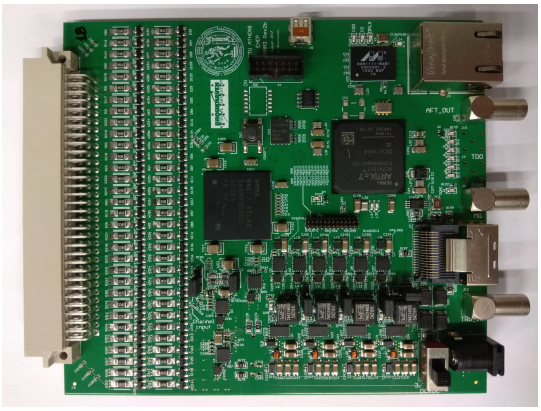

Fig. 6: GPVMM board. On the left the new connector and the protection circuitry are visible. Moreover at the center of the board the DIP header for the twelve VMM direct outputs is also visible.

protection scheme of Fig. 7, derived from Cathode Strip Chambers (CSC) technology, was used in the GPVMM board. Additionally, twelve direct outputs of the VMM were driven to a $1.27\,\mathrm{mm}$ DIP header.

These boards were basically used for performance studies of the full size sTGC prototypes (Module-0) in Weizmann Institute of Science, in Israel by Ilia Ravinovich et al. Noise levels driven by MO output were measured for both pad and wires of the sTGC detectors and for different gains. In Fig. 9 the noise measurements of the wires for $3\,\mathrm{mV/fC}$ gain and $200\,\mathrm{pF}$ wire capacitance is presented. The standard deviation of the distribution is proven to be proportional to the gain. In Fig. 10 the noise measurements of the pads for $3\,\mathrm{mV/fC}$ gain and $100\,\mathrm{pF}$ effective capacitance (after a pi-network) is

presented. In this case, noise is not proportional to the gain and is close to the theoretical limit ($2000\,e$) with $100\,\mathrm{pF}$ input capacitance.

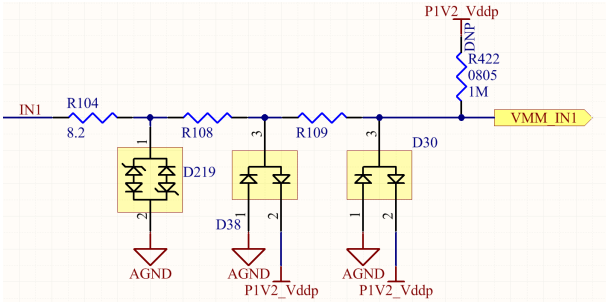

Fig. 7: Alternative protection scheme of the GPVMM board. Circuitry is the same with the one that was used in CSC detectors utilizing TVS and BAV99 diodes. A pull-up resistor was also used for the bias of the input possitive pulses.

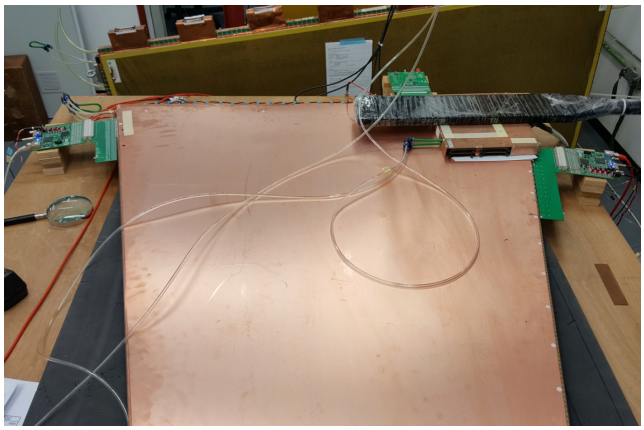

Fig. 8: Full size prototype Module-0 (QL1) chamber equipped with three GPVMM boards connected to nine wires groups, 16 pads and 30 strips through adapter boards.

IV. Conclusion

MMFE1 and GPVMM boards are flexible and mutlifunctional boards with almost perfect noise performance and can be used by many type of detectors. The protection scheme on the GPVMM boards prove to be robust enough to protect the VMM channels from electrostatic discharges. Along with the corresponding GUI the boards are extremely easily to be used even by a novice user. The boards used for data taking during test beams with prototype micromegas (T and TLP) detectors and data analysis showed that VMM ASIC is capable to fulfil all the needs of the ATLAS experiment and can be successfully used on the upgrade of the NSW. Finally GPVMM boards were also used for performance studies of full sTGC modules.

References

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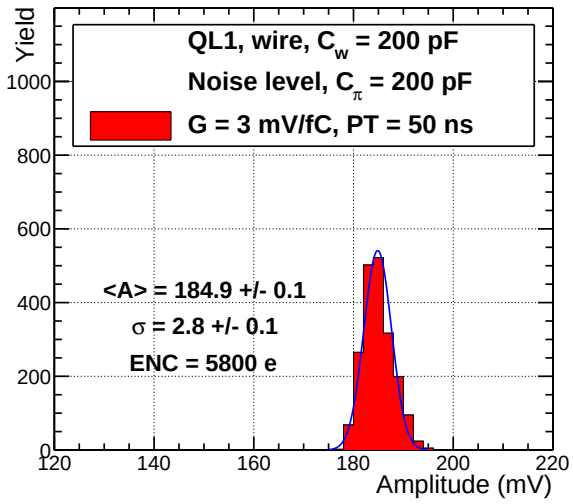

Fig. 9: GPVMM board noise measurement on the wire sTGC with a wire capacitance of $200\,\mathrm{pF}$ and $3\,\mathrm{mV}$ gain. Noise was measured with the MO output of the VMM and the standard deviation of the distribution is 2.8 (proportional to the gain of the VMM).

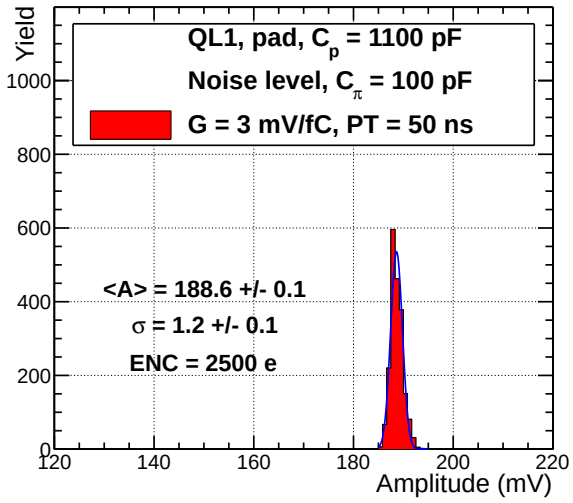

Fig. 10: GPVMM noise measurement on the pad sTGC with an effective capacitance of $100\,\mathrm{pF}$ due to a pi-network, and $3\,\mathrm{mV}$ gain. Noise was measured with the MO output of the VMM and the standard deviation of the distribution is 1.2 (appeared to be not proportional to the gain of the VMM).

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