PROCEEDINGS OF SCIENCE

Development of the jet Feature EXtractor (jFEX) for the ATLAS Level 1 Calorimeter Trigger Upgrade at the LHC

Marcel Weirich*
Institut für Physik, Johannes Gutenberg-Universität, Mainz, Germany
E-mail: weirich@uni-mainz.de

B. Bauss[1], A. Brogna[2], V. Büscher[1], R. Degele[1], H. Herr[1], C. Kahra[2], S. Rave[1], E. Rocco[1], U. Schäfer[1], J. Souza[1], S. Tapprogge[1]

[1] *Institut für Physik, Johannes Gutenberg-Universität, Mainz, Germany*
[2] *PRISMA Detektorlabor, Johannes Gutenberg-Universität, Mainz, Germany*

To cope with the enhanced luminosity delivered by the Large Hadron Collider from 2021 onwards, the ATLAS experiment has planned several upgrades. The first level trigger based on calorimeter data will be upgraded to exploit fine-granularity readout using a new system of Feature EXtractors (FEXs, FPGA-based trigger boards), each optimized to trigger on different physics objects. This contribution is focused on the jet FEX. The main challenges of such a board are the input bandwidth of up to 3.1 Tbps, dense routing of high-speed signals and power consumption. The design, PCB simulations and results of integrated tests of a prototype are shown in this document.

ATL-DAQ-PROC-2017-032
15 October 2017

Topical Workshop on Electronics for Particle Physics
11 - 14 September 2017
Santa Cruz, California

*Speaker.

1. Introduction and Motivation

Due to the increased luminosity ($\sim 2.5 \times 10^{34}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$) and average number of interactions per bunch crossing (~ 60) expected in Run 3 (starting 2021) after Long Shutdown 2 (LS2), ATLAS [1] has planned a major upgrade of the sub-detectors (Phase 1 upgrade [2]). The Level 1 Calorimeter Trigger system (L1Calo) is redesigned to take advantage of the latest technology available by exploiting higher granularity data from the calorimeter (see Figure 1). It consists of three subsystems, called Feature EXtractors (FEXs), each optimized to trigger on different physics objects: eFEX (electromagnetic FEX) identifies electron, gamma and tau signatures; jFEX (jet FEX) identifies jets and large-area taus and calculates energy sums including missing transverse energy; gFEX (global FEX) identifies large-area jets and calculates global variables.

In the following the design, PCB simulations and performance tests of a jFEX prototype are shown.

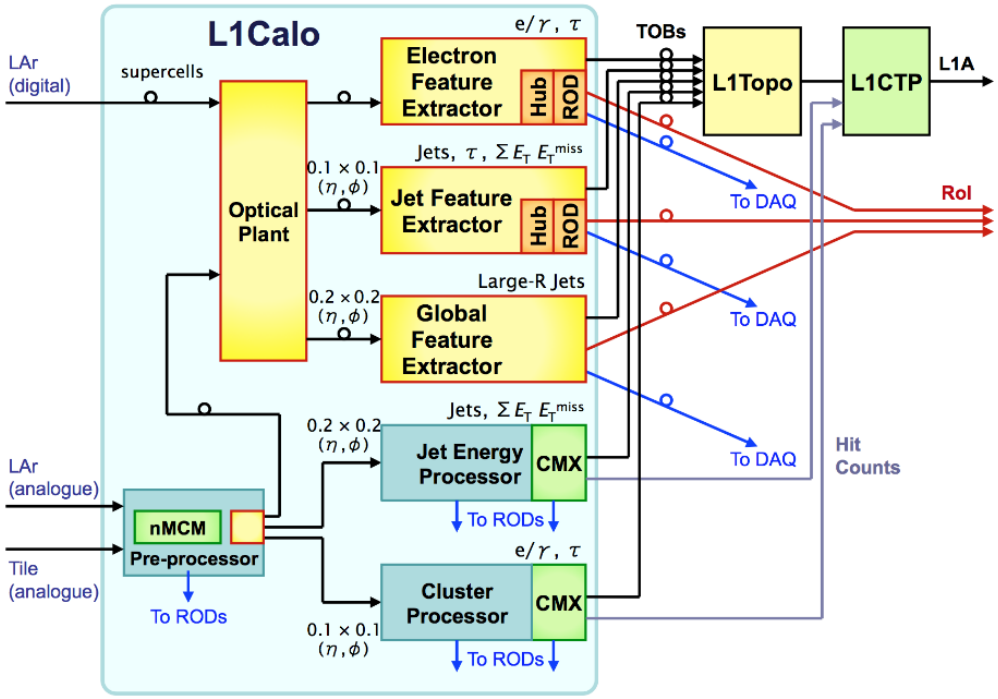


Figure 1: Schematic view of the upgraded L1Calo system architecture after LS2. The blue and green components are part of the current system, the yellow and orange ones will be added as part of the Phase 1 upgrade. Taken from Ref. [2].

2. The jet Feature EXtractor (jFEX)

2.1 Requirements

The jFEX is intended to receive high granularity data from the calorimeters (0.1×0.1 in $\eta \times \phi$

for the central calorimeter, larger in the forward regions)[1] and identify jets and large-area taus. It also calculates global variables like the total transverse energy $\sum E_{\mathrm{T}}$ and the missing transverse energy $E_{\mathrm{T}}^{\mathrm{miss}}$.

In total, 6 modules, each populated with 4 processor "FPGAs" (Field Programmable Gate Array), are required to cover the full calorimeter system. Each jFEX module covers a ϕ ring (η slice), while each FPGA covers a quarter of a ϕ ring. The input bandwidth of the jFEX needs to be high enough to receive the highest possible E_{T} resolution and to have the capability to identify large-area jets, which cover an area of up to 1.7×1.7 in $\eta \times \phi$. Since for large-area jets data from half of the ϕ range is needed, data duplication at board level between a processor FPGA and its two neighbors is required.

The baseline algorithms running on the jFEX processors are the highly parallelized identification of local maxima together with the calculation of jet energy sums e.g. by weighting adjacent trigger towers ("Gaussian Weighting Algorithm").

2.2 Features and Design Challenges

The jFEX is an ATCA board populated with 4 Xilinx UltraScale+ FPGAs (XCVU9P-FLGA2577) [3] as processors. In addition, an extension mezzanine is used, where a smaller FPGA manages board control and FPGA configuration / monitoring via IPBus. Each processor FPGA comes along with 120 Multi-Gigabit transceivers (MGT). The incoming data is received via optical fibers and converted to electrical signals with the help of optical transceivers (Avago "MiniPODs"). jFEX is designed to support line rates of up to 12.8 Gbps resulting in a total input data bandwidth of 3.1 Tbps.

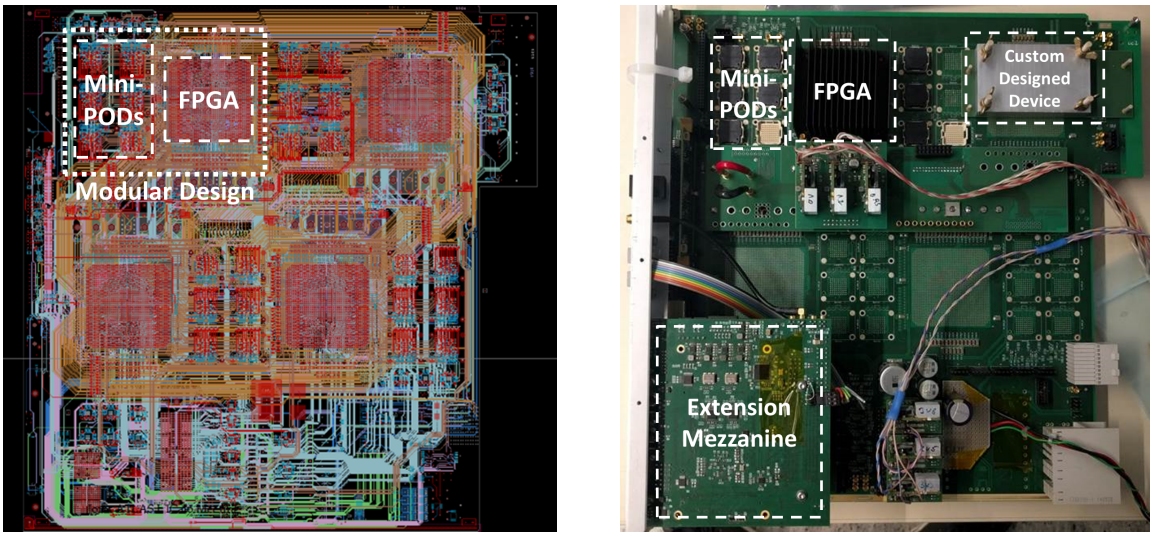
The ATCA board consists of 24 layers (including ground layers) of MEGTRON6. The material was chosen because of its low dielectric constant (low attenuation). A high number of high-speed data lines from the optical receivers to the processors and from each processor to its two neighbors have to be routed paying attention to signal integrity issues, e. g. avoiding cross talk. In total, the jFEX PCB layout has more than 16000 connections (see Figure 2(a)).

Each processor needs to share the data it receives directly with its two neighbors. Passive splitting would affect the signal quality, therefore a feature of the MGTs is used: The incoming serial data is digitized in the analogue front-end of the receiver and forwarded to the FPGA fabric. In parallel a connection to the transmitter of the MGT channel allows the received data to be re-transmitted to the neighboring processor before it is decoded.

2.3 Power and Signal Integrity Simulations

The PCB design was accompanied by power and signal integrity simulations. Concerning the power consumption the main focus was on the voltage drop on the power planes of the processor FPGA supply voltages. It was reduced by optimizing the PCB layout using larger power planes and higher copper thickness (up to 105 μm). Thus the voltage drop was reduced, e.g. for the VCCINT voltage (1 V, 60 A, main voltage of the FPGA) to 12 mV, which is less than half of the maximum specified by Xilinx (30 mV).

[1] Pseudorapidity $\eta = -\ln\left[\tan\left(\frac{\theta}{2}\right)\right]$; θ: polar angle; ϕ: azimuthal angle



(a) jFEX PCB layout **(b)** jFEX prototype

Figure 2: (a) Layout of the jFEX PCB (modular design is used four times); (b) Image of the jFEX Prototype (assembled with one processor FPGA).

Post layout simulation of the PCB traces for MGT links were carried out using "Cadence Sigrity PowerSI" [4]. The results were compared with recommendations of the SFP+ specifications (industrial standard with similar line rates and use cases) [5] without seeing any larger problems.

2.4 Prototype Test Results

The jFEX prototype was received in December 2016 (see Figure 2(b)) and assembled with one processor FPGA (Xilinx UltraScale XCVU190-FLGA2377). At CERN it was tested together with two other modules ("LATOME" and "FTM", both provide optical signals at high speed), using pseudo-random data (Xilinx "iBERT IP Core" [6] with PRBS31) and a simple custom protocol encoded with 8B10B. The tests were performed at two different line rates (11.2 Gbps and 12.8 Gbps). The iBERT tests were run to a bit error rate of better than 10^{-15} (on 48 links with LATOME and 60 links with FTM) without seeing a single error.

To verify the on-board data duplication measurements were performed successfully on the jFEX prototype at 12.8 Gbps link speed using iBERT and a custom designed device connecting transmitters with receivers on the position of a second FPGA (compare with Figure 2(b)).

In total, all tests were successful and the module meets the specifications.

3. Conclusions and Outlook

In 2021 the LHC will be able to deliver data at highly increased luminosity and event rate. Thus an upgrade of the ATLAS Level 1 Calorimeter Trigger System is required. The jFEX is one of the new subsystems and is mainly intended to identify jets and large-area taus. It is an ATCA board with 4 Xilinx UltraScale+ FPGAs (120 MGTs per FPGA) and is designed to have an input bandwidth of up to 3.1 Tbps. The PCB layout was accompanied and checked by power and

signal integrity simulations. A prototype was received in December 2016 and has been tested very successfully so far.

The final prototype is in production, the final production is planned for July 2018.

References

[1] ATLAS Collaboration, *The ATLAS Detector*, JINST 3 (2008) S08003, https://cds.cern.ch/record/1129811

[2] ATLAS Collaboration, *Technical Design Report for the Phase-I Upgrade of the ATLAS TDAQ System*, CERN-LHCC-2013-018, https://cdsweb.cern.ch/record/1602235

[3] Xilinx, UltraScale Architecture and Product Data Sheet: Overview, https://www.xilinx.com/support/documentation/data_sheets/ds890-ultrascale-overview.pdf

[4] Cadence, *Sigrity PowerSI - Fast and accurate electrical analysis of full IC packages or PCBs*, https://www.cadence.com/content/cadence-www/global/en_US/home/tools/ic-package-design-and-analysis/si-pi-analysis-point-tools/sigrity-powersi.html

[5] SFF Committee, *SFF-8431 Specifications for Enhanced Small Form Factor Pluggable Module SFP+*, ftp://ftp.seagate.com/sff

[6] Xilinx, IBERT for UltraScale GTY Transceivers, https://www.xilinx.com/products/intellectual-property/ibert_ultrascale_gty.html