Challenges and Performance of the Frontier Technology Applied to an ATLAS Phase-I Calorimeter Trigger Board Dedicated to the Jet Identification

B. Bauss[1], A. Brogna[2], V. Buescher[1], R. Degele[1], H. Herr[1], C. Kahra[2], S. Rave[1], E. Rocco[1], U. Schaefer[1], J. Souza[1], S. Tapprogge[1], and M. Weirich[1]

[1] Institut fuer Physik, Johannes Gutenberg - Universitaet, Mainz, Germany
[2] PRISMA Detektorlabor, Johannes Gutenberg - Universitaet, Mainz, Germany
E-mail: ckahra@uni-mainz.de

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1 Abstract

The 'Phase-I' upgrade of the Large Hadron Collider (LHC), scheduled to be completed in 2021, will lead to an enhanced collision luminosity and an increased number of interactions per LHC bunch crossing. To cope with the new and challenging accelerator conditions, all the CERN experiments have planned a major detector upgrade to be installed during the associated experimental shutdown period. One of the physics goals of the ATLAS experiment is to maintain sensitivity to electroweak processes despite the increased event rate. To this end, the first-level hardware trigger based on calorimeter data will be upgraded to exploit fine-granularity readout using a new system of Feature EXtractors (FEXs), which each uses different physics objects for trigger selection. There will be three FEX systems in total, the electron, the jet and the global Feature Extractor. This contribution focuses on the first prototype of the jet FEX (jFEX) and presents the hardware design challenges and adopted solutions to preserve signal integrity within a densely populated high signal speed ATCA board.

2 Introduction

The Large Hadron Collider (LHC) at CERN will stop operation in 2019 to be upgraded to an instantanenous luminocity (L) of about $L \approx 2.5 \times 10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ during Long Shutdown 2 (LS2). Restarting operation for Run 3 (planned for 2021) it is expected to have an average number of interactions per bunch crossing of ≈ 60. To cope with these new conditions an upgrade programme, 'Phase-I' upgrade, for the trigger and data acquisition system (TDAQ) of the ATLAS experiment [1] has been planned [2]. As part of this, the upgrade of the Level-1 Calorimeter trigger system (L1Calo)[3] will include the new sub-system jet Feature EXtractor (jFEX), which is the focus of this contribution. In figure 1 an overview of the Phase-I L1Calo system is given.

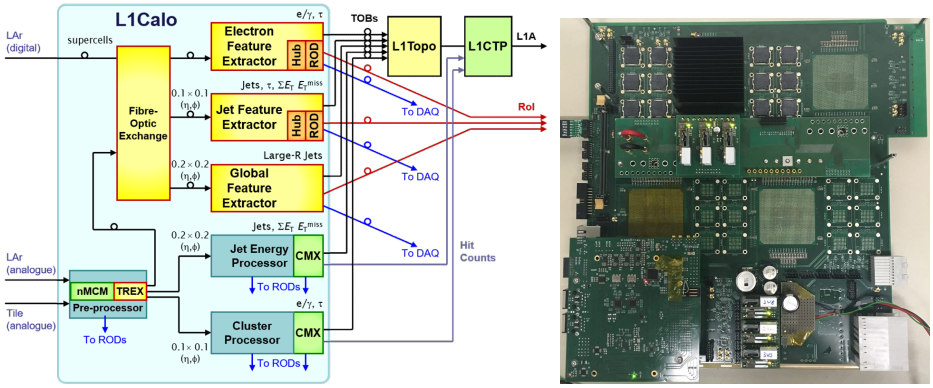

Fig. 1. Left: Overview of the planned Level-1 Calorimeter trigger system for LHC Run 3 (Blue and green: the legacy system; yellow: new components added as part of the Phase-I upgrade); Right: photograph of the first jFEX prototype (assembled with only one processor FPGA)*

3 The jet Feature Extractor

3.1 Requirements

The jFEX is intended to receive data from the calorimeters and to identify jet and large-area tau candidates in real-time. It also calculates global variables like the total transverse energy $\sum E_t$ and the missing transverse energy $\boldsymbol{E}_t^{\text{miss}}$. To cover the the full η range (pseudorapidity $\eta \equiv -\ln\left[\tan\left(\frac{\theta}{2}\right)\right]$, θ: polar angle), there will be 6-7 jFEX modules (the handling of $\eta = 0$ is still under discussion), each with four processors. Each module receives for its η slice the full ϕ range (azimuthal angle). The input bandwidth of the jFEX needs to be high enough to receive the calorimeter data with the highest possible E_t resolution and to have the capability to identify "fat jets" (jets with an area up to 1.7×1.7 in $\eta \times \phi$). To identify a fat jet, a jFEX processor needs to receive data from half of the ϕ range processed by a jFEX. However, each processor receives only one quarter of the ring directly, so data duplication at board level between a processor FPGA and its neighbours is required. In the jFEX processors several algorithms will run with the "Sliding window with Gaussian weighting" algorithm [2] as baseline algorithm for jet identification. The latency budget for jFEX is ≈ 387.5 ns.

3.2 Features and Challenges

The jFEX board is designed as an ATCA board populated with four Xilinx Ultrascale XCVU190FLGA2577 FPGAs as processors. Each of these FPGAs provide 120 Multi-Gigabit transceivers (MGT, high-speed receiver-transmitter pairs for serial data). The line rate of the input data is still under discussion, but jFEX is designed to support line rates of 12.8 Gbps. At this line rate the

total input data bandwidth per jFEX board would be 3.1 Tbps.
The jFEX PCB layout has in total more than 16000 connections, where a high number of high-speed data lines from the optical receivers to the processors, and from each processor to its neighbours, have to be routed paying attention to signal integrity issues (avoiding cross-talk). For the stack-up of the 24-layer PCB the high-speed material MEGTRON6 was used for the signal layers, which are alternated with ground layers. The processors need to share the data that they receive directly with their neighbours. To avoid passive splitting, which would affect the signal quality, a feature of the MGTs of the processor FPGAs is used. The incoming serial data is digitized in the analogue front-end of the receiver and a connection to the transmitter of the MGT channel allows the received data to be re-transmitted to the neighbouring processor before it is decoded. This mechanism for data duplication was proven to work reliably by doing a bit error rate test (BERT) with the Xilinx "iBERT" IP Core on a Xilinx Ultrascale evaluation board VCU110. The test was run to a bit error rate of less than 2.15×10^{-16} at a line rate of 28 Gbps without seeing a single error.

3.3 Signal Integrity Simulations

The layout of the jFEX PCB was accompanied by signal integrity simulations for the high-speed data links. To evaluate the simulation results the recommendations of the SFP+ specification [4] were taken for comparison, because it is an industrial standard with similar line rates and use cases. The left plot in figure 2 shows the simulation results for the S_{11} parameters. Only a few traces exceed the recommendation for max. channel return by less than 2 dB.
The simulation results for the S_{21} parameter are shown in the right plot of figure 2. The jFEX board was designed to have very low attenuation, e.g. by choosing the material MEGTRON6 for its low dialectric constant, but the specification recommends a minimum attenuation to damp occuring reflections. The channel transfer is about 5 dB "too good" as its attenuation is lower than the recommendation, which should be no problem as long as the reflections are low.

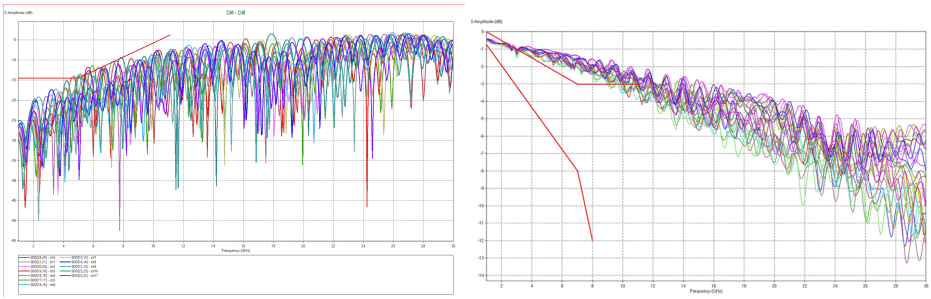

Fig. 2. Results of signal integrity simulations. Left: S_{11} parameter (channel return); Right: S_{21} parameter (channel transfer)*.

3.4 Link-speed tests

The first jFEX prototype (see figure 1) was delivered in December 2016. Link-speed tests with other modules, the LATOME (LAr Trigger prOcessing MEzzanine) and the FTM (FEX Test Module), were performed in March at CERN. These tests were done with two different data sets, pseudo-random data (Xilinx iBERT IP Core with PRBS31) and a simple custom protocol (encoded with 8B10B), at the two line rates 11.2 Gbps and 12.8 Gbps. The iBERT tests were run on 48 links with LATOME and 60 links with FTM to a bit error rate of better than 1×10^{-15} without seeing a single error.

3.5 Power Integrity Simulations

Because of the high power consumption of the processor FPGAs the PCB design was also accompanied by power integrity simulations. The main focus here was on the voltage drop on the power planes of the processor FPGA supply voltages, which are specified to have a tolerance of 3%. Optimizing the PCB layout by larger power planes and higher copper thickness (up to 105 μm) the voltage drop on the power planes was reduced e.g. for the VCCINT voltage to 12 mV, which is less than the half of the specifications (30 mV).

3.6 Conclusions and Outlook

The challenging luminosity conditions expected for Run 3 of the LHC require an upgrade of the ATLAS Level-1 Calorimeter trigger system. The jFEX, one of the new sub-systems, is designed to have an input bandwidth of up to 3.1 Tbps. Each jFEX module is equipped with four Xilinx Ultrascale processor FPGAs. The PCB layout was accompanied and checked by power, thermal and signal integrity simulations. The first prototype was produced in December 2016 and the power and thermal measurements of the board itself and the link-speed tests with other modules as data sources have been very successful so far. The final production of the full system is scheduled for July 2018 and the installation and commissioning in ATLAS will take place before the LHC restart in 2021.

References

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