A TTC to Data Acquisition interface for the ATLAS Tile Hadronic calorimeter at the LHC

Francisco García*, Fernando Carrió*, Luca Fiorini*,
Raimundo García†, Julio Martos†, Jesus Soret†, José Torres†,
Alberto Valero*, Juan Valls*, Pedro Zuccarello*
*Instituto de Física Corpuscular IFIC, Universidad de Valencia-CSIC
†Departamento de Ingeniería Electrónica, ETSE-UV

ATL-TILECAL-PROC-2017-003
05 April 2017

***Abstract*—TileCal is the central tile hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider at CERN. The TDI is a VME 6U module able to receive and decode the Trigger, Timing and Control information and transmit it to the Data Acquisition system in the TileCal back-end crates. The input stage is an optical receiver connected to the CentralFPGA which unpacks and decodes the TTC signals. The data is stored in internal buffers and can be read out by a DAQ application through VME. In addition, the TTC information in the TDI module can be also reached through an Ethernet port on the front panel. Finally, the TDI module is able to transmit signals to the trigger system to stop the generation of trigger a busy signal to prevent the generation of Level1 accepts while the internal buffer is full. The system functionalities and communication protocols are all implemented in firmware in the CentralFPGA. The TDI module is particularly important during calibration runs to decode and store the configuration used in every processed event. The TDI functionalities are implemented in a Xilinx Spartan 6 FPGA which provides flexibility and the possibility of upgrading the functionalities along the lifetime of the board which should be operative until the LHC technical stop in 2024. In this contribution we define the components and interfaces of the TDI module, the main functionalities and a detailed description of the board design.**

I. Introduction

TileCal is the central tile hadronic calorimeter of the ATLAS experiment [1] at the Large Hadron Collider (LHC) at CERN. It is a sampling calorimeter where scintillating tiles are embedded in steel absorber plates. The tiles are read-out using almost 10,000 photomultipliers which convert the light into an electrical signal. These signals are digitized and stored in pipeline memories in the front-end electronics. Upon the reception of a trigger signal, the PMT data is transferred to the Read-Out Drivers in the back-end electronics which process and transmit the data to the ATLAS Data AcQuisition (DAQ) system. The Timing, Trigger and Control (TTC) system [2] is an optical network used to distribute the clock synchronized with the accelerator, the trigger signals and configuration commands to all the read-out electronics components. During physics operation, the TTC system is used to configure the electronics and to distribute trigger information, used to synchronize the different parts of the readout chain. This information includes event identification, synchronization signals and configuration and calibration commands.

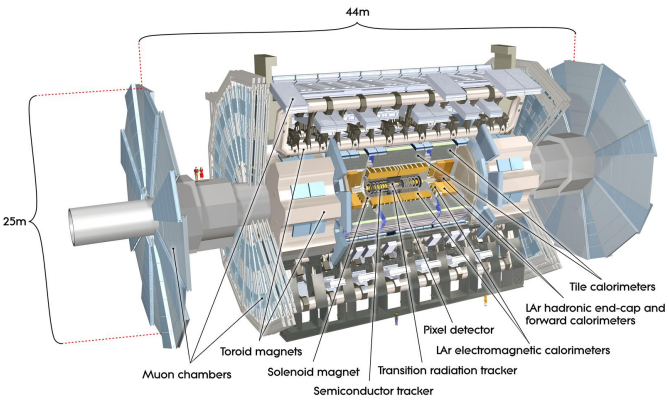

Fig. 1. Sketch of the ATLAS experiment.

The TTC signals are encoded with a 160.32 MBaud biphase mark encoder which time-division multiplexes 2 channels, clock and data, using a balanced DC-free code. Currently, TileCal uses a TTCpr [3] card to decode the TTC information at the back-end electronics crates. This board is equipped with an Altera 10K30A which is con-

nected to the TTCrx [4], an AMCC 5933 and 4 blocks of 8K x 16b FIFO. The computer can access the TTCpr memory through a DMA controller.

II. Motivation

The need for the TDI is two-fold. First, the current hardware for TTC to VMEbus communication (TTCpr) is aging while it should be operative until the LHC Long Shutdown 3 planned for 2024. Second, it is not possible to manufacture new cards because most of the components have been discontinued. Therefore, it was decided to design a new board with improved functionalities. While it's predecessor was a PCI Mezzaine Card (PMC) for use in a VME Single Board Computer, this is a 6U size VME board, that will act as a slave to the processor, as specified by the VME protocol [5]. Figure 2 shows the layout of the TDI PCB design. In the far left side we have the VME connectors, to their right we have the VME level shifters, which are connected to the FPGA at the center of the card. On the top we have the power supply and the clock and data recovery IC. Finally, on the rightmost part of the PCB we have the optical and JTAG connectors and some status LEDs. The different colored lines correspond to traces in different layers of the PCB using green for the top, yellow for the bottom, and blue and magenta for the internal signal layers.

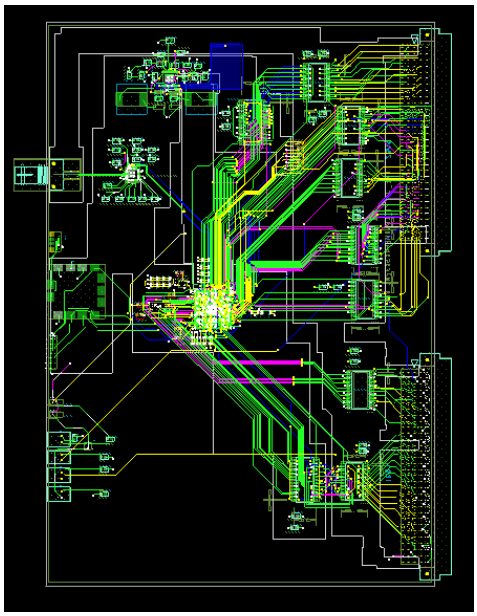

Fig. 2. Layout of the TDI VME module.Green corresponds to top layer, yellow to bottom, and blue and magenta are internal signal layers.

III. Architecture of the TDI

The TTC information is received through an optical receiver, then transmitted to a clock and data recovery integrated circuit (ADN2814 [6]), which unpacks and recovers the data and clock transmitted by the TTC system (Figure 3). Both clock and data differential signals are then sent to the Xilinx Spartan-6 [7] FPGA.

The TTC information is decoded and saved in FIFO memories in the FPGA. In addition, the FPGA implements the VME protocol and provides an interface with the VME bus. From the SBC thus, the decoded TTC information is accessible through the VME bus.

We can also access this information trough Ethernet. From the FPGA we connect a KSZ9021RN, an IC that acts as a Gigabit Ethernet Transceiver. It uses RGMII (Reduced Gigabit Media Independent Interface) to connect to the FPGA. It connects to the Ethernet cable using a magnetic module, embedded in the connector, to isolate the connection. The communication is done using, for example, the IPbus protocol, although other protocols can be implemented into the FPGA.

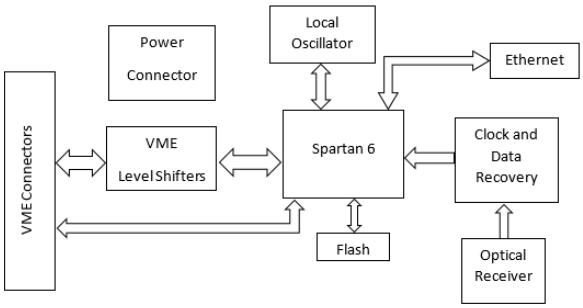

Fig. 3. Block diagram of the TDI VME module.

The card has two VME connectors, each one with 160 pins. The connectors provide up to four voltages (3.3V, 5V, 12V and -12V) to power the board. In this design we only use the 5V pins to power up the board and we use an integrated circuit to convert those 5V into 3.3V and 1.2V. Most of the components are powered at 3.3V, for example the FPGA IO banks or the VME level shifters. 1.2V is used only for the FPGA core power, and 5V is used for the VME level shifters and the fiber optics transducer. In addition the TDI module can be powered through a 4-pin Molex on-board connector for standalone operation outside the VME crate.

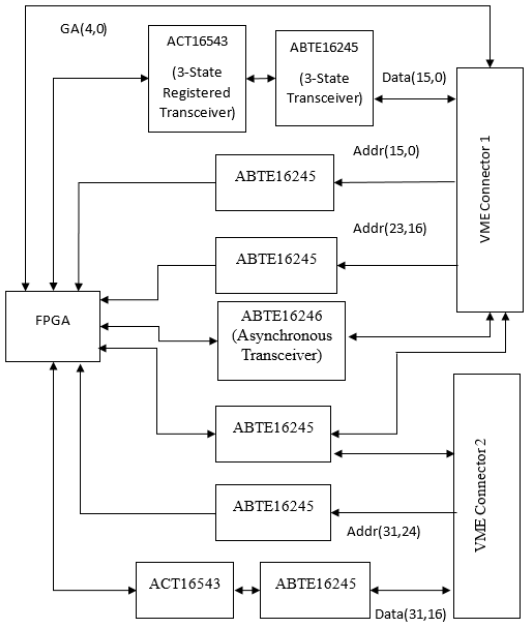

Fig. 4. Block diagram of the VME signals.

Figure 4 shows a simplified diagram of the communication and dataflow between the FPGA and the VME connector. Switching bus level shifters ICs are used to implement the bidirectional 32-bit address and data buses (ABTE16245, ABTE16246 and ACT16543). Other signals are for the interrupts or address width selection. The level shifters convert the signals from the FPGA voltage levels into the VME bus standard ones and vice versa.

The fiber optics transducer converts the optical signal into an electrical differential pair which is transmitted to the ADN2814, which decodes the clock and the data. Both of them are LVDS pairs. Figure 5 presents a diagram of the TTC differential pairs decoded in the ADN2814 and transmitted to the FPGA.

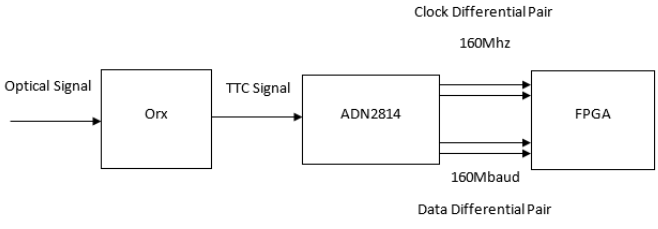

Fig. 5. Block diagram of the differential signals.

The FPGA is a XC6SLX25-FTG256 Spartan-6 model from Xilinx, with 24,051 logic cells and 186 user IO pins. It gives enough configurable logic and connectivity for our needs. A local oscillator provides a 100MHz clock to the FPGA, and a 16Mb SPI serial flash memory is used for FPGA configuration. The FPGA is powered with 1.2V and 3.3V.

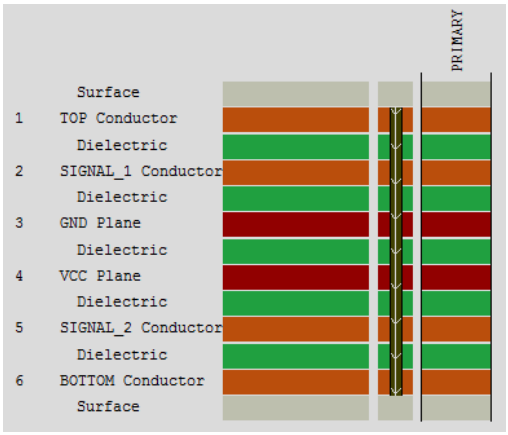

Fig. 6. Stackup of the TDI PCB.

The board has six layers, four for routing signals, one for power and one for ground. Standard FR4 is used as a dielectric material (Figure 6).

IV. Operation of the TDI

The main use of the TDI is to bridge the TTC signal from the optical network to the DAQ system on the same crate. The functionality can be divided in two. On one hand we have the clock and data recovery of the TTC signal.

This step is done through the ADN2814 IC, which recovers data and clock. In the FPGA the data received from the differential signals is processed and stored on internal FIFO buffers.

On the other hand the FPGA also acts as a VME interface. The data is made available to the DAQ software trough the VME bus. The single board computer inside the crate runs the software and acts as an arbiter in the VME communication protocol.

In the case when the internal buffers become full, we can send an interrupt to the single board computer which can, trough Ethernet, communicate to the TTC system and stop the generation of trigger signals. When the backlog is cleared, whenever there are no more triggers stored in the buffer, trigger signals can be generated again. The busy signal can also be reset manually, clearing the buffers of any info stored. The number of triggers stored in the buffers can be modified inside the firmware.

In addition, the signal used to stop the generation of triggers can be transmitted to the TTC system trough a dedicated connector located in the front panel. Another possible functionality allows to access the TTC information stored in the internal FIFO memories through an Ethernet connector in the front panel. Thus, the TDI board can be operated in standalone mode, powered by the extra power connector.

V. Summary

The TDI has been designed by the Valencia TileCal group and will be used to provide TTC information to the DAQ system for the TileCal detector. The goal was to develop a module that is able to be integrated into existing VME setups, replacing transparently the current hardware and improving its functionalities. Once development is completed, we will begin production of a small batch of modules and the validation will be performed in the TileCal readout test-bench at IFIC (Valencia).

Acknowledgments

This work has been supported by the project FPA2015-65652-C4-2-R from the Ministry of Economy, Industry and Competitiveness of the Spanish Government and ERDF funds.

References

[1] G. Aad et al., *The ATLAS Experiment at the CERN Large Hadron Collider*, Journal of Instrumentation, Volume 3, August 2008.

[2] B. Taylor, *TTC Distribution for LHC Detectors*, IEEE Trans. Nuclear Science, Vol. 45, 1998.

[3] John W. Dawson et al., *TTCPR: A PMC Receiver for TTC*, 7th Workshop on electronics for LHC experiments, Stockholm, Sweden, 10-14 Sep 2001: Proceedings, pages 215-216, 2001.

[4] J. Christiansen et al., *TTCrx Reference Manual*, http://ttc.web.cern.ch/ttc/ttcrx_manual3.9.pdf, Accessed March 22th 2017.

[5] *VMEbus Technology FAQ*, http://www.vita.com/page-1855175, accessed March 18th 2017.

[6] *ADN2814 technical specifications*, http://www.analog.com/media/en/technical-documentation/data-sheets/ADN2814.pdf, accessed March 18th 2017.

[7] *Spartan-6 Family Overview*, http://www.xilinx.com/support/documentation/data_sheets/ds160.pdf, accessed March 17th 2017.