Readout and Trigger for the AFP Detector at the ATLAS Experiment at LHC

K Korcyl[1,5], M Kocian[2], I Lopez Paz[3] and G Avoni[4]

[1] Institute of Nuclear Physics, Polish Academy of Sciences, Radzikowskiego 152, 31-342 Cracow, Poland
[2] SLAC, 2575 Sand Hill Road, Menlo Park, USA
[3] Institut de Fisica d'Altes Energies (IFAE), The Barcelona Institute of Science and Technology (BIST), 08193 Bellaterra (Barcelona), Spain
[4] INFN - Instituto Nazionale di Fisica Nucleare - Bologna - Italy

E-mail: Krzysztof.Korcyl@ifj.edu.pl

Abstract. The ATLAS Forward Proton is a new detector system in ATLAS that allows study of events with protons scattered at very small angles. The final design assumes four stations at distances of 205 and 217 m from the ATLAS interaction point on both sides of the detector exploiting the Roman Pot technology. In 2016 two stations in one arm were installed; installation of the other two is planned for 2017. This article describes details of the installed hardware, firmware and software leading to the full integration with the ATLAS central trigger and data acquisition systems.

ATL-FWD-PROC-2017-002
14 February 2017

1. The ATLAS Forward Proton (AFP) detector

The AFP detector [1] of the ATLAS experiment [2] allows reconstruction of the momentum transfer and the energy loss of protons emitted in the very forward direction by tagging and measuring their trajectory. At the distance of about 200 m from the ATLAS interaction point (IP) the protons are sufficiently separated from the nominal beam orbit so they can be intercepted by the detectors inserted into the beam pipe aperture using the Roman Pot (RP) technology. In the first stage of the AFP installation during the 2015-2016 LHC winter shutdown, the two Roman Pot stations were installed on one side (Arm C) of IP (see Figure 1), the near station at 205 m and the far one at 217 m from the ATLAS IP. Each station houses a 3D silicon tracker [3]. In 2017, the stations in the other arm will be installed and the far stations on both sides will also be equipped with time-of-flight counters [4] aimed for the background rejection.

The tracker in the stations consists of four pixel modules of about 2x2 cm^2 sensors bump-bonded to the FEI4B readout chip [5]. The sensor was developed for the ATLAS innermost pixel layer (IBL [6]) and modified for AFP [7]. It contains 26880 pixels configured in an array of 80x336 with a pitch of 250x50 μm^2. The FEI4B chip is SEU (Single Event Upset) tolerant and built using the radiation-hard technology. It delivers 8b/10b-encoded data at 160 Mbps rate. In addition to the coordinates of fired pixels, the FEI4B can deliver a trigger signal if any of the enabled pixels records a hit. This signal is

[5] Corresponding author

produced at one of the chip's outputs. For the data taking, the sensors inside the Roman Pots are moved close to the beam at a distance of 20 σ of the beam size, which corresponds to 4-8 mm.

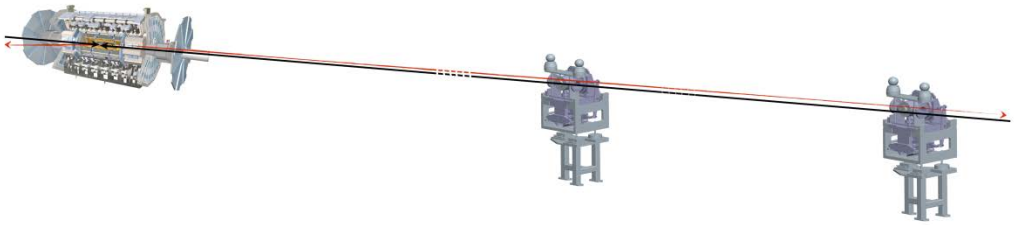

Figure 1. Location of the AFP detectors in one arm. The black arrows represent the LHC incoming proton beams, the red arrows show the scattered proton leaving the interaction point.

2. AFP TDAQ system architecture

2.1. Trigger path

During the low luminosity runs in 2016 the trigger signals from AFP were used in the ATLAS central trigger. The AFP trigger signal originates at the front-end module which provides a logical OR of the discriminated signals from all enabled pixels.

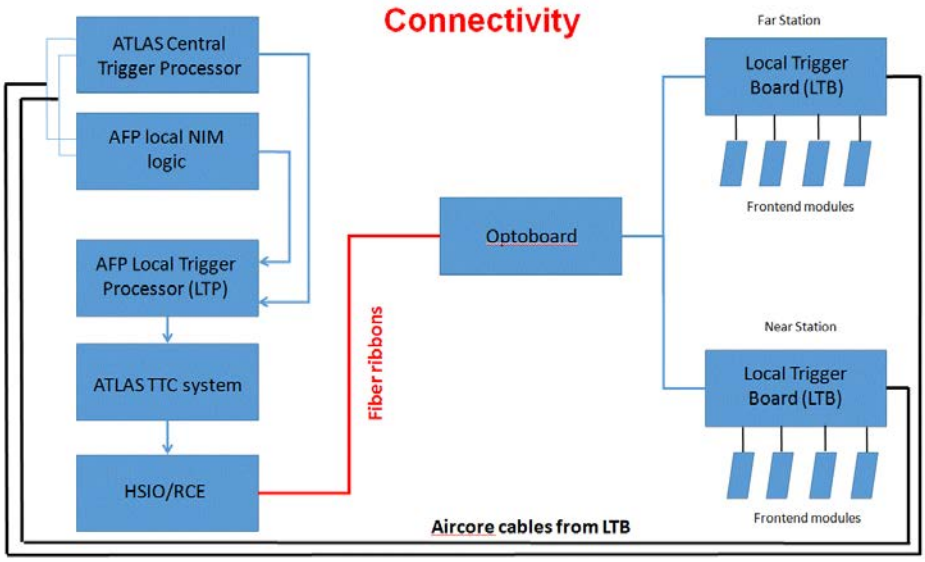

Figure 2. Main path of the trigger signals (black) and data (red)

The signals are then sent to a dedicated ASIC hitbus chip, installed on a Local Trigger Board (LTB) in each station (see Figure 2). The chip has only 3 inputs and a set of jumpers at the LTB allows selection of three out of four FEI4B modules to produce logical OR, AND or majority vote depending on the chip configuration. The output from the chip is in a CMOS standard and the signal is synchronized with the LHC clock. The LTB provides the level conversion to the NIM standard before sending the pulse to the ATLAS first level trigger hardware located in the counting house. To reach the counting house within the ATLAS first level trigger latency, the signals travel over 350 m along special air-core cables with the transmission speed of 93% of the speed of light in vacuum.

At the counting house the signals are split between the ATLAS Central Trigger Processor [8] (CTP) and the AFP local NIM logic. The NIM logic produces logical AND or OR from pulses from the near and far stations before sending the resulting signal to the AFP Local Trigger Processor (LTP). The LTP selects the source of the AFP trigger either as ATLAS, if the AFP participates in the ATLAS combined partition, or, as the NIM local logic, when the AFP performs commissioning or calibration runs. The pulse is then forwarded to the Timing, Trigger and Control system (TTC) [9] which is used by the ATLAS TDAQ to distribute LHC clock and trigger commands. The TTC interface uses both A and B channels to multiplex, encode, perform the optical conversion and distribute the trigger signals to TTC ASIC chips associated with the front-end electronics. The TTC channel A is used to transmit the Level-1 Accept (L1A) signal whereas channel B transmits the trigger control commands (BCR - Bunch Counter Reset, ECR - Event Counter Reset and user commands). In AFP the TTC signals are received at the TTC mezzanine in the HSIO-II board [10] and processed by the on-board firmware.

2.2. Readout path

The main component of the AFP readout path is the HSIO-II board (Figure 3). It houses the Xilinx Artix 200 FPGA, which provides the data flow for the data acquisition system (central chip in Figure 3). The other components contributing to and controlling the AFP DAQ system are the TTC mezzanine, RCE mezzanine and SFP output lines.

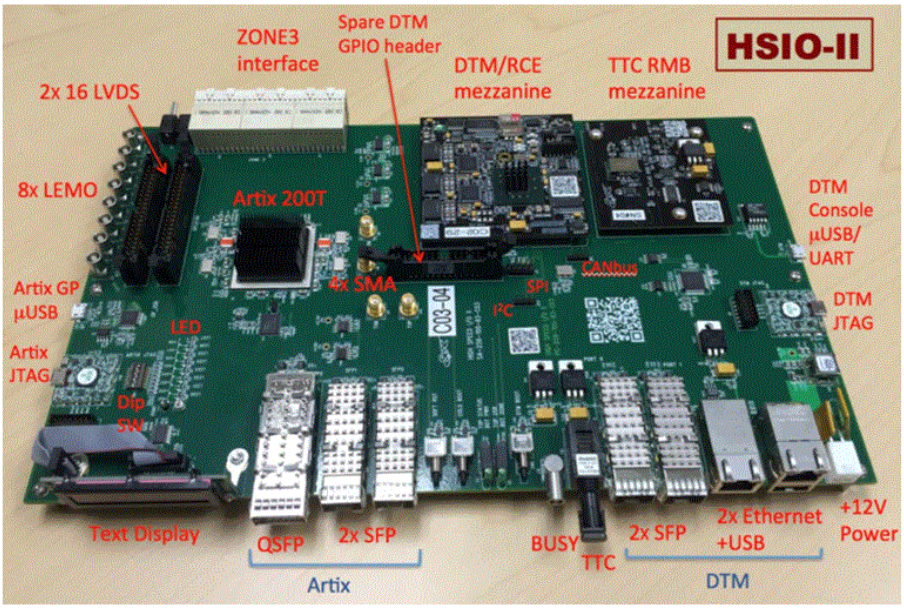

Figure 3. The HSIO-II DAQ board

The firmware in the Artix forms the data request for the front-ends based on information decoded from the bitstream received via the TTC system. This includes the regular triggers as well as the trigger control commands BCR and ECR. The command is then serialized and sent via the interface board (not shown in Figure 3) attached to the ZONE3 connector. The data request is sent via a 350 m long MTP fiber ribbon as a biphase mark encoded bitstream at 80 Mbps and arrives at the Optoboard (see Figure 2). The Optoboard decodes and converts the bitstream to 40 MHz clock and 40 Mbps data stream in electrical symmetric LVDS format and forwards them to the hitbus chip at the LTB. The chip allows a fine time tuning of delays for the clock and command signals. To provide the clock and command for four tracking modules we use two sections of the hitbus chip each one serving three front-ends. In the future, one of the remaining two inputs at the hitbus chip will be used to connect the signals from the time-of-flight detectors.

On the return path, the FEI4B modules send the event data in the form of the 8b/10b-encoded serial data stream at 160 Mbps. The stream of the front-end data arriving via the ZONE3 connector is then deserialized, decoded and stored in a FIFO to become part of the event fragment building. When the data from all front-ends arrive, the FPGA forms a single data fragment and sends it off via the SFP output line to the ATLAS Readout System (ROS – the ATLAS-wide interface between the detector specific DAQ subsystems and the central ATLAS DAQ). The FIFO is a derandomizer, which allows the buffering of few events in the case when the link to the ROS is overloaded. A number of events in the FIFO exceeding a high limit can lead to the generation of a BUSY signal at the front panel connector.

2.3. Control path

The data flow from the front-ends to the ROS is controlled by a chain of interconnected software modules (see Figure 4). The Artix firmware is controlled and configured from the RCE mezzanine on the HSIO-II board. The RCE [10] is built around the Zynq chip and runs ArchLinux. The communication between Artix and RCE is based on the custom PGP protocol. It allows for the transfer of data in both directions between Linux and FPGA registers in Artix. In one direction it is used to download the FPGA registers that define the configuration for data taking, and in the other to sample the statistics information on parameters of the data flow accumulated in the FPGA registers. The operation of the RCE is controlled from the AFP adopted version of the ROD Crate DAQ (RCD) – the ATLAS main software framework providing data acquisition functionality synchronized with the Run Control transitions. The access from AFP RCD to RCE is provided by the Remote Call Framework (RCF) from the Delta V Software [11]. The ATLAS TDAQ state transition commands received from the ATLAS Run Control at RCD are then translated to the related calls to the RCE. The RCE reports back on success or failure of the call what allows synchronization of its operation with the RCD. Due to the security restrictions at CERN the connection between the RCE and the AFP RCD has to go via a private connection with a dedicated Ethernet switch.

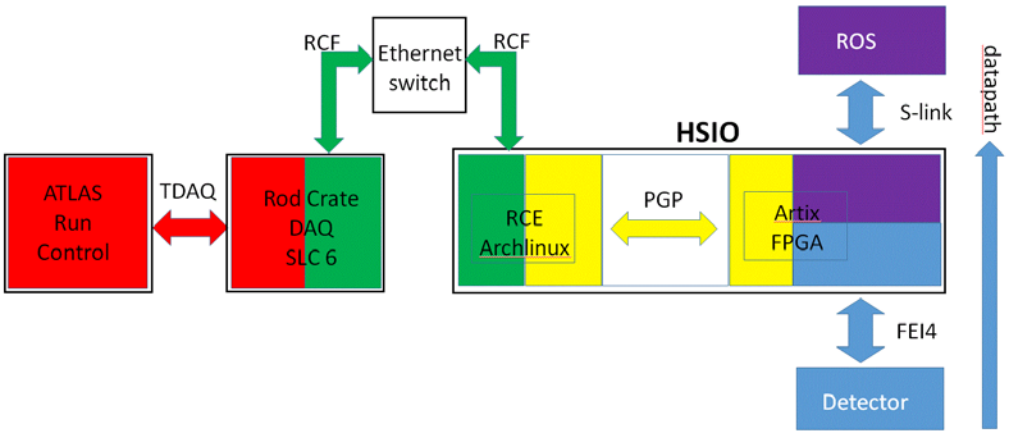

Figure 4. Chain of software components to control and monitor data flow

The RCE enables the monitoring of the data flow performance. With the access to the Artix FPGA registers the data flow statistics, collected by the Artix firmware, can be retrieved and passed on to the RCD. The firmware counts the numbers of processed triggers, cases of the front-end modules not responding, bad formats of the front-end data, occupancy monitoring, etc. The RCD forwards these numbers to the ATLAS Information Service (IS). This information can be inspected with standard tools provided by ATLAS.

The complete set of parameters needed for operation of the trigger and data acquisition systems is stored in the ATLAS DAQ online configuration database.

3. Status and Outlook

AFP – a new ATLAS subdetector to measure trajectories of the forward scattered protons was installed in 2016 and successfully commissioned. Two stations with tracking modules were installed in one arm. The AFP trigger and data acquisition systems were performing smoothly and were fully integrated with the corresponding systems of the ATLAS experiment.

In the winter shutdown of 2016/2017, the detectors in the second arm will be installed. The far stations in both arms will be equipped with the time-of-flight detectors. These new detectors will use the same protocol and format as the silicon detector chips. This will help in the AFP DAQ firmware upgrade (increasing the number of serviced channels will be needed), but will require modifications to the configuration online database to accommodate new objects.

Acknowledgments

This work was supported in part by Polish National Centre grants: UMO-2012/05/B/ST2/02480 and UMO-2015/18/M/ST2/00098, also by the MINECO/FEDER, under grants FPA2015-69260-C3-2-R, FPA2015-69260-C3-3-R and SEV-2012-0234 (Severo Ochoa excellence programme) and by CERN, Geneva, Switzerland.

References

[1] ATLAS Collaboration 2015 *ATLAS Forward Proton-Phase-I Upgrade, Technical Design Report* ATLAS-TDR-024

[2] ATLAS Collaboration 2008 *The ATLAS Experiment at the CERN Large Hadron Collider JINST* **3** S08003

[3] G. Pellegrini et al., *3D double sided detector fabrication at IMB-CNM*; NIM A 699 (2013) pp. 27-30

[4] L. Nozka et al., *Construction of the optical part of a time-of-flight detector prototype for the AFP detector*, Opt. Express, 2016 Nov 28; 24(24):27951-27960.

[5] M. Garcia-Sciveres et al., *The FE-I4 pixel readout integrated circuit*; NIM A 636 Issue 1 pp. 155-159

[6] The ATLAS IBL Collaboration, *Prototype ATLAS IBL modules using the FE-I4A front-end readout chip*, JINST 7 (2012) P11010

[7] S. Grinstein et al., *Module productionof the one-arm AFP 3D pixel tracker*, JINST 12 (2017) C01086

[8] P. Borrego Amaral et al., *The ATLAS Level-1 Central Trigger System*, IEEE Transactions On Nuclear Science VOL. 52, NO 4, Aug 2005

[9] http://ttc.web.cern.ch/TTC

[10] https://indico.cern.ch/event/546846/

[11] http://www.deltavsoft.com