The FTK to Level-2 Interface Card (FLIC)

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***Abstract*—The Fast TracKer (FTK) to Level-2 Interface Card (FLIC) of the ATLAS FTK trigger upgrade is the final component in the FTK chain of custom electronics to connect the system to the High-Level trigger (HLT). The FTK performs full event tracking using the ATLAS Silicon detectors for every Level-1(L1) accepted event at 100 kHz. The FLIC is a custom Advanced Telecommunications Architecture (ATCA) card that interfaces the upstream FTK system with the ATLAS trigger and data acquisition (TDAQ) system, and allows for event processing on commercial PC blades, making use of the 10 Gb Ethernet full mesh ATCA backplane.**

The FLIC receives data on eight optical links at a bandwidth of about 1 Gbps per channel, reformats the data to the ATLAS standard record format, and performs a conversion from local to global module identifiers using look up tables stored in static RAM (SRAM). After processing, the event records are sent out to the TDAQ system using the simple link interface (S-LINK) protocol at 2 Gbps. The data processing is handled in two Xilinx Virtex-6 FPGAs, with two additional Virtex-6 FPGAs communicating with the processor blades over the ATCA backplane. The four FPGAs are connected via a full internal mesh of high speed GTX lines. This paper reports the design goals, implementation, and testing results of the FLIC.

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I. Introduction to the ATLAS TDAQ and Fast TracKer system

THE ATLAS [1] trigger system is deployed to reduce the event rate from the Large hadron collider (LHC) bunch crossing frequency of 40 MHz to about 1000 Hz for permanent storage. For Run 2, the architecture is a two tier trigger system, consisting of a custom hardware-based Level-1 (L1) trigger [2] and a computer-based High-Level trigger (HLT) [3]. The L1 trigger system uses custom-made electronics to determine the regions of interest (RoI) from the calorimeter and muon spectrometer coarse signals. The L1 trigger reduces the event rate from 40 MHz to 100 kHz with a latency of 2.5 μs. The HLT then runs trigger algorithms with near-offline reconstruction quality on either the RoIs or the full event information with an off-the-shelf CPU farm. This further reduces the event rate from 100 kHz to about 1000 Hz with an average latency of 0.3 s.

In Run 2, as the luminosity and pile-up increases, the rapid growth of the event sizes will push the load on the HLT because only a finite number of RoIs can be processed. Without selection using tracks, this results in a reduced efficiency or higher trigger thresholds for the objects to be considered. Global event information, such as the location of the hard interaction vertex or number of primary vertices in the event, is useful for object selections, corrections or background rejection. To provide track information to the HLT before full reconstruction, a hardware-based track finder (Fast TracKer) has been designed to run at the L1 rate. It will be partially implemented (central region only) in spring, 2016.

The Fast TracKer (FTK) [4] is a custom electronics system that rapidly finds and reconstructs tracks in the inner-detector layers for every event that passes the L1 trigger. It provides global track reconstruction so that the HLT has access to early tracking information. The track reconstruction is performed in hardware with massive parallelism of associative memories and FPGAs. Since tracks from FTK closely match to offline tracks, a pre-selection can be done before full track reconstruction. The performance has been studied with FTK tracks implemented in the trigger chains [4]; a large improvement can be seen on the ability to identify single particles, as well as on b-tagging and primary vertex finding efficiency.

II. The FTK to Level-2 Interface Card

A. Functionality

The FTK to Level-2 Interface Card (FLIC), shown in Figure 1, is the final component of the FTK system. It is a custom Advanced Telecommunications Computing Architecture (ATCA) card that interfaces the upstream FTK components with the HLT.

Each FLIC board receives the upstream event record from the eight optical links in the front panel. Each link receives data with a bandwidth of bandwidth is 2Gbps (tested up to 3Gbps). Because the FTK has its own coordinates for the hit clustering, local identifiers have to be converted to the coordinate system used by HLT algorithms. The two FLIC boards do the conversion using lookup tables, and insert the corresponding ATLAS global module identifier into the event record during data processing. The event record is reformatted to the ATLAS standard record format before it is sent out to the HLT.

The FLIC communicates with the multiple processor blades housed in the same ATCA shelf using the full backplane bandwidth. This enables event processing and monitoring by the multiple blades.

B. Data Processing, Control and Monitoring

The FLIC board is composed of the input card and the rear transition module (RTM). Two FLIC boards occupy the hub slots of an ATCA shelf, with processor blades in payload slots. This allows the full event record to be sent to any of the blades via 10 Gb Ethernet.

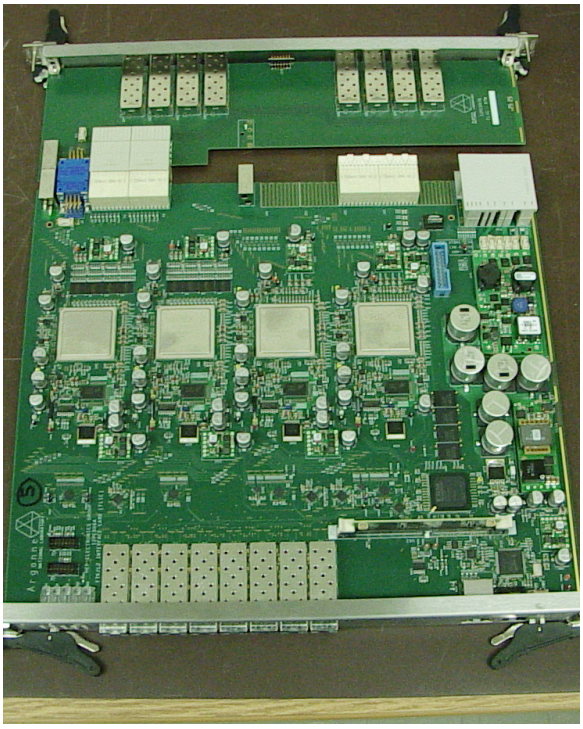

Fig. 1. The FLIC production board.

The input card is divided into two areas, the data processing area and the management area. In the data processing area, there are four Xilinx Virtex-6 FPGAs. Two are used to handle the data processing (processing FPGA) with the other two communicating with the processor blades over the ATCA backplane (interface FPGA). The four FPGAs are connected to each other via a full internal mesh of high speed low-voltage differential signaling (LVDS) lines (designed to run at 4 Gpbs) (Figure 2).

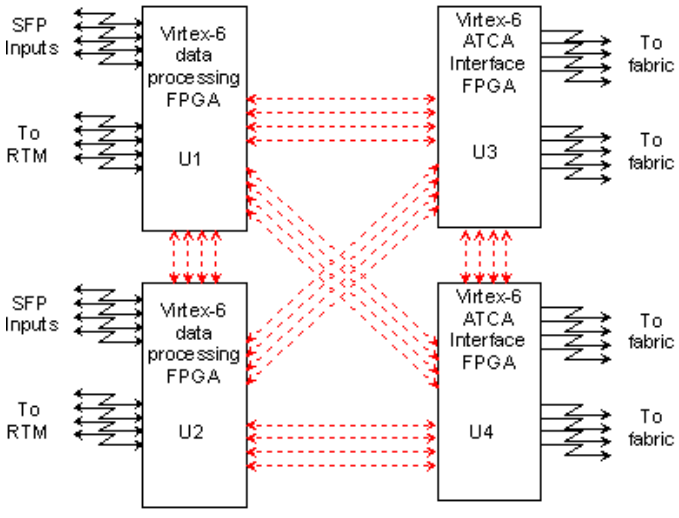

Fig. 2. Then internal mesh between the four FPGAs. Each FPGA is connected to another one using four high speed GTX lines.

The management area provides the slow control and monitoring of the FLIC board. It consists of one small Spartan-3 FPGA, one Microchip peripheral interface controller (PIC), four Flash RAMs and one Intelligent Platform Management Controller (IPMC) card made by LAPP [5] , shown in Figure 3). The small FPGA provides level translation and bus control logic to interface the microprocessor and Flash RAMs to the Virtex-6 FPGAs. When requested, it loads the firmware for each FPGA from the Flash RAM for configuration. Data for the SRAM fast lookup tables used by the Virtex-6 FPGAs is also stored in the Flash RAM. The PIC monitors voltage, current and temperature of the board directly using its internal Analog-to-digital converter (ADC). The PIC receives commands over the front panel Ethernet port, performing the required register and data accesses to all other devices by controlling the small FPGA. All transactions on the front panel Ethernet port are acknowledged. A secondary Inter-Integrated Circuit (I2C) interface connects the LAPP IPMC, a custom mezzanine card, to the PIC. Through this interface all monitoring information may be transferred through the IPMC to the shelf manager. Main board power is controlled in accordance with ATCA specifications by the IPMC. The power enable signal from the IPMC is sent to the PIC, which then re-drives the enable to the DC-DC converter. This allows the FLIC to be bench tested using a power supply.

Data processing in each processing FPGA is divided into four pipelines. Each pipeline processes data received from one small form-factor pluggable (SFP) on the front panel (Figure 4). The upstream data is buffered immediately after arrival, then pulled out by the receiver state machine. The internal processing uses a faster clock (3.2 Gbps for each pipeline) to insure that, ON AVERAGE, no more than one event's worth of data will be stacked in the FIFO. Each processing FPGA has 32 Mb of fast SRAM per input link performing the conversion of the module identifier (ID) from the FTK local ID to ATLAS global ID. The address for the lookup is built from the header of each track. The lookup is performed in parallel with the track processing, which ensures that the global ID is ready to be inserted to the track record before processing finishes. The global module ID is inserted into the event record on the fly in the merge state machine. Event records are then reformatted to the ATLAS standard record format, sent out from the RTM to the HLT. In total eight 2 Gbps S-LINK protocols are used for the RTM and readout card communication. A second version of firmware that emulates the output of the FTK system has been developed at Argonne to test the performance of the board as a function of the size of event records, event rate, and stability over time.

Monitoring of each pipeline is performed by the use of diagnostic counters and a multiplexed capture FIFO, all accessible by the PIC using register I/O as mentioned above. Each pipeline implements multiple counters showing the number of records and/or the number of fragments that have been processed. The multiplex capture FIFO may be used to capture data at multiple points along each pipeline, saving a copy of raw data as it passes through the pipeline. Both the counters and capture FIFO can be read using the front panel port. The spy buffer functionality has been implemented in the FLIC as well using the two interface FPGAs. They copy fragments of the selected event from the processor FPGAs using the internal mesh. Those fragment are then assembled, formed into

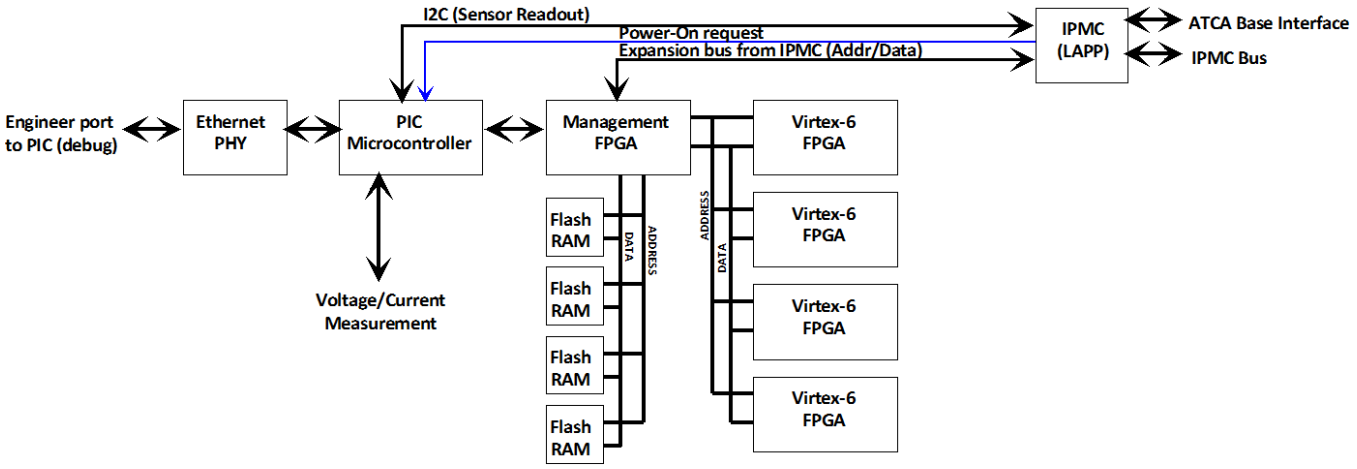

Fig. 3. Then slow control of the FLIC board.

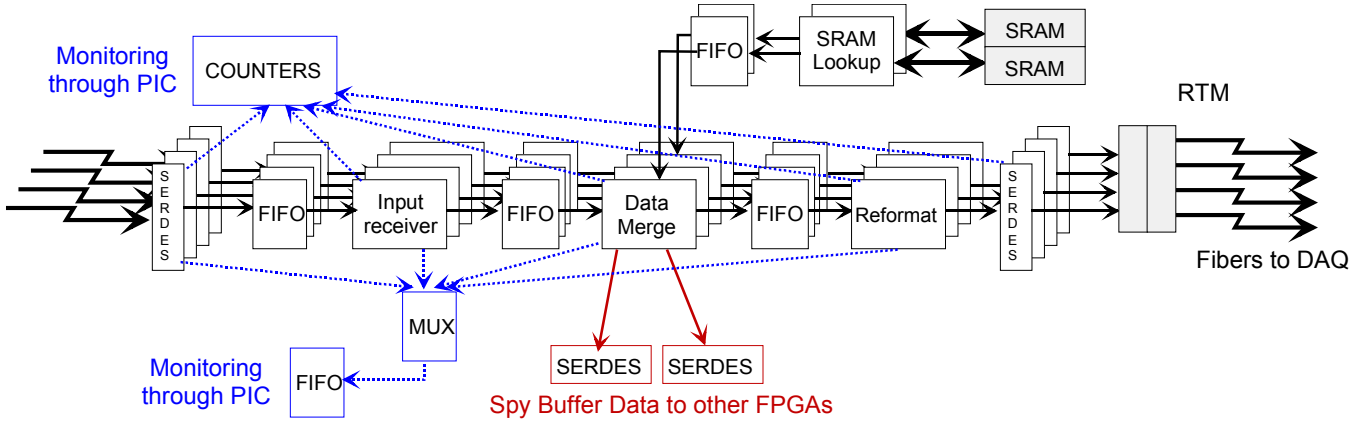

Fig. 4. The data processing pipeline in the processing FPGA.

Ethernet packets, and sent to multi-processor blades through the ATCA backplane. Analysis of these events by the blades in the shelf may then provide advanced monitoring or triggering options as appropriate software is developed.

C. *Performance study*

Two prototype FLIC boards have been tested for all requirements and demonstrated to perform at or above design specification. For the data processing inside the FLIC, the Chipscope measurements show the SRAM lookup takes a maximum of 139 ns to resolve for all detector layers, while processing of each track takes 160 ns. The latency has been measured as a function of the number of tracks per event (Figure 5). Good agreement can be seen between measurement and theoretical model predictions (the time taken to write the event record into the various FLIC FIFOs as the data expands within the board). In the specification, the Run 2 event record contains an average of 17 tracks, which corresponds to a latency of about 20 μs. The event rate from the FLIC to the HLT has also been studied. Figure 6 shows the measured event rate as a function of the number of tracks per event record. For an event with 17 tracks, the rate is about 120 kHz, above the 100 kHz HLT requirement. As all pipelines are independent, the rate per pipeline does not change when processing multiple

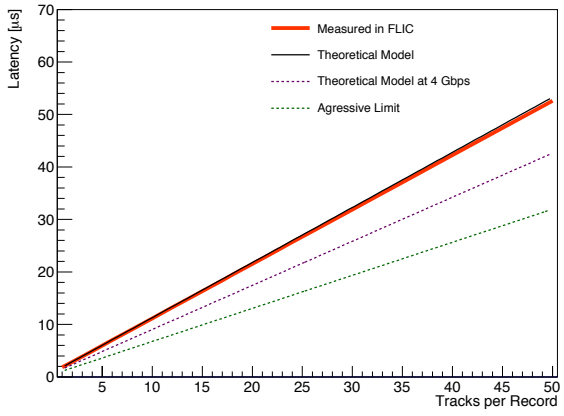

Fig. 5. Latency of the FLIC data processing as a function of the number of tracks per event record. The red line is the rate that FLIC sends event records. The black line is calculated based on the theoretical model. The rate for a 4 Gbps output link (purple dashed line) and aggressive limit (using full bandwidth, green dashed line) are also shown.

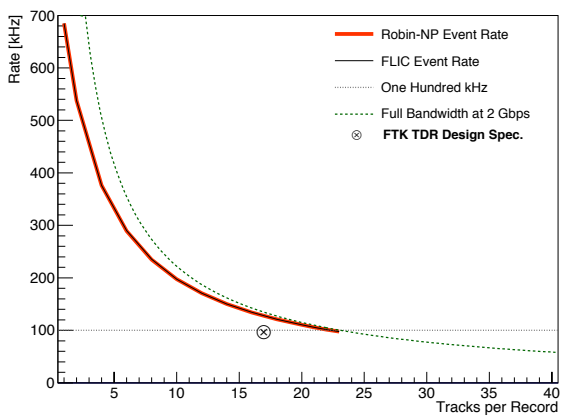

Fig. 6. The FLIC to HLT event sending rate as a function of the number of tracks per event record. The black line shows the event record rate of FLIC sending date while the red line is the receiving rate on the HLT side. The green dashed line shows the maximum rate when using the full 2 Gbps bandwidth. The cross shows the FTK specification which is 100 kHz of 17 tracks per event record.

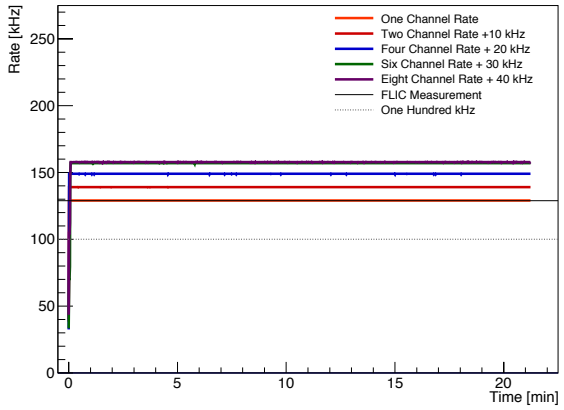

Fig. 7. The rate at which the FLIC sends events to the HLT is measured with a fixed number of tracks per event record in each output channel. Measurements have been performed using one (orange line), two (red line), four (blue line), six (green line), and eight (purple line) output channels. The measured rate using multiple output channels have been shifted up for better visibility. The rate limit in the specification is 100 kHz (dashed line).

channels (Figure 7).

III. Summary

The FLIC is an interface between the FTK and the High Level Trigger built with all necessary and desired functionality. It does the data dispatching to HLT with geometry description conversion, as well as the data monitoring and processing on ACTA blades. It has been extensively tested, meets or exceeds all the specifications.

References

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