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THE SPS TIMING SYSTEM PROPOSAL

by

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ABSTRACT

This note describes the principles and design criteria of the timing system for the SPS. This includes the control philosophy and the command structure of the timing modules. The global timing transmission is discussed and the local interaction required at each auxiliary building is outlined. Also the distribution of these signals in the auxiliary buildings via means of the General Purpose Multiplexer is explained. Finally detailed specification of the timing modules plus full operating instructions are included. The user modules concerned are the general purpose timing modules TIMING TG1 and TIMING TG2, the manual module TIMING TM, the fan-out module TIMING TF and the visual display test module TIMING TD.

Only the global timing signals ie. Event Train and Clock Train are described in this paper, other timing signals such as the 44kHz Revolution Frequency will be generated and distributed locally.

The SPS Timing System Proposal

1. INTRODUCTION

The correct operation of the SPS is absolutely dependent, amongst other parameters, upon an accurate and reliable timing system. This proposal describes such a system.

The environment of the SPS, in particular its physical size and its required mode of operation, greatly influenced the design criteria of the timing system. The versatility of the SPS dictates that the timing system itself must be extremely flexible. This flexibility is achieved at the generation end by using a computer to provide the cycle information for the Master Timing Generator unit (MTG). At the user end the flexibility is provided by distributing the timing signals through the General Purpose Multiplexer (GP.MPX) system. The timing repeatability precision is not affected by the various lengths of the GP.MPX Bus.

2. PS - SPS DIALOGUE

In order for correct beam injection to occur the timing system of the SPS must be synchronised to that of the PS. The dialogue between the two machines is of the master - slave relationship where the PS is the master. Under no circumstances whatsoever can the SPS delay the programmed cycle of the PS. If, for any reason, the SPS is not ready to accept injection it must miss that injection period and wait for another Injection Prepulse response from the PS. (Fig.1a)

The SPS generates a 'Beam Required' signal which is transmitted to the PS. This signal informs the PS that the SPS is ready for injection. The PS interrogates this line twice during the injection sequence, the first test occuring approximately one second before ejection. This is the Linac test and if the line was inactive at that time the Linac pulse will be dumped at the output of the Linac and the injection sequence terminates, but if the line was active it is interrogated again 3.6 mSec. before ejection. This is the Booster-PS test and if the SPS was unable to continue the injection sequence the beam will

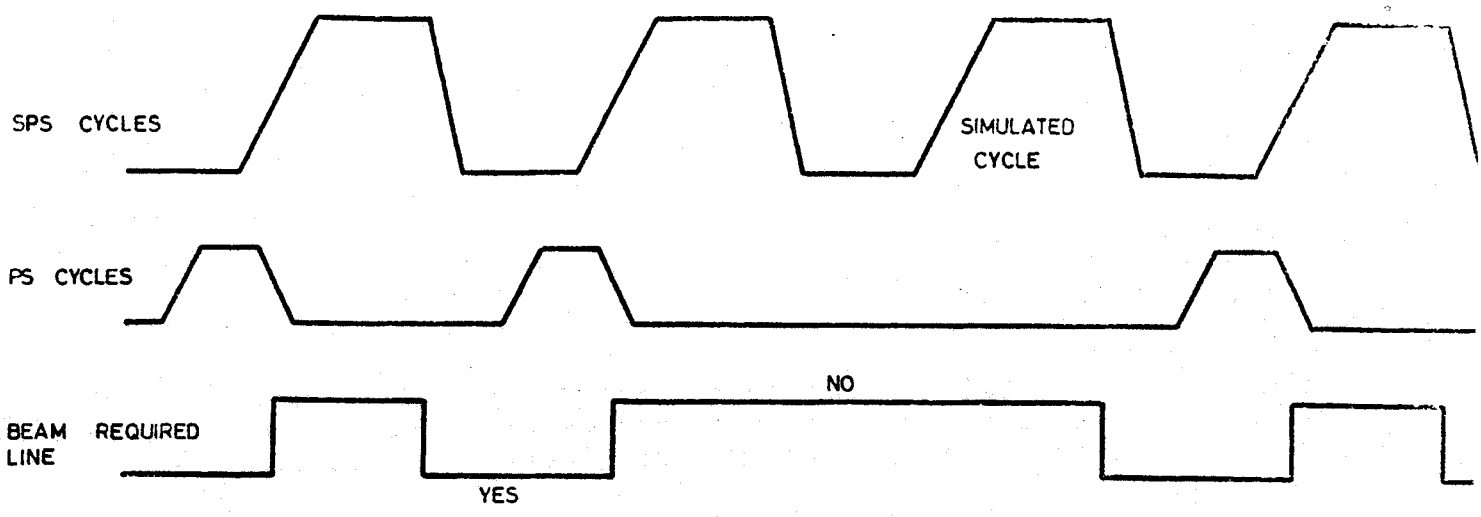


FIG. 1a

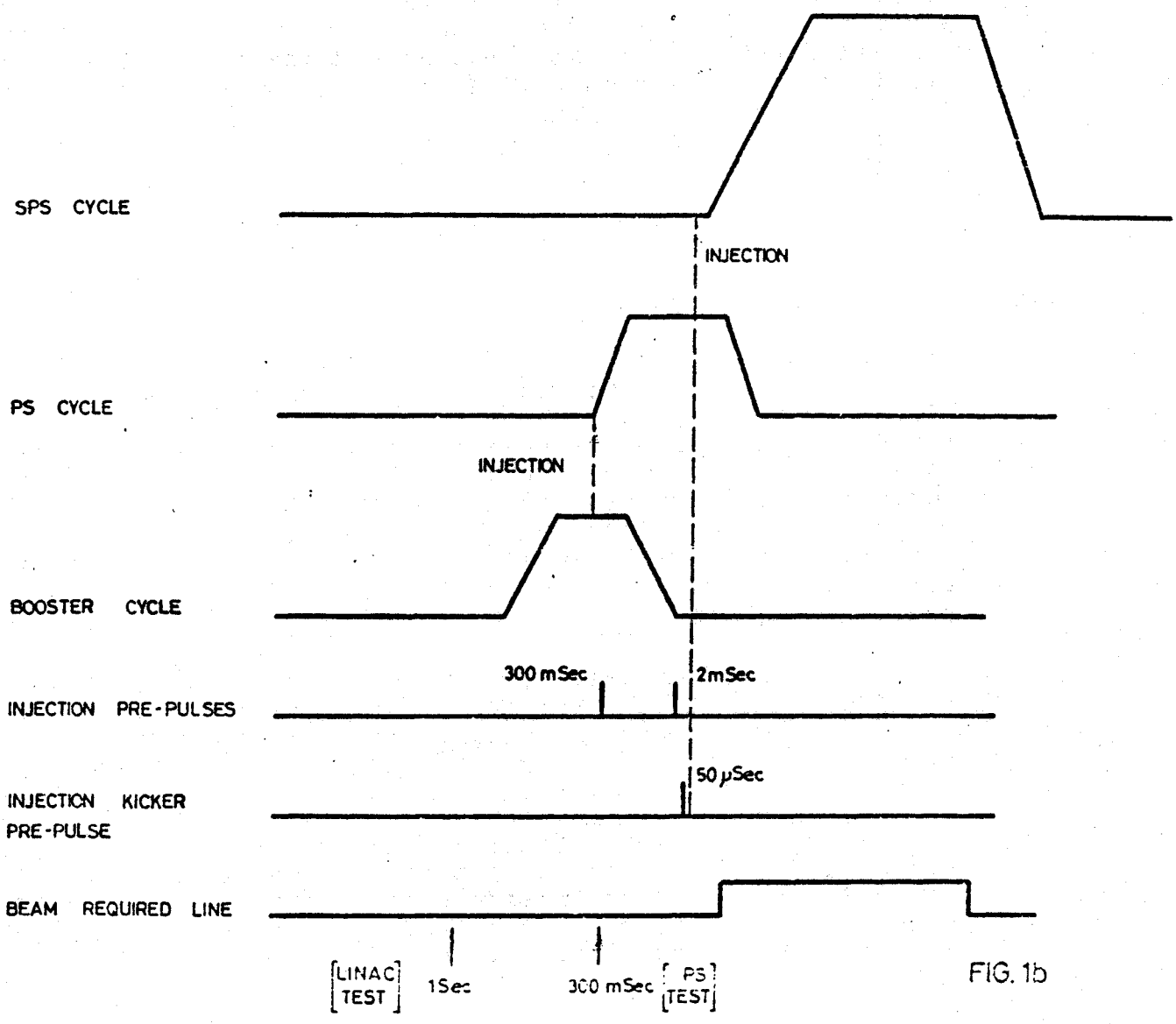


FIG. 1b

FIG.1 PS-SPS DIALOGUE

be dumped in the PS at the lowest energy possible. If the test was successful the PS commences its acceleration cycle to SPS injection level at 1Ø GeV.

Besides interrogating the Beam Required line from the SPS the PS also transmits three injection pre-pulses to the SPS. The first pulse occurs just before the PS acceleration cycle approximately 3ØØ mSec prior to ejection. A second pulse is transmitted to the SPS informing it that beam was successfully de-bunched during the acceleration cycle and that ejection from the PS will definitely occur 2 mSec. + or- 2uSec. later. This pulse is used to generate the Reset signal in the SPS. Finally the Injection Kicker Pre-pulse is transmitted 5Ø uSec before injection. [Ref.1]

3. THE GENERAL SPS TIMING PHILOSOPHY

The basic time unit for the SPS is 1mSec. This time information is transmitted to the user by the Clock Train which consists of a series of pulses at 1mSec. intervals with a repeatability accuracy of + or - 1uS. The clock is referenced to the injection kicker pre-pulse at the start of each cycle. (Fig.2a) Under normal operating conditions all timing operations will be referenced to this clock.

In conjunction with the 1mSec clock a coded Event Train is also transmitted. [Ref.2] This code uniquely identifies specific operations during a cycle, eg. start of front porch, slow extraction, dump etc. When a timing module receives and recognises a valid Event Code it waits for the next clock pulse which it interprets as the Event Marker Pulse. The instant at which the events actually start will be coincident with the appropriate clock pulse. (Fig.2b) This guarantees a repeatability accuracy of + or - 1uS for each event. The Event Code can be programmed by the Master Timing Generator to occur during any 1mSec time interval. (Fig.2c)

The most significant binary bit of each event code is the Simulated Cycle bit. The MTG sets this bit to a logic '1' if the SPS cycle is being simulated, ie. no

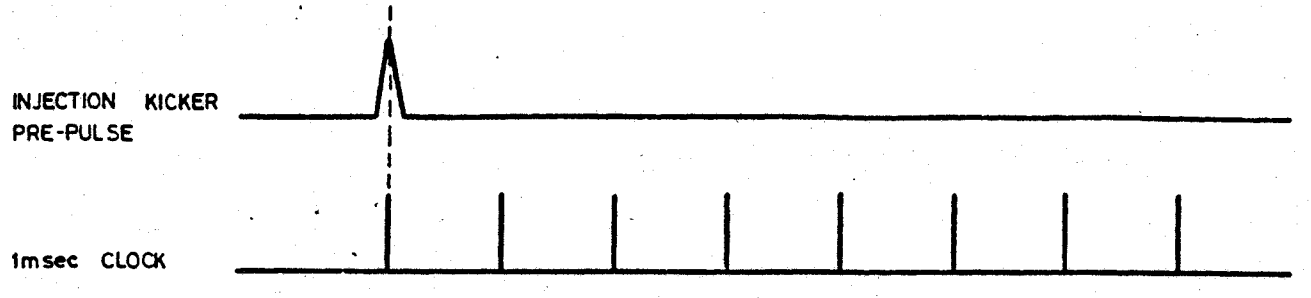


FIG. 2a

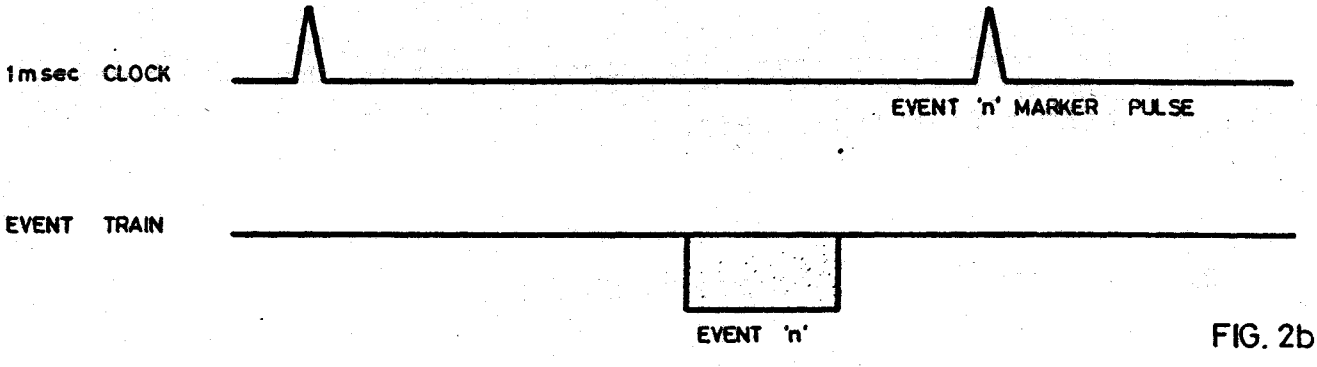


FIG. 2b

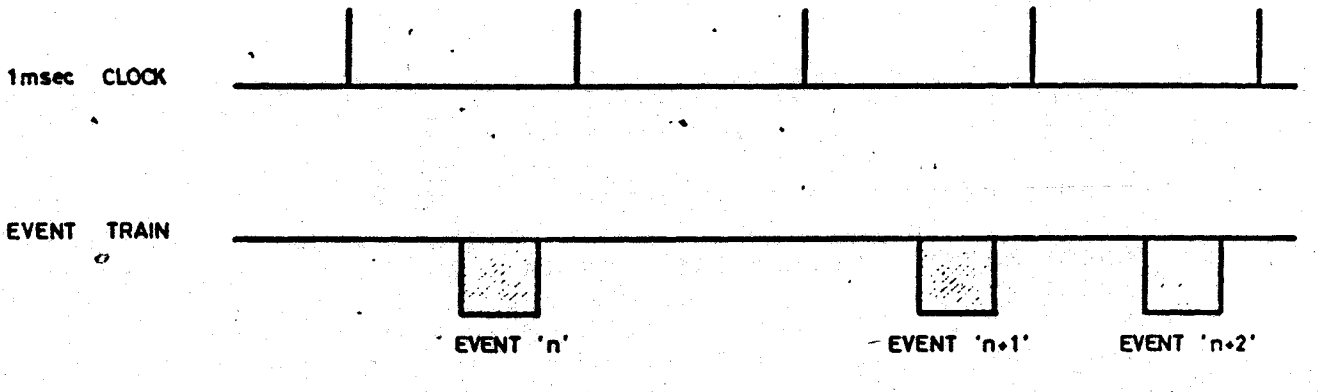
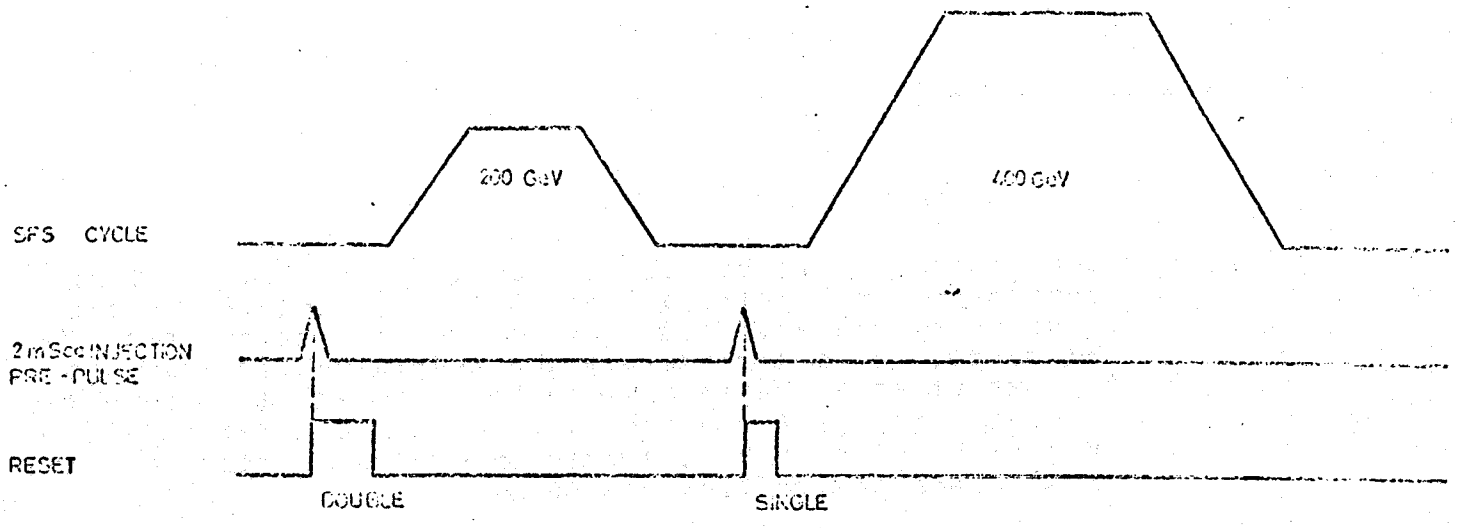


FIG. 2c

FIG. 2 GENERAL TIMING WAVEFORMS



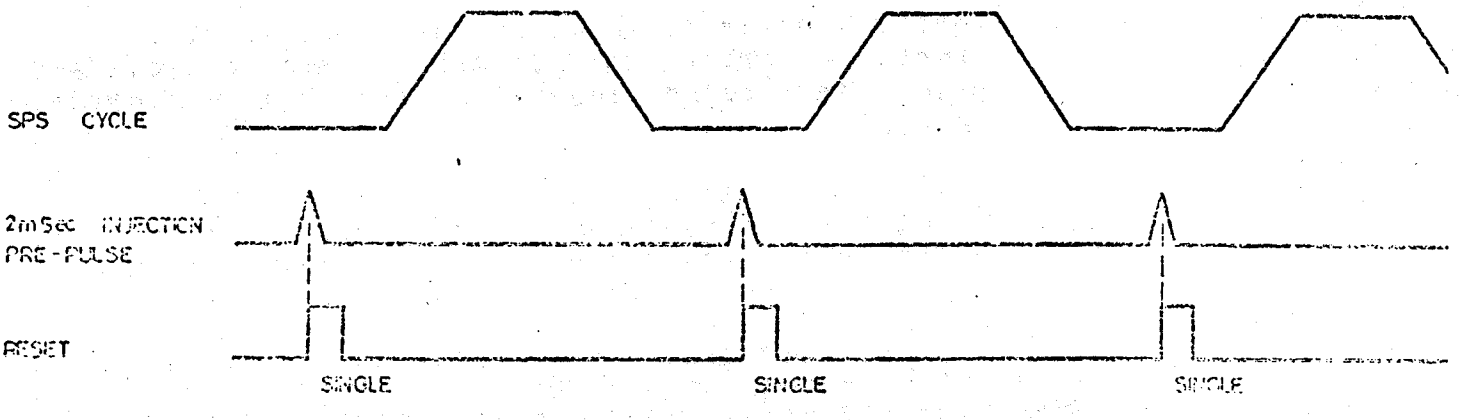


FIG. 2

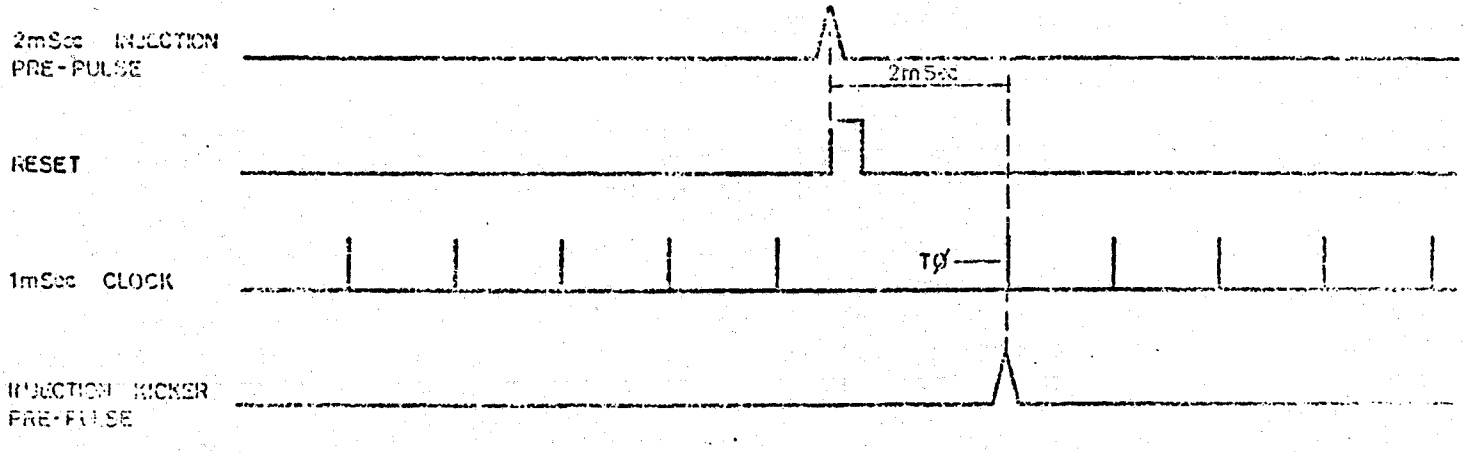


FIG.

FIG. 2 GENERAL TIMING WAVEFORMS (cont.)

beam present. This bit is tested in the GP.MPX Timing Connection Unit (Fig.6) where a flag is set if the cycle is being simulated. This flag may be used to generate an interrupt, or alternatively the General Purpose Computer may use it as a status bit. In both cases the computer receives the information through CAMAC. The connection unit will normally be situated in the same rack as the CAMAC crate controlling the GP.MPX.

To enable users to initialize their equipment for each cycle a reset pulse is transmitted 2mS prior to injection. Two types of reset signals will be generated.

a) Double - prior to injection of double cycle.
b) Single - prior to injection of single cycle and prior to second injection of double cycle. (Fig.2d)

Both the resets halt the 1mSec clock which remains disabled until the injection kicker pre-pulse occurs, consequently the first clock pulse after a reset will always be at time zero (T0) (Fig.2e)

The four signals, 1mSec Clock, Event Code, Reset single and Reset double are the only ones to be transmitted globally. Other signals, such as the 44kHz Revolution Frequency, are only of interest to certain specialized users therefore they will be generated and distributed locally.

4. GLOBAL TIMING DISTRIBUTION

The MTG situated in the Control Building must transmit the timing signals to each auxiliary building. The transmission may be accomplished as a 'star' connected system or as a global series connection. (Fig.3) Although previous timing systems eg. PS. ZNPL [Ref.3] tended to utilise the 'star' approach as it was generally simpler to implement and afforded more user isolation the SPS will use the global transmission system. This is because for large accelerators, such as the SPS or NAL, [Ref.4] the cost of the extra terminated cables that are required becomes significant. Furthermore

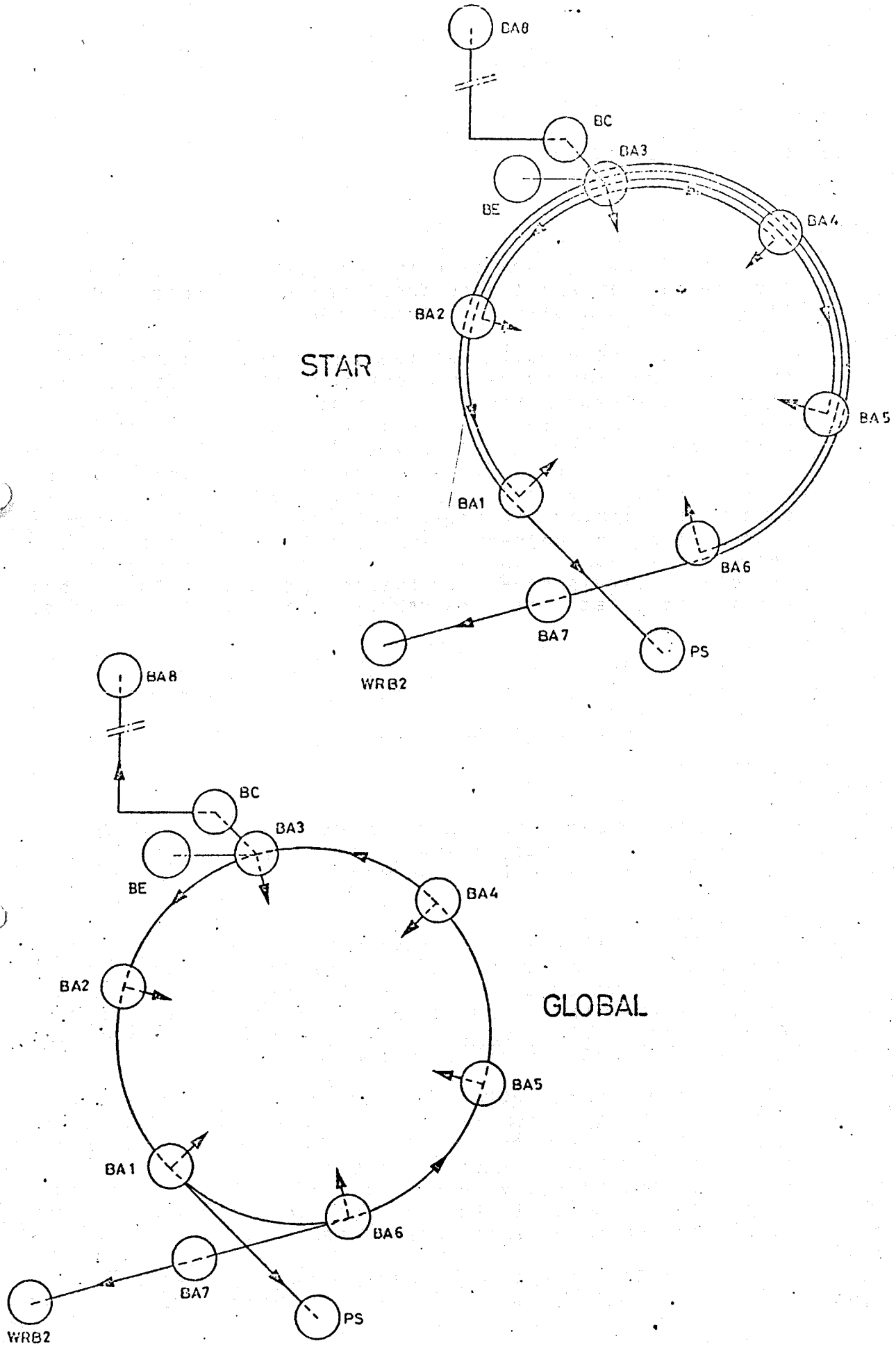


FIG. 3 INTER-BUILDING CONNECTIONS

for the MTG to perform on-line data validation checks on the star system additional circuitry and cabling would be required at each user end of the star.

Also the global distribution system requires only one cable passing round the periphery of the accelerator. At each auxiliary building the timing signals are 'tapped off' the main cable and connected to the GP.MPX by means of the repeater units. (Fig.4) It is extremely important that good isolation exists between the user and the main timing cable in order to prevent the user from corrupting downstream timing information. There must be good common mode isolation between each auxiliary building and between signals generated and transmitted in those buildings. Transformer isolation is ideal for both applications as the transformer acts as a band-pass filter.

As both the origin and the final destination of the global signals is the MTG itself it is a relatively simple exercise to include logic for checking the transmitted information. Two modes of checking are available:-

1) Digital

The number of bits transmitted is compared with the number of bits received. This can be achieved by a simple up/down counter in the MTG.

2) Time

The total inherent propogation time for the global transmission, including the transmission time from the head of the access shaft to the repeater units in each auxiliary building, is 42.5uSec which must be constant within + or- 1.0 uSec. (Fig.5a) This can be checked by standard time of flight techniques.

Both modes will be essential during the system installation and commissioning stages as diagnostic tools. During run time mode 2) could be included in the pre-check procedure prior to injection acceptance, whilst 1) will be extremely useful as a monitor of the overall system performance. It is not intended that this mode will function on an interactive basis during a cycle.

Fig.5a clearly indicates that whilst the beam travels in a clockwise direction the timing signals are

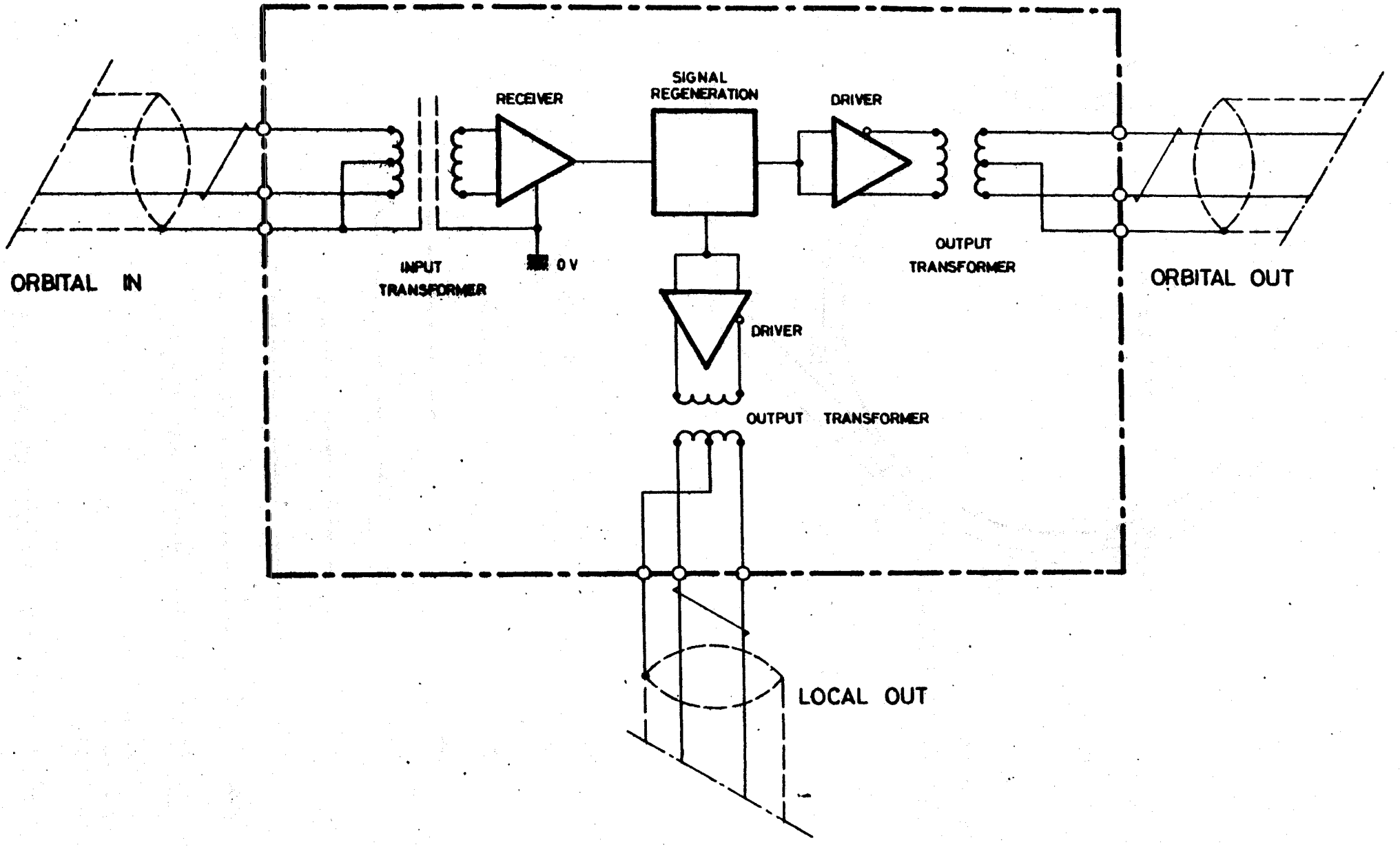


FIG.4 REPEATER UNIT

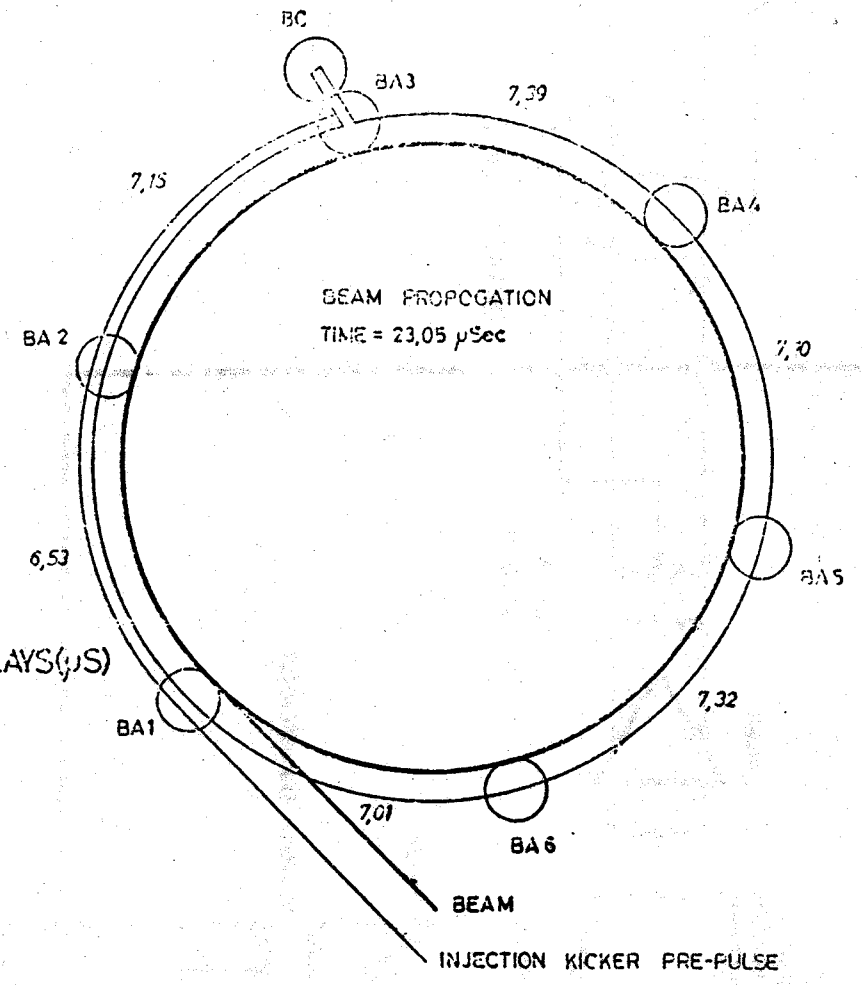


FIG. 5a TIMING SIGNAL PROPOGATION DELAYS(μS)

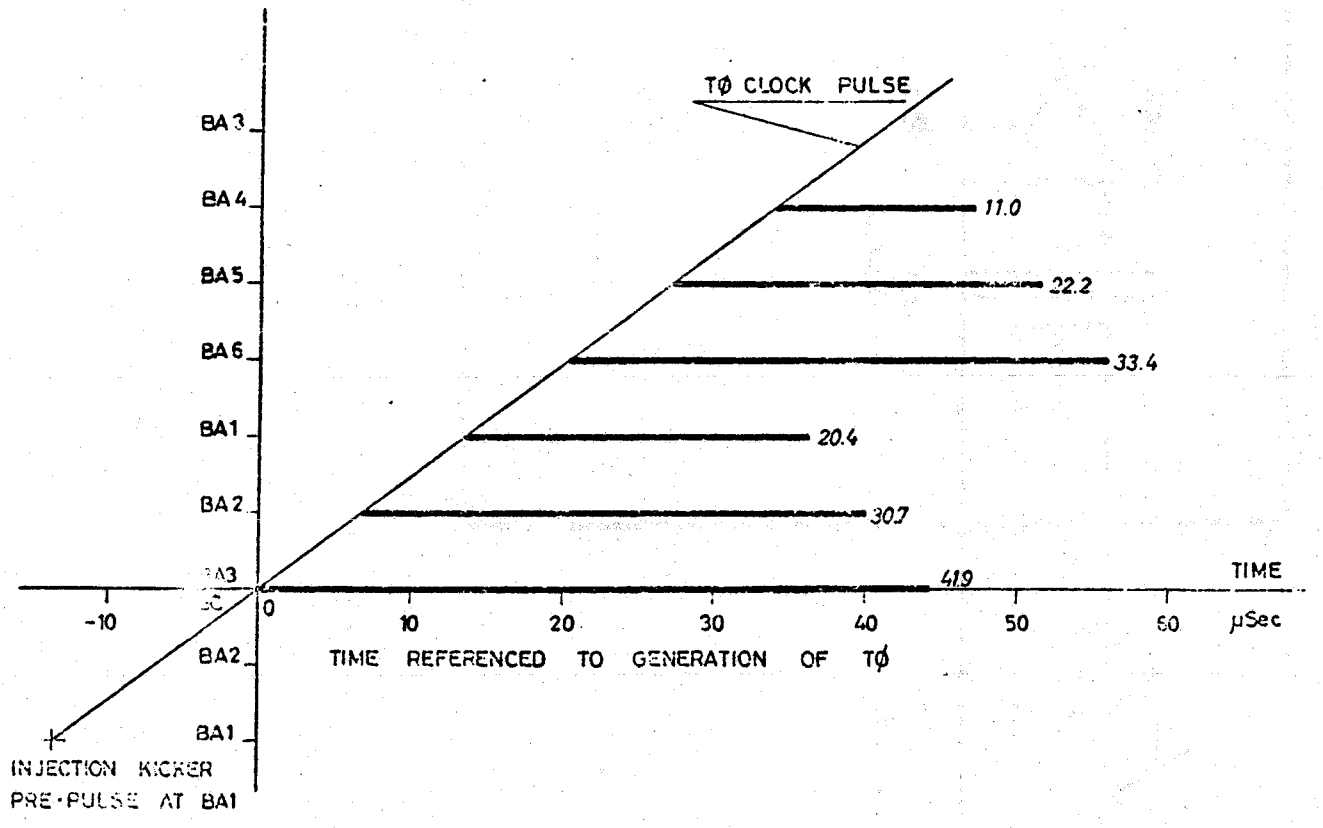


FIG. 5b CHART INDICATING ARRIVAL OF BEAM (μSec) REFERENCED TO TØ AT EACH AUXILIARY BUILDING

transmitted from the control buildings in an anti-clockwise direction. This approach provides the users with the maximum possible warning time between T0 and the arrival of the beam at each super-period. It can be seen from the chart (Fig.5b) that this time varies from 41.9 uSec at BA3 to 11.6uSec at BA4. If the signals were transmitted in a clockwise direction there would be a minimum warning time of only 2.5uSec at BA2.

5. LOCAL TIMING DISTRIBUTION

The timing signals are distributed throughout the auxiliary buildings by means of the GP.MPX. (Fig.6) The overall concept of the GP.MPX makes it ideally suited for this task. [Ref 5]

In each MPX Station Crate the Tete de Station unit receives the di-phase timing signals from the MPX bus and translates them to binary code. These signals, at TTL levels, are then transmitted onto the Station Crate Dataway. (Fig.7) The signals are listed in Table 1. The 1mSec clock and the Reset signals are taken to the front panel of the Timing Tete de Station module where they are connected to Lemo connectors through buffer isolators. User timing modules will be inserted into the Station crates where they receive the global timing information via the dataway. Note that the translation from di-phase to binary performed by the Tete de Station simplifies the logic necessary in each user timing module.

All timing modules will have blue anodised front panels in order to provide an obvious means of identification when inserted amongst the GP.MPX modules.

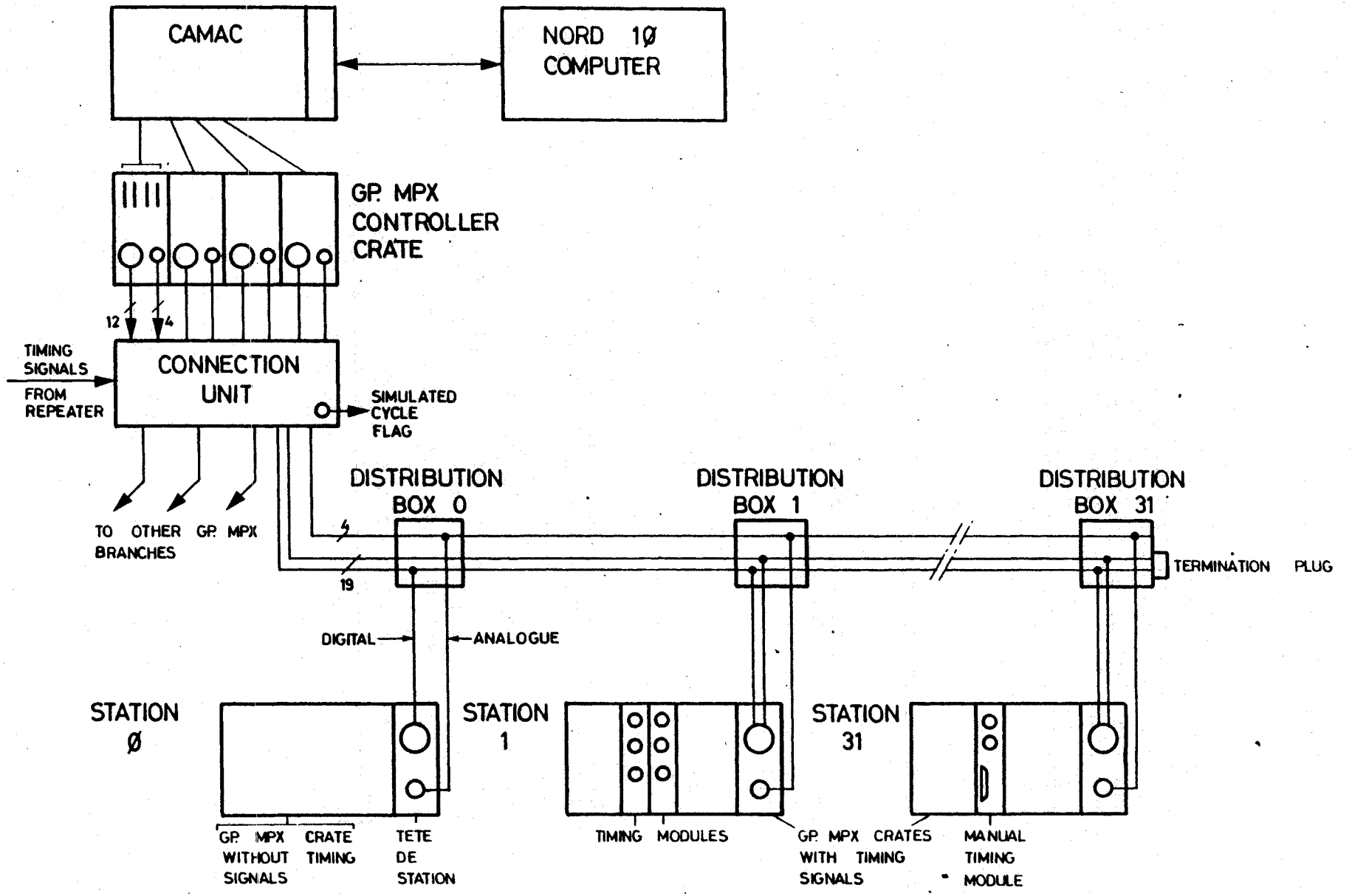


FIG. 6 TIMING DISTRIBUTION THROUGH THE GP. MPX

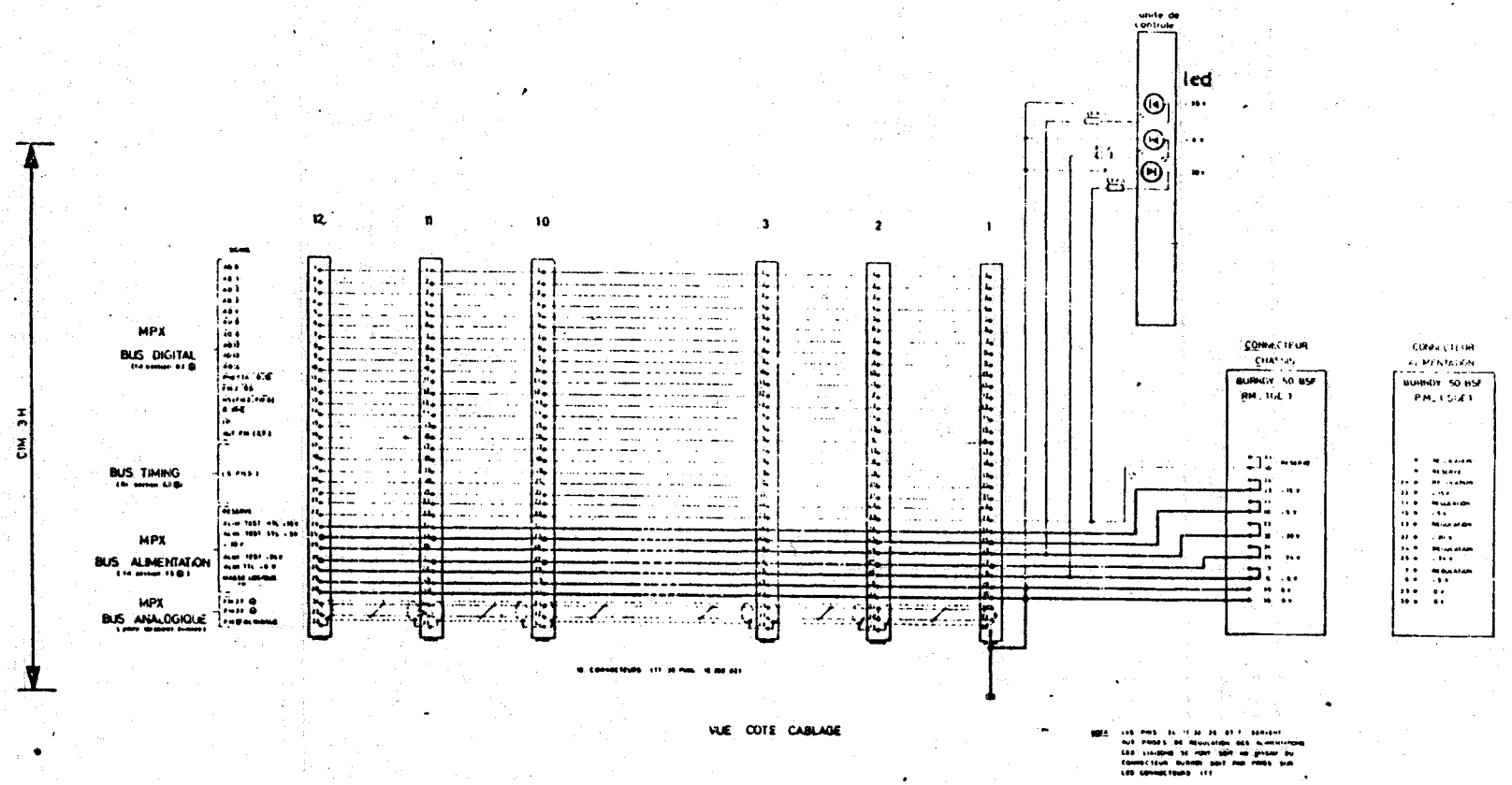


FIG. 7 GP. MPX DATAWAY

TABLE 1.

DATAWAY PIN NO	SIGNAL IDENTIFICATION	GENERAL COMMENTS
17	1mSec CLOCK	All the signals
		on pins 17 > 22
18	BINARY EVENT CODE	inclusive are
		TTL compatible.
19	EVENT CODE CLOCK	
20	RESET	SINGLE 20uS
		DOUBLE 40uS
21	INTER-	Balanced
	MODULE	Line driver
22	LINK	signal.

6. SIGNAL STANDARDS

a) Global

The global signals are transmitted on one pod of a standard six pod video cable. The audio twisted pair of the pod is used to transmit the Event Train whilst the larger diameter video pair transmits the Clock Train plus the Reset signals. All global signals are transmitted as a Manchester di-phase code. This code, coupled with the characteristics of the repeater units, provides good noise immunity. The amplitude of the signals are + and - 5 volts.

b) Local

In this context local is defined as the transmission medium between the local outputs of the repeater units and the input to the Tete de Station unit in the GP.MPX crate. The two twisted pairs required for the timing signals are contained in the main GP.MPX bus cable. (Fig.6) Again the Manchester di-phase code is used but the signal levels are at 0 and + 5 volts. This is

to make it compatible with the standard power supply of the GP.MPX and also to reduce the possibility of crosstalk from the timing signals onto the multiplexer data lines.

c) User

Three types of outputs are provided:

1..For connecting to users external equipment.
Blocking oscillator levels

Timing signals for driving the users external equipment will be generated by a blocking oscillator circuit. The circuit will provide a transformer isolated positive pulse of 25 volts amplitude into a 50 load. The pulse width will be 2uSec with a rising edge of less than 50nSec.

2..For connecting to users CAMAC equipment.
TTL levels

Negative logic TTL levels are used compatible with the CAMAC unterminated signal standards. Each output will be capable of driving a minimum of 32 TTL loads. OP1 and OP2 signals are time-stretched by monostables to 1uSec to make them compatible with all CAMAC interrupt registers. This enables the user to generate an interrupt during any selected part of the SPS cycle.

3..For connecting to users equipment situated in the same GP.MPX crate.
Balanced line driver levels.

This signal is generated by the general timing module TIMING TG2 (see module description for full details). It is intended for users who have a number of modules which require a common timing pulse. The timing module generating the signal and the user modules receiving the signal must all be in the same GP.MPX crate. The 2uSec wide signal is transformer isolated in the timing module and all receiving devices must utilize the National Semiconductor balanced line receiver type DM 8820A preferably with transformer isolation.

The SPS Timing System Proposal

TIMING MODULES

Five different types of modules are described in detail. The two general timing modules, TIMING TG1 and TIMING TG2, will normally be used by the users for generating the majority of their timing signals. The manual timing module TIMING TM enables the users to change their timing parameters manually. Normally these can only be changed by the computer operating system. The fan-out module TIMING TF accepts either a blocking oscillator or TTL level input and generates five completely isolated blocking oscillator type outputs. Finally the display module TIMING TD is a test module which, when connected to either the general or manual timing modules, visually indicates the programmed parameters of that module.

The two general purpose timing modules are both able to generate two blocking oscillator type output pulses. The outputs of TIMING TG1 are of the format:

Output A = En + x
Output B = En + y

where En is the selected event and x and y are the respective delays, in milliseconds, between the event and the two output pulses.

Module TIMING TG2 has the format:

Output 1 = En + n
Output 2 = En + n + m

where En is either the selected event or the external start, n is the delay between En and Output 1 and m is the delay between Output 1 and Output 2. Both the delays can be in either millisecond or external clock units.

The main difference between the general modules is the trigger point for the second counter. For TIMING TG2 and TIMING TM this point occurs at the completion of the first delay counter whilst the counters of TIMING TG1 are both triggered when the selected event has been detected. Also a number of integrated circuits and front panel connectors have been omitted from TIMING TG1 to reduce cost. (see module descriptions for full details)

The SPS Timing System Proposal

The general timing modules incorporate all the features originally proposed for the Type A, Type B and Type C timing modules. [Ref.6] TIMING TG2 contains the combined features of the original type B and C whilst TIMING TG1 is effectively a dual Type A module but with both outputs referenced to the same event. This approach was adopted after studing the replies to the Memorandum [Ref.6] and also from subsequent informal discussions with the users.

The same type of printed circuit board is used for the manufacture of both the general timing modules and also the manual timing module. This board enables many module configurations to be realised. For example a user may require a single output pulse similar to TIMING TG1 but referenced to his external clock. Whilst TIMING TG2 can satisfy these requirements, it may be economically viable to manufacture a different timing module utilizing the same printed circuit board but with a different front panel. The economics will depend largely upon user demand.

Another possibility is a multiple output pulse module similar to TIMING TG1 but with four or even eight outputs. The delays to be independant of each other but all referenced to the same Event Code Marker Pulse. This can be accomplished by simply adding a second printed circuit board to the module. Again manufacture of such a module will depend upon user response bearing in mind that the same operation can be performed by a number of TIMING TG1 modules.

The provisional front panel layouts of the timing modules are included to provide the user with a visual indication of what the proposed modules will look like. (Fig.A1)

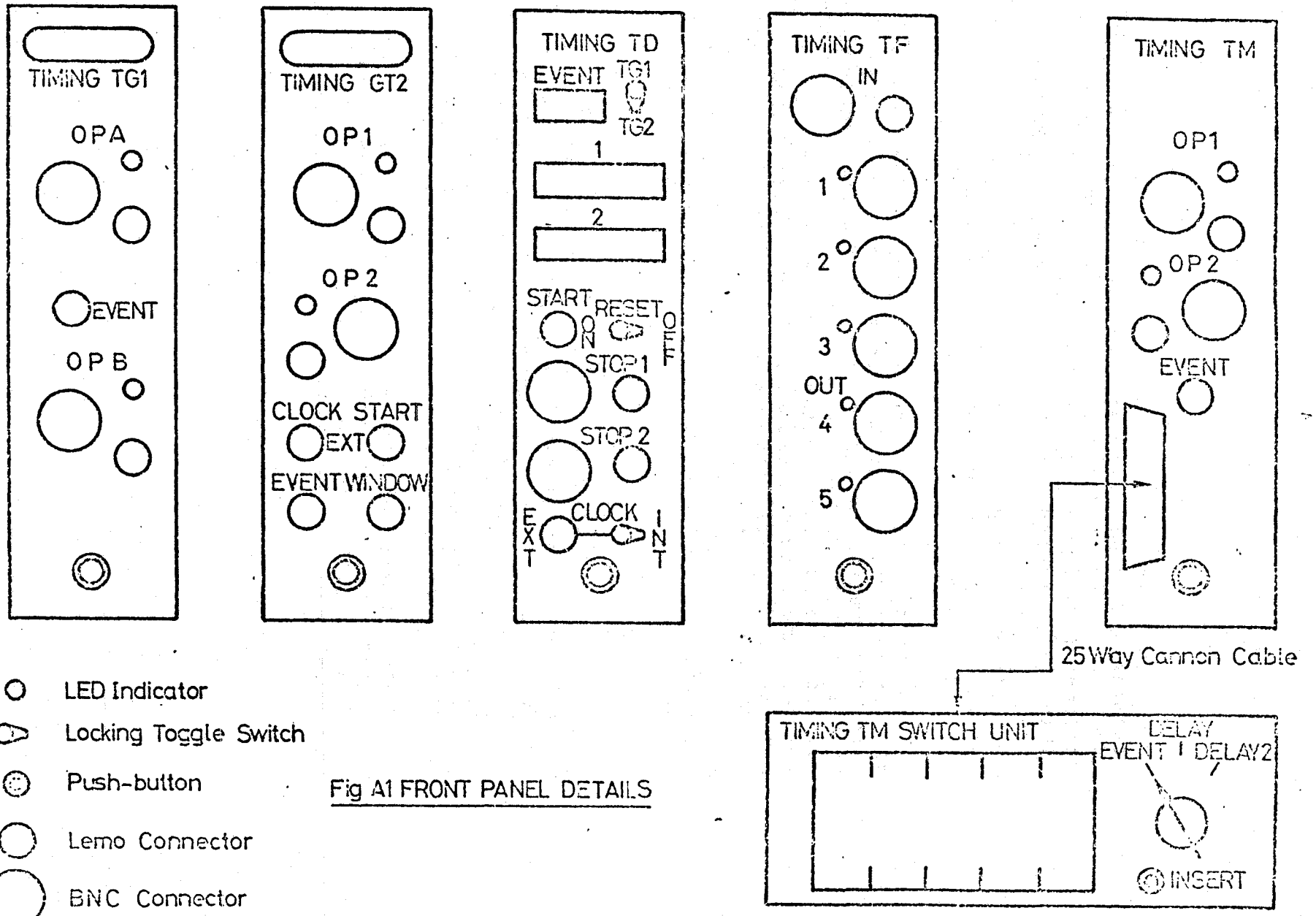


Fig A1 FRONT PANEL DETAILS

REFERENCES

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2 Proposals for the Timing System for the SPS. - M.C. Crowley Milling LAB 2 CO-66 MCCM-73.33

3 The Timing Pulse Generator and Simulator - L.R. Johnstone J.Meadows DNPL MCR-2119

4 PRIMATE: A Versatile Accelerator Timing System - C.A. Swoboda et al. NAL.

5 General Purpose Digital and Analogue Multiplexer for the SPS Computer Control System - R. Rausch J.M. Sainson R. Wilhelm LAB 2 CO-73.2

6 Memorandum: Timing System for the SPS - M.C.Crowley Milling LAB 2-CO MCCM nm

GENERAL TIMING MODULE - TIMING TG1

INTRODUCTION.

This is a simple general purpose timing module which can be programmed by the local general purpose computers to generate either one or two timing pulses per cycle. The pulses can be varied independently of each other but both are referenced to the same event and occur a given number of milliseconds after that event. The single width 3U unit can be plugged into any location of a standard GP.MPX crate.

The three operating parameters, Control + Event word, Delay A and Delay B, are loaded from from the local computers into the timing module by means of the GP.MPX system. Likewise the global timing signals, Reset, 1mSec Clock and Event Train are also connected through the GP.MPX Dataway. Individual user signals viz, Output Pulse A, are connected by means of front panel BNC connectors. User TTL signals to other timing modules and monitor points are connected to Lemo connectors.

A block diagram of the module is shown in Fig 8

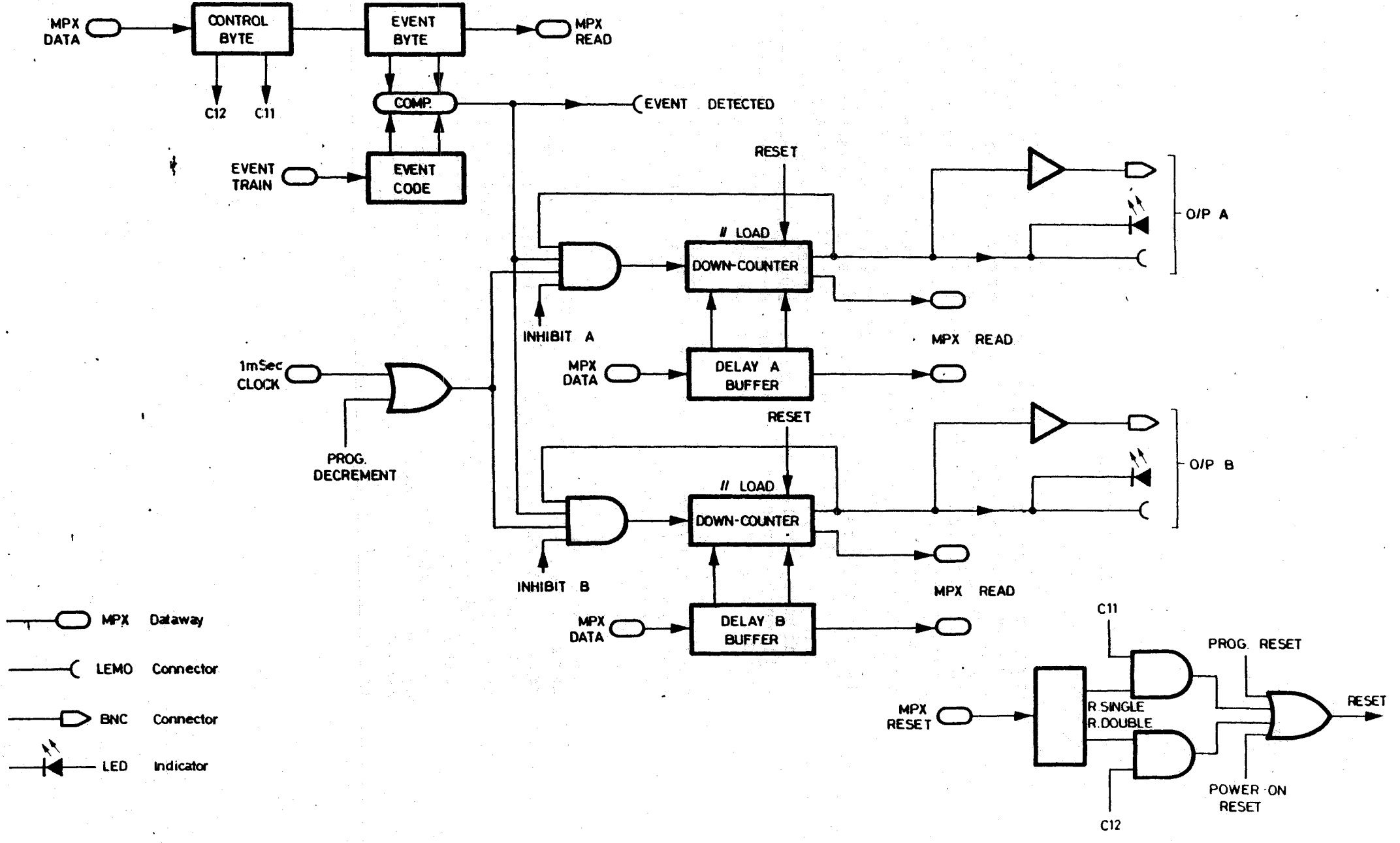

FIG. 8 BLOCK DIAGRAM OF MODULE TIMING G1

PRINCIPLES OF OPERATION

The Control + Event Word and the Delay A Buffer must be pre-loaded with the operating parameters to enable the module to function correctly. The two counters are the preset, count down to zero type each permitting one operation per SPS cycle. A double cycle may effectively be considered as two single cycles. If a particular operation, eg. Beam Dump, has the same Event Code for both cycles then the module can be programmed to operate on either or both of the cycles by means of the two reset bits, C11 and C12. This is possible because once an output has been triggered the associated counter remains disabled until reset occurs. If each operation of a double cycle has a unique Event Code then the module will only operate once per double cycle unless the parameters are changed before the second cycle commences.

The contents of the Control Byte determine the mode of operation of the unit. The various modes are explained in the GP.MPX COMMANDS section. This section also contains the Multiplexer Function (FM) plus the sub-address (A) for each operation. The read functions (FM6) are provided primarily as a module commisioning and debugging aid although obviously they can be used for data validation purposes but only if the user considers this feature absolutely essential.The standard software packages will not normally read back this data. This facility must not be used during an SPS cycle as a time clash may occur with the timing signals which could prevent an Event from being recognised. This is due to the fact that data is transfered serially and in order to prevent an erroneous comparison during this shift operation the comparator is disabled whenever the module is addressed by the computer.

TIMING TG1

TIMING TG1 FEATURES

2 Digital Inputs from the computer via the CP.MPX Bus
1) Event Byte + Control Byte

2) Delay, in 1mSec clock units, between event Rn. and the first output pulse.

4 Inputs
1) 1mSec Clock
2) Event Train
3) Event Train Clock
4) Reset Single + Reset Double

!--MPX Dataway

2 User Blocking Oscillator outputs
1) Output Pulse A
2) Output Pulse B

!--Front Panel BNC

3 User TTL outputs
1) Output A
2) Output B
3) Event Detected

!--Front Panel Lemo

2 Led.Indicators
1) Output A

2) Output B

Output pulses A and B can be altered independently of each other but both are referenced to the same Event code. Also both circuits are affected by the common control bits and reset signals. (Fig.9)

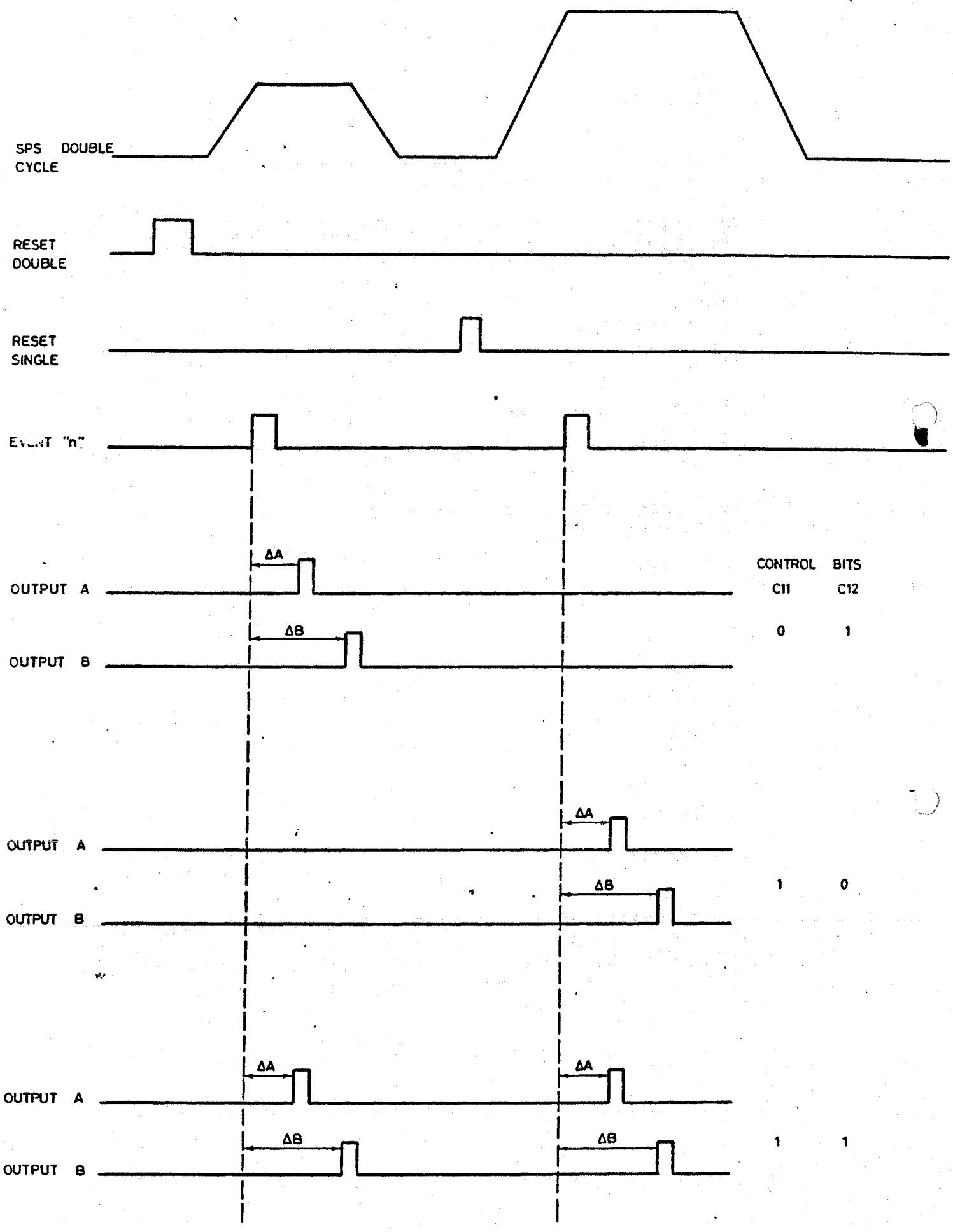

FIG. 9 OPERATING MODES OF TIMING G1

TIMING TG1

CP.MPX COMMANDS

1) Load Control + Event Word FM2 A0

Bits 0>5
Six bit Event Code allowing for up to sixty three different events per cycle.

Bits 6>7
Must be at logic '0'.

Bits 8>10
Reserved Control bits.

Bit 11
Reset prior to start of a single cycle.
The two preset counters are loaded with the count value from their associated delay buffers prior to the commencement of each single cycle.

Bit 12
Reset prior to start of a double cycle.
The preset counters are loaded only at the start of each double cycle.
If bits 11 and 12 are both in their active states ie.logic '1', then the preset counters are loaded twice during each double cycle. (Fig.2d) One or both of the reset bits must be enabled for the module to operate correctly.

Bits 13>15
Must be at logic '0'.

2) Load Delay Buffer A FM2 A1

Bits 0>14
15 bit binary delay count providing a possible delay of up to 32 Sec.
Bit 15
Logic zero.

3) Load Delay Buffer B FM2 A2

Bits 0>15
Specification as per 2).

TIMING TGI

4) Read Control + Event Word FM6 A6

5) Read Delay Buffer A FM6 A1

6) Read Delay Buffer B FM6 A2

7) Read Delay Counter A FM6 A3

8) Read Delay Counter B FM6 A4

9) Reset FM0 A0
This function provides a software reset facility as distinct from the automatic one.

10) Decrement FM0 A1
This function provides the test facility of decrementing both the counters simultaneously under program control.

11) Enable Inhibit A FM0 A2
This function disables counter A and also disables output A.

12) Disable Inhibit B FM6 A3
The counter and output A are enabled. This action is also performed by Programmed Reset.

13) Enable Inhibit B FM0 A4
This function disables counter B and also disables output B.

14) Disable Inhibit B FM0 A5
The counter and output B are enabled. This action is also performed by Programmed Reset.

INITIALIZATION

There are four modes of reseting the module:

1) Single Cycle Reset

2) Double Cycle Reset

3) Program Reset

4) Power-on Reset

These four signals are used in various ways to produce a reset pulse. This pulse transfers data from the delay buffers to the down-counters. Power-on Reset and Programmed Reset unconditionally generate the reset pulse. Single Cycle and Double Cycle Reset are conditioned by bits 11 and 12 of the Control + Event word, the appropriate bits must be enabled in order to permit the signals to produce a reset pulse.

GENERAL TIMING MODULE - TIMING TG2

INTRODUCTION.

This is a general purpose timing module designed to fulfill the majority of users requirements. The module generates two pulses, the first being referenced to either the event or the front panel External Start input, whilst the second is generated a given number of clock pulses after the first pulse. The clock may be the 1mSec. global clock train or a users external clock. The single width 3U unit can be plugged into any location of a standard GP.MPX crate.

The three operating parameters, Control + Event word, Delay 1 and Delay 2, are loaded from the local computers into the timing module by means of the GP.MPX system. Likewise the global timing signals, Reset, 1mSec Clock and Event Train are also connected through the GP.MPX Dataway. Individual user signals viz, Output Pulse 1, are connected by means of front panel BNC connectors. TTL signals to other timing modules and monitor points are connected to Lemo connectors.

A balanced line driver output, transformer isolated, is provided for connecting to a number of user modules situated in the same GP.MPX crate as the TIMING TG2. The pulse will be 2uSec wide and can be connected to either OP1 or OP2 by means of an internal link. Also a TTL level Window signal is generated which is activated by the first output pulse and disabled by the second. Typically this signal could be used to provide the 'gate' input to a number of CAMAC scalers.

A block diagram of the module is shown in Fig.1.

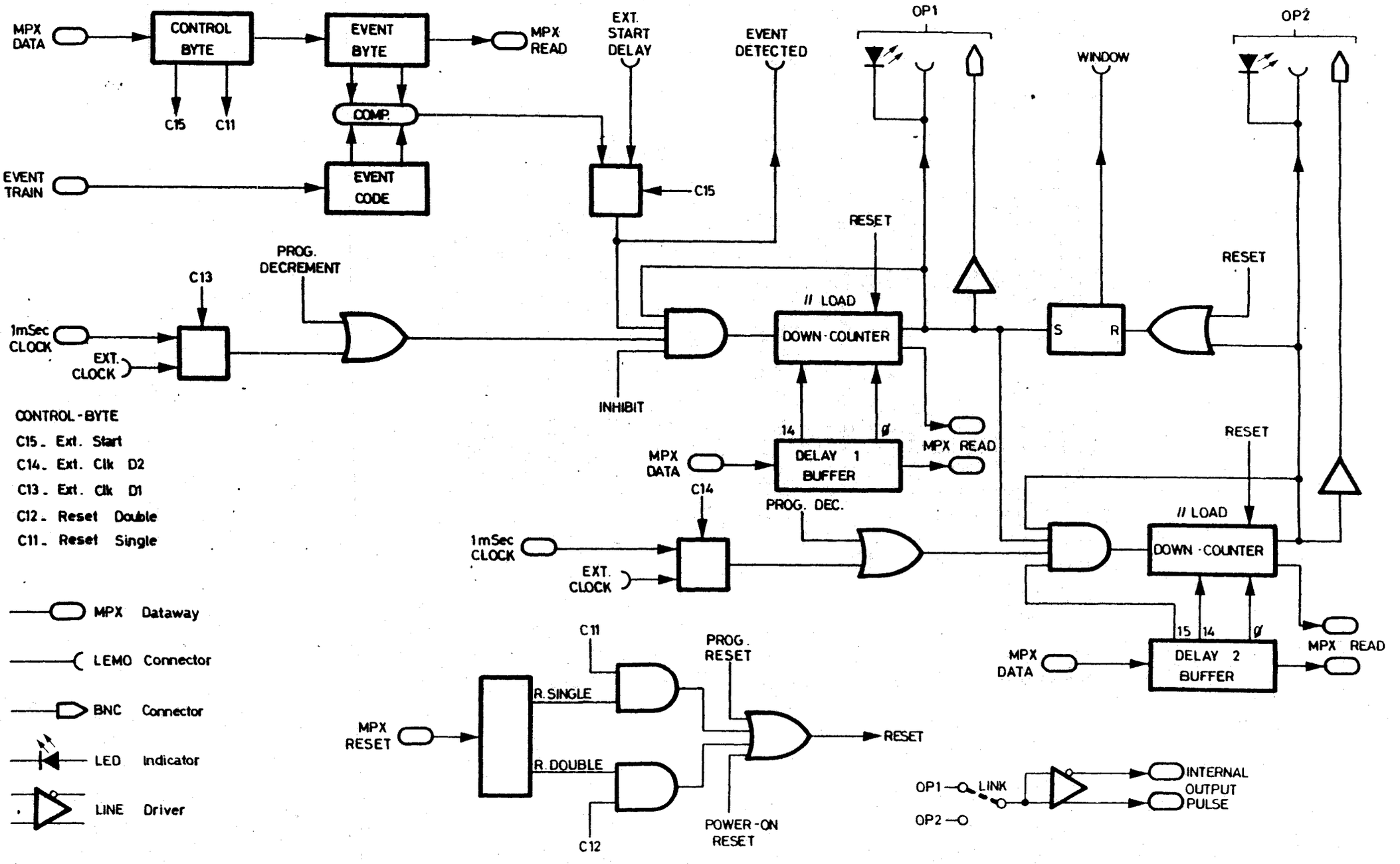

FIG. 10 BLOCK DIAGRAM OF MODULE TIMING G2

PRINCIPLES OF OPERATION

The various registers of the module must be pre-loaded from the local computers to enable the module to function correctly. The Control + Event Word and the Delay 1 buffer must always be loaded, Delay 2 buffer is optional depending upon the users requirements. Both the counters are the preset, count down to zero type which permit one operation per SPS cycle. A double cycle may effectively be considered as two single cycles. If a particular operation, eg. Beam Dump, has the same Event Code for both cycles then the module can be programmed to operate on either or both of the cycles by means of the two reset bits, C11 and C12. This is possible because once an output has been triggered the associated counter remains disabled until reset occurs. If each operation on a double cycle has a unique Event Code then the module will only operate once per double cycle unless the parameters are changed before the second cycle commences.

The contents of the Control Byte determine the mode of operation of the unit. The various modes are explained in the GP.MPX COMMANDS section. This section also contains the Multiplexer Function (FM) plus the sub-address (A) for each operation. The read functions (FM6) are provided primarily as a module commissioning and debugging aid although obviously they can be used for data validation purposes. This facility must not be used during an SPS cycle as a time clash may occur with the timing signals which could prevent an Event from being recognised. This is due to the fact that data is transfered serially and in order to prevent an erroneous comparison during this shift operation the comparator is disabled whenever the module is addressed by the computer.

TIMING TC2 FEATURES

3 Digital Inputs from the computer via the GP.MPX Bus

1) Event Byte + Control Byte

2) Delay, either in 1mSec or external clock units, between event En. and the first output pulse.

3) Delay, either in 1mSec or external clock units, between the first and the second output pulse.

6 Inputs

1) 1mSec Clock
2) Event Train
3) Event Train Clock
4) Reset Single + Reset Double

!--MPX Dataway

5) External Clock
6) External Start Delay

!--Front Panel Lemo

2 User Blocking Oscillator outputs

1) Output Pulse 1
2) Output Pulse 2

!--Front Panel BNC

1 User Line Driver output

1) Internal Output Pulse !--MPX Dataway

TIMING TOO

4 User TTL outputs

1) Output 1
2) Output 2
3) Window. OP1>OP2
4) Event Detected

!
!
!
!--Front Panel Lemo
!
!
!

2 Led.Indicators

1) Output 1
2) Output 2

GP.MPX COMMANDS

1) Load Control + Event Word FM2 AØ

Bits Ø>5
Six bit Event Code allowing for up to sixty three different events per cycle.

Bits 6>7
Must be at logic 'Ø'.

Bits 8>1Ø
Reserved Control bits.

Bit 11
Reset prior to start of a single cycle. The preset counter associated with Output 1 is loaded with the count value from delay 1 buffer prior to the commencement of each single cycle.

TIMING TG2

Bit 12
Reset prior to start of a double cycle. Output 1 preset counter is loaded only at the start of each double cycle.
If bits 11 and 12 are both in their active states ie.logic '1', then the preset counter is loaded twice during each double cycle Fig 2d. One or both of the reset bits must be enabled for the module to operate correctly.

Bit 13
External Clock D1. If at logic '0' the 1mSec clock is selected to decrement delay 1 counter, if at logic '1' the External Clock is selected.

Bit 14
External Clock D2 If at logic '0' the 1mSec clock is selected to decrement delay 2 counter, if at logic '1' the External Clock is selected.
The various timing modes possible from the use of the two Control bits 13 and 14 are illustrated in Fig.11

Bit 15
External Start Delay. If at logic '0' the first delay counter starts decrementing with a valid event comparison. If at logic '1' decrementing commences with the External Start Delay signal, thus allowing several modules to start from a common external origin.

2) Load First Delay Buffer FM2 A1

Bits 0>14
15 bit binary delay count providing a possible delay of up to 32 Sec. when using the 1mSec clock.

Bit 15
Logic zero.

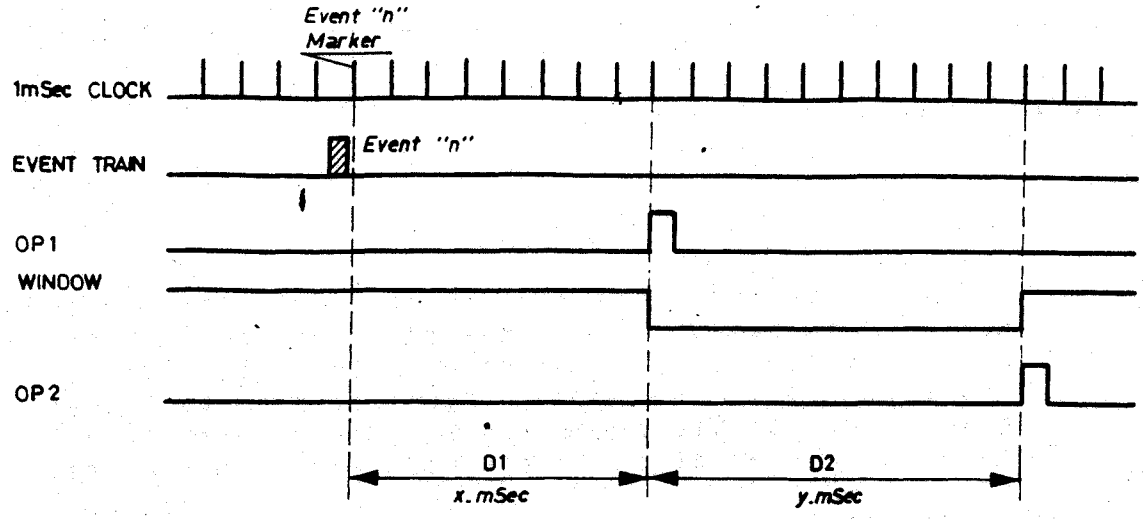

FIG. 11a

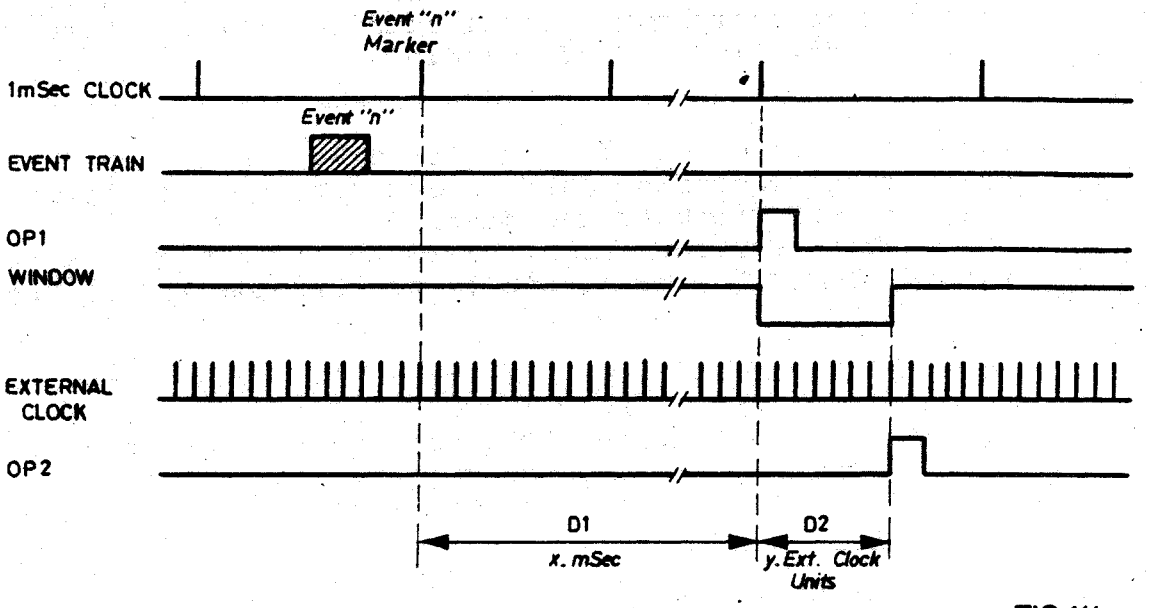

FIG. 11b

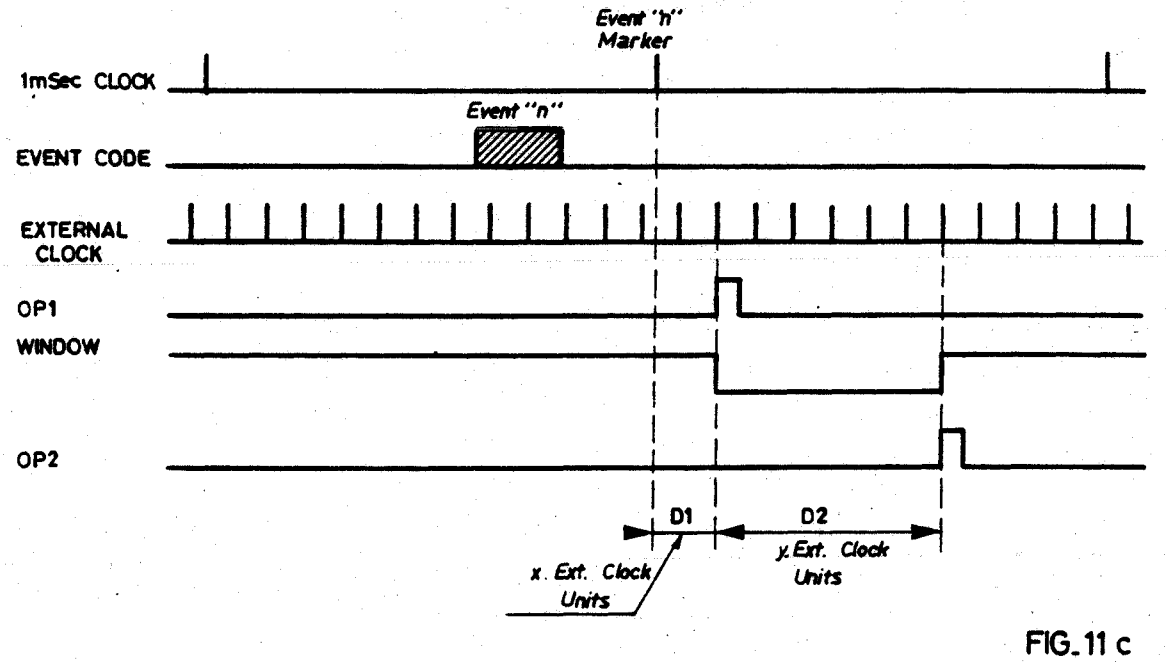

FIG. 11 c

FIG. 11 DIFFERENT DELAY MODES OF GENERAL MODULE TIMING G2

TIMING T32

3) Load Second Delay Buffer FM2 A2

Bits 0>14
Specification as per 2).

Bit 15
Logic '0' counter enabled
Logic '1' counter disabled. This facility enables the module to generate Output Pulse 1 only.

4) Read Control + Event Word FM6 A0

5) Read First Delay Buffer FM6 A1

6) Read Second Delay Buffer FM6 A2

7) Read First Delay Counter FM6 A3

8) Read Second Delay Counter FM6 A4

9) Reset FM0 A0
This function provides a software reset facility as distinct from the automatic one.

10) Decrement FM0 A1
This function provides the test facility of decrementing the counters under program control.

11) Enable Inhibit FM0 A2
This function disables the counters and also disables the outputs.

12) Disable Inhibit FM0 A3
The counters and the outputs are enabled. This action is also performed by Reset.

TIMING TGG

INITIALIZATION

There are four modes of reseting the module:

1) Single Cycle Reset

2) Double Cycle Reset

3) Program Reset

4) Power-on Reset

These four signals are used in various ways to produce a reset pulse. This pulse transfers data from the delay buffers to the down-counters. Power-on Reset and Programmed Reset unconditionally generate the reset pulse. Single Cycle and Double Cycle Reset are conditioned by bits 11 and 12 of the Control + Event word, the appropriate bits must be enabled in order to permit the signals to produce a reset pulse.

DISPLAY TIMING MODULE - TIMING TD

INTRODUCTION

During the system commissioning and installation phase it is extremely important for the users to know that the timing signals have occured in the correct sequence and at the correct time.This module is designed to provide that information visually.

The three displays of TIMING TD indicate the Event, Delay 1 and Delay 2 of the timing module connected to it. It may be connected to both the general timing modules and also the manual timing module. During run time the module may be used both as a debugging aid for locating the boundary between good and faulty equipment and also as a 'comfort' indicator for the users, especially when they are changing their timing parameters. It is not intended that these modules be permanently installed in every GP.MPX timing crate.

A block diagram of the module is shown in Fig 12.

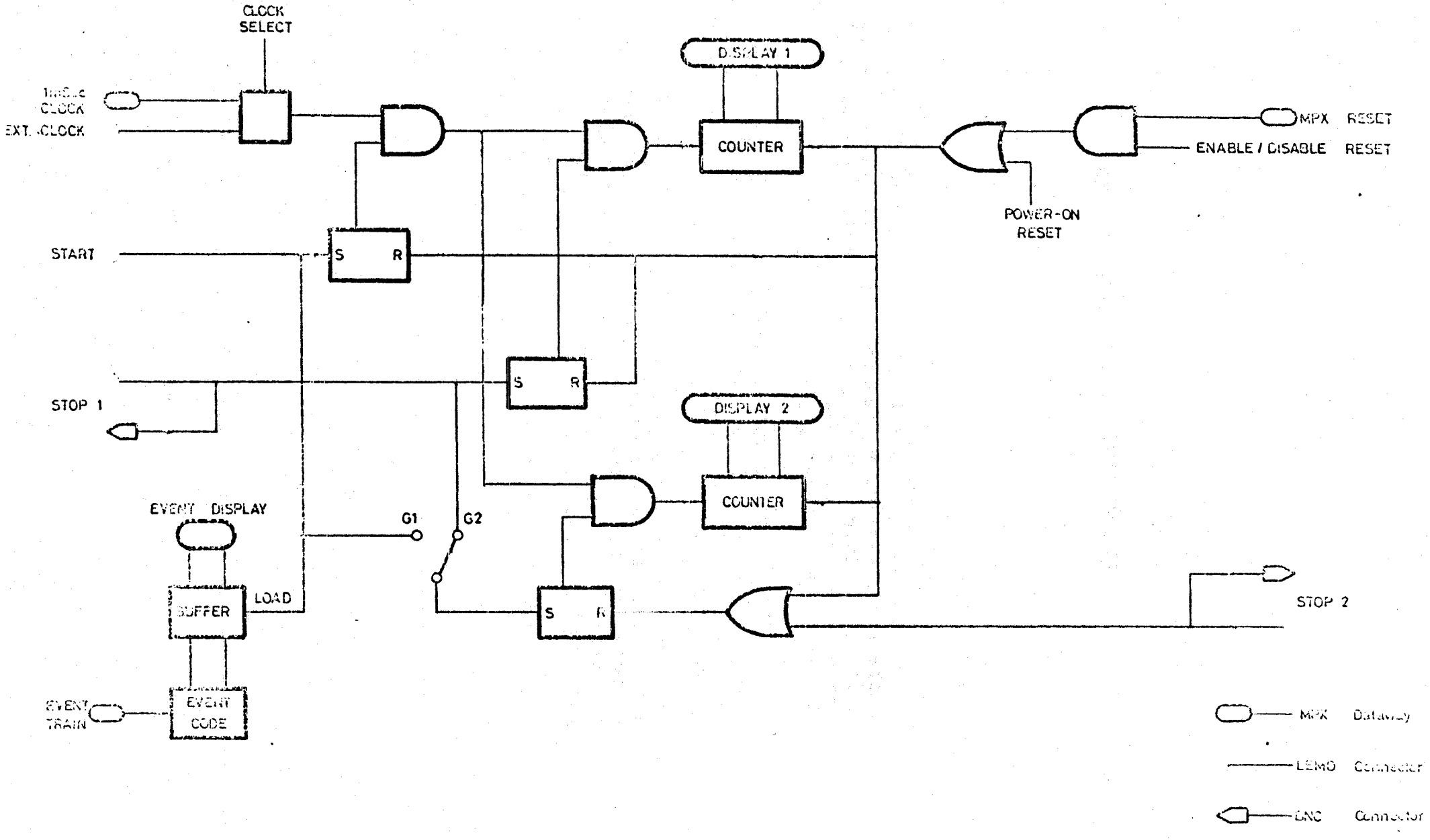

FIG. 12 BLOCK DIAGRAM OF MODULE TIMING D

TIMING TD

PRINCIPLES OF OPERATION

The module is not intended to detect the obscure intermittent fault but rather to indicate that the overall system is either operating correctly or that there is a 'hard' fault in the system. Typically it will operate in conjunction with the general timing modules. In this mode the following connections are required between the outputs of the Timing TG and the inputs of Timing D. Either the TTL or the blocking oscillator outputs may be used.

TIMING TG	TIMING TD
OP 1	STOP 1
OP 2	STOP 2
EVENT DETC.	START

When the module receives the START signal the event code that was transmitted by the Event Train during the previous one millisecond time interval is indicated by the event display. With the Internal Clock and Internal Reset selected Display 1 indicates the time, in mSec, between the specified event and Output 1, whilst Display 2 indicates, again in mSec, the delay between Output 1 and Output 2. If the user desires the display outputs to be referenced to TØ rather than the Event then the START input should be terminated in a 50 Lemo terminator. In this mode display 1 indicates the time between TØ and Output pulse 1, Display 2 remains as before and the event display indicates zero.

The External Clock input is provided to enable the user to connect his own external clock to the module so that Display 1 and Display 2 indicate external clock units as opposed to mSec. It is not possible to mix the mSec and the external clock. The two possible modes of timing are illustrated by Fig.11a and 11b of module Timing TG2.

TIMING TD

TIMING TD FEATURES

3 Displays

1) 2 Decade seven segment display, Event.

2) 5 Decade seven segment display, Delay 1.

3) 5 Decade seven segment display, Delay 2.

10 Inputs

1) 1mSec Clock
2) Reset
3) Event Train
4) Event train Clock

--MPX Dataway

5) Start
6) Stop 1
7) Stop 2
8) External Clock

--Front Panel Lemo

9) Stop 1
10) Stop 2

--Front Panel BNC

3 Switches

1) Select 1mSec - External Clock

2) Select TIMING TG1 - TIMING TG2

3) Enable / Disable Reset

TIMING TD

GP.MPX COMMANDS

None.

The module only uses the GP.MPX Dataway as a means of obtaining logic power and the global timing signals.

INITIALIZATION

There are two modes of reseting the module:

1) Single + Double Cycle Reset

2) Power-on Reset

The reset signal clears the three displays plus their counters to zero and also enables the module to accept another data acquisition. The front panel Enable / Disable switch provides a means of preventing the module from being reset at the start of each cycle. This provides the user with a means of retaining a faulty indication as 'proof' of a malfunction.

MANUAL TIMING MODULE - TIMING TM

INTRODUCTION.

This module enables users to change their timing parameters without the need for computer intervention. The delays controlling the output pulses are varied by means of a hand-held switching unit.

The mode of operation of the module is similar to TIMING TG1. The two output pulses can be varied independently of each other but both are referenced to the same event and occur a given number milliseconds after that event. The module resets itself on both the Reset Single and Reset Double, it is not possible to select one or the other. Users who require a more complex unit should use the TIMING TG2 module and vary the paramters by means of the computer operating system.

A block diagram of the module is shown in Fig 18.

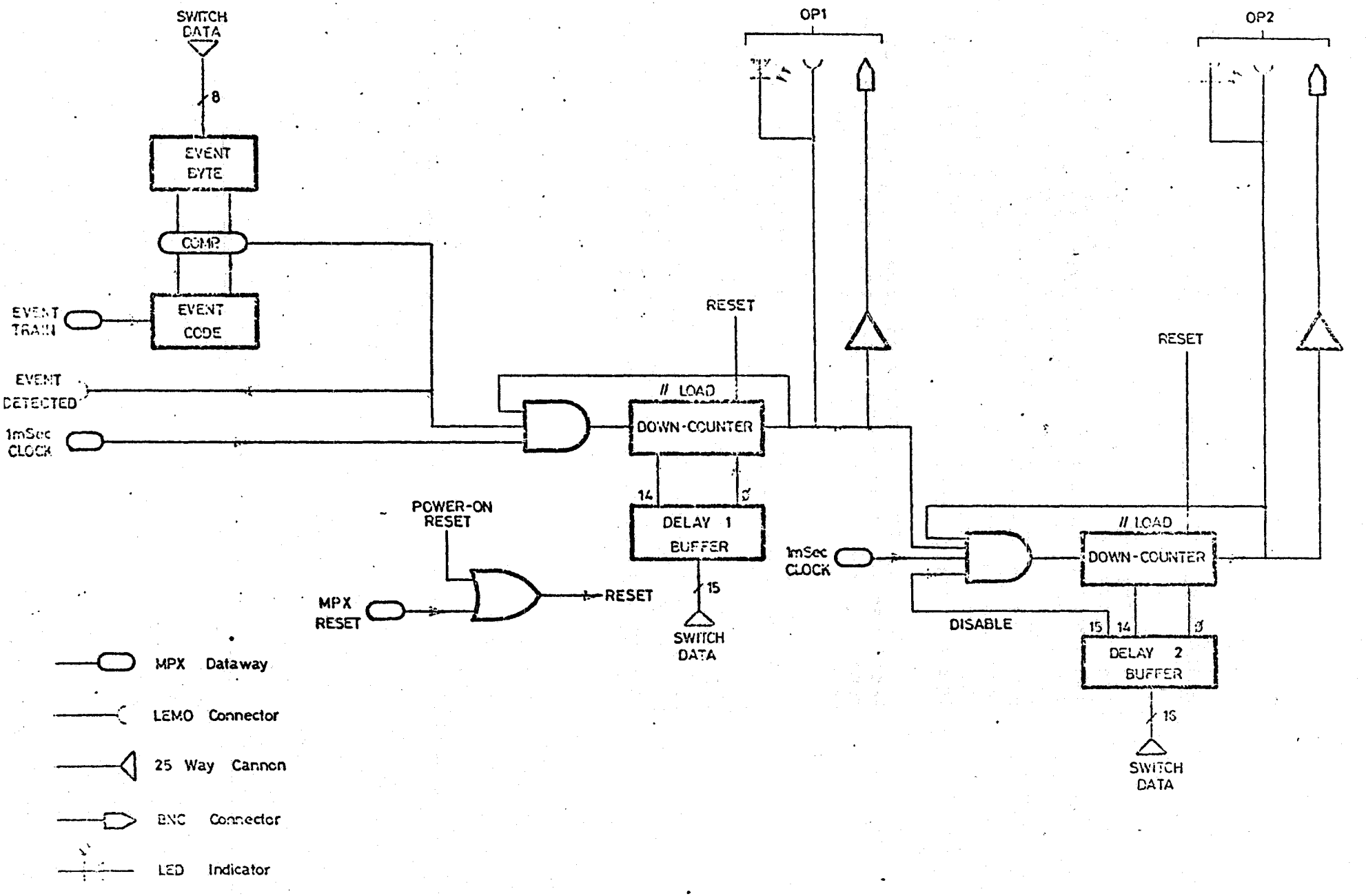

FIG. 13 BLOCK DIAGRAM OF MODULE TIMING TM

PRINCIPLES OF OPERATION

The hand-held switching unit must be connected to the TIMING TM by means of a standard 25 way Cannon cable. The register that requires modifying is selected by the three position rotary switch. The parameters that can be altered are the Event Code, Delay 1 and Delay 2. The new value of the selected register is entered into the switch unit via the thumb-wheel switches and this new value is then transfered into the TIMING TM by depressing the Insert push-button.

It is not necessary to have a switching unit for each manual timing module, one switching unit should control a number of modules simply by plugging it into each module in turn.

Under normal operating conditions the output pulses are referenced to the Event code Marker Pulse, but if the user wants to use TM as the reference point this may be accomplished by terminating the Event detected output with a 50 Lemo terminator. The Event Detected TTL output is to make the module compatible with the general timing modules and also the manual module so that it may work in conjunction with TIMING TD.

TIMING TM

TIMING TM FEATURES

3 Digital Inputs from the hand-held switching unit by means of the front panel 25 way Cannon connector.

1) Event Byte

2) Delay, in 1mSec. clock units, between event En. and the first output pulse.

3) Delay, in 1mSec. clock units, between event En. and the second output pulse.

4 Inputs

1) 1mSec Clock
2) Event Train
3) Event Train Clock
4) Reset Single + Reset Double

--MPX Dataway

2 User Blocking Oscillator outputs

1) Output Pulse 1
2) Output Pulse 2

--Front Panel BNC

3 User TTL outputs

1) Output 1
2) Output 2
3) Event Detected

--Front Panel Lemo

TIMING TM

2 Led.Indicators

1) Output 1

2) Output 2

GP.MPX COMMANDS

None.
The module only uses the GP.MPX Dataway as a means of obtaining logic power and the global timing signals.

INITIALIZATION

There are two modes of reseting the module:

1) Single + Double Cycle Reset

2) Power-on Reset

The reset pulse transferes data from the delay buffers to the down counters. This action is performed by both modes unconditionally.

FAN-OUT MODULE TIMING TF

DESCRIPTION

This module provides the user with the facility to distribute a pulse from a single timing module to a number of external locations simultaneously. The module receives a single blocking oscillator or TTL type input and generates five blocking oscillator transformer isolated outputs. The propogation time between the input and output pulse will be less than ten nano-seconds. A maximum of two modules can be connected together in parallel to provide ten simultaneous outputs. If the user requires more than ten such outputs then the modules must be cascaded together.

The 3H module only uses the GP.MPX Dataway as a means of obtaining logic power, consequently it will operate in all powered MPX crates.