Performance of the Demonstrator System for the Phase-I Upgrade of the Trigger Readout Electronics of the ATLAS Liquid Argon Calorimeters

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ABSTRACT: For the Phase-I luminosity upgrade of the LHC a higher granularity trigger readout of the ATLAS LAr Calorimeters is foreseen to enhance the trigger feature extraction and background rejection. The new readout system digitizes the detector signals, which are grouped into 34000 so-called Super Cells, with 12 bit precision at 40 MHz and transfers the data on optical links to the digital processing system, which extracts the Super Cell energies. A demonstrator version of the complete system has now been installed and operated on the ATLAS detector. Results from the commissioning and performance measurements are reported.

KEYWORDS: ATLAS; Liquid argon calorimeter; Trigger, Electronics, Phase 1.

Contents

1. Introduction

The ATLAS detector [1] operated very successfully during Run 1 (2009-2013) and collected a large number of events during proton-proton and heavy ion collisions, leading to important discoveries [2]. The calorimeters, in particular the Liquid Argon (LAr) calorimeter, play an essential role in the energy measurement of all particles and also in the calorimeter trigger.

One particular challenge when looking towards the future operation of the ATLAS detector and the LAr calorimeters is the limitation in the online event selection (Level-1 trigger) due to the existing trigger electronics with its constraints in granularity, bandwidth and latency. Without modifications, the peak instantaneous luminosity of $3x10^{34}cm^{-2}s^{-1}$ expected during Run 3 (2018-2022), would force substantial increases in trigger thresholds because the detector will be operated in an environment with a mean number of pileup events of $\langle\mu\rangle = 55$ per bunch crossing, as opposed to $\langle\mu\rangle \sim 20$ during Run 1. The ATLAS is also constrained by readout dead time to a 100 kHz event rate at the Level-1 trigger.

In order to handle the increased background rates to lepton triggers, the upgrade of the LAr calorimeter trigger readout electronics aims at keeping the capability of triggering on low electromagnetic (EM) transverse energy (E_T). In 2014 a first version of the upgraded trigger readout electronics has been installed to demonstrate the feasibility of a new triggering system. The motivation and the new components of such a demonstrator system are described in the Section 3. The following paragraphs present the installation of the front end and back end electronics and present the first results taken during calibration runs in the ATLAS cavern.

2. ATLAS calorimeters

The ATLAS calorimetry system consists of several sectors; all fully symmetrical in φ. They are designed to measure energy deposits of both charged and neutral particles within $|\eta| < 4.9$. The structure of the ATLAS calorimeters is shown in Figure 1.

ATLAS calorimeters are sampling calorimeters. Thus, absorber layers which initialize particle showers are alternated with layers of active material to perform energy measurements. An incident particle produces showers in stages, losing energy until the shower is completely absorbed. By summing up all measured energy within the calorimeter, the initial energy of the particle is reconstructed. In the EM calorimeter, the forward calorimeter (FCal) and the endcap of the hadronic calorimeter (HEC), LAr is used as active medium. In the barrel hadronic region scintillating tiles are used. LAr does not suffer from radiation damage as opposed to the tiles and is therefore preferable in the region close to the interaction point and in the forward region.

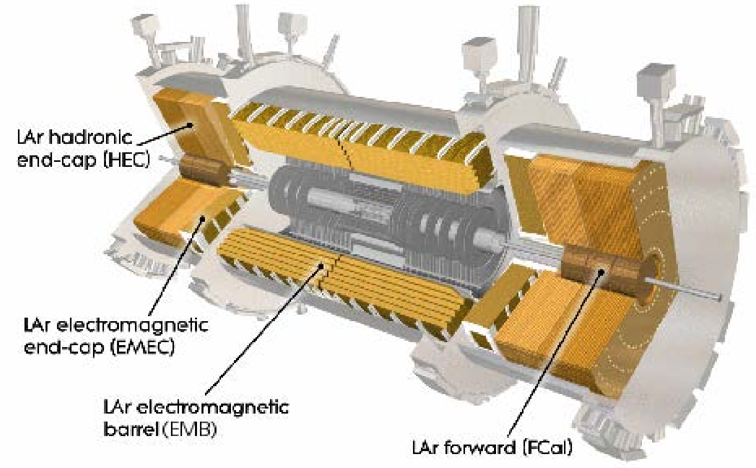

Figure 1 : The ATLAS calorimeters

The central cryostat contains the EM barrel (EMB) calorimeter and the superconducting solenoid. Each endcap cryostat houses an EM Endcap (EMEC), two hadronic wheels and one FCal with 3 layers. The barrel of the LAr calorimeter is longitudinally separated into layers: the presampler, front, middle and back layer. The accordion geometry is motivated by the aim to have full φ coverage with no cracks in between the module edges. In the EM barrel and the EMEC the absorbing material is lead, in the HEC copper is used. For the FCal, tungsten or copper rods, which form the cathode of the LAr cell, are set into an absorber matrix (copper for the EM module and tungsten for the two hadronic modules).

3. Triggering system

3.1.1 Motivation for an upgrade [3]

The existing triggering system is based on the concept of the "Trigger towers" where E_T is summed across the longitudinal layers of the calorimeters in an areas as large as $\Delta\eta * \Delta\varphi = 0.1*0.1$. The new finer granularity scheme is based on Super Cells, which provide information for each layer of the calorimeter and finer segmentation areas as large as $\Delta\eta * \Delta\varphi = 0.025*0.1$ in the front and middle layer of the EMB and EMEC. In that scheme E_T is summed in calorimeters and the segmentation of the detector is increased by up to a factor of 10.

To illustrate the difference between the two concepts, the Figure 2 shows one 70 GeV electron shower which deposits energy in only one calorimeter Trigger tower whereas the same shower can be seen by several Super Cells in each detector layer. The finer granularity of the Super Cells will improve the trigger energy resolution and efficiency for selecting electrons, photons, τ leptons, jets and missing transverse momentum, while enhancing the discrimination against hadronic jets and pileup.

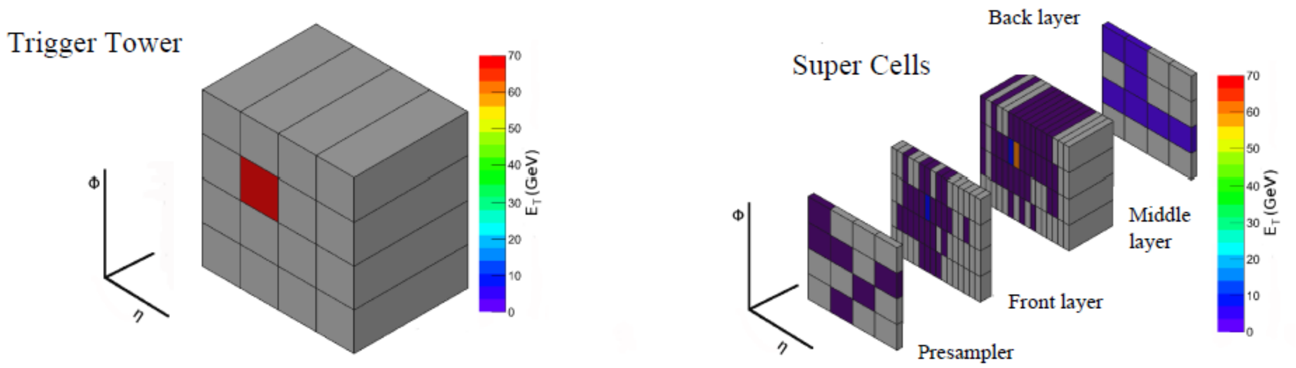

Figure 2 : A 70 GeV shower seen by one Trigger Tower or multiple Super Cells

3.1.2 New trigger electronics architecture

The readout electronics is described in the Figure 3 where the current and the upgraded systems are shown. The blue block represents the synoptic of the current readout system while the red block contains the upgraded triggering system.

The calorimeter cells deliver a triangular signal to the Front End Boards (FEB) [4] where this signal is amplified, shaped and stored in an analog circular buffer waiting for the decision of the Level 1 accept (L1A) coming from the L1A calorimeter triggering system. Once this decision is received, the signal is digitized with a 12 bits ADC and typically 4 samples are sent over 70m of optical fibers to the next electronics stage which is made by the Read Out Driver (ROD) boards [5]. These boards process the incoming data with optimal filtering algorithms in order to extract the energy, the timing and the form factor of the pulse for the Data Acquisition system.

In parallel to this regular readout, signals for the L1A are summed to form the current Trigger Towers which cover a trigger unit of $\Delta\eta * \Delta\varphi = 0.1*0.1$ of the calorimeters. This analog summing is performed in 3 steps: on the shaper chips, on the Layer Sum Boards (LSB) located on the FEB and on the Tower Builder Boards (TBB) [6]. The resulting analog sums are transferred to the trigger receivers, which can equalize gain differences among channels, and then passed on to the L1ACalo digitizer system operating at 80 MHz

The upgraded triggering system, shown in the red block, will segment the calorimeters into the new Super Cells corresponding to a trigger unit of $\Delta\eta * \Delta\varphi = 0.025*0.1$. The new LSB produces a summing with a finer granularity in order to build the Super Cells signals. These signals are driven over the Front End Crate (FEC) backplane to the new LAr Trigger Digital Board (LTDB) [7] which digitizes the Super Cell signals with a 12 bits ADC at 40MHz. The samples are sent over optical fibers to the new Back End electronics made by the LAr Digital Processing Boards (LDPB) which calculate the transverse energy deposited by particles showers and assign it to the correct bunch crossing. These results are transmitted to the L1A calorimeter system in order to produce the L1A decision.

It has to be noted that, during the Ru n3 startup, the current analog and upgrade digital system will work in parallel. That is why the Trigger Tower summing will be performed partially by the new LSB and the new LTDB and rerouted by the FEC backplane.

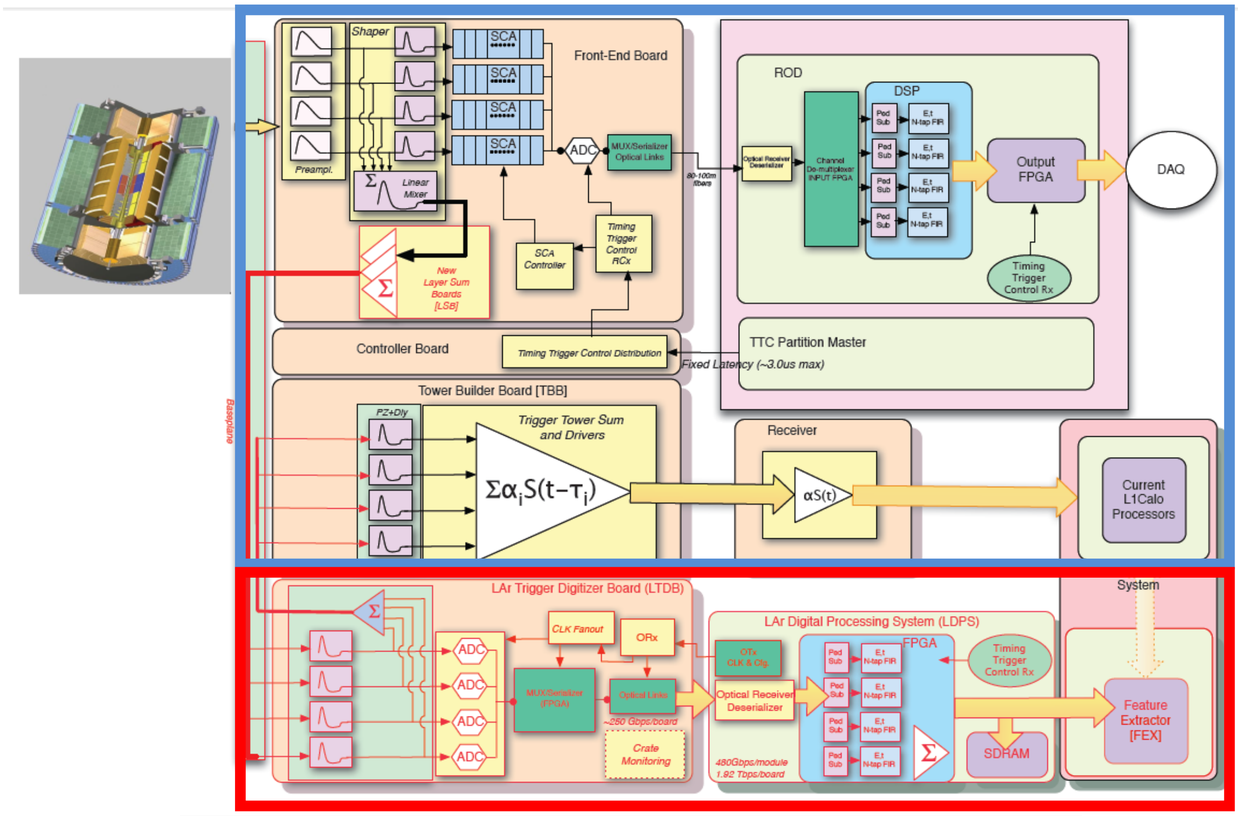

Figure 3 : The current and upgraded architecture of the LAr calorimeter trigger readout

4. Demonstrator

4.1.1 Goal of the Demonstrator

Before installing the upgrade system in 2019, a demonstrator has been designed, validated and installed during the Phase 0 shutdown in 2014. One FEC corresponding to the part of the Electromagnetic barrel covering an area of $1.767<\varphi<2.160$, $0<\eta<1.4$ has been equipped with a non-radiation hard version of the electronics foreseen for the Phase 1 upgrade. The goal was to show that this demonstrator does not disturb and does not add extra noise to the current system and to evaluate the procedure for the replacement of the backplane and also to gain experience on the Super Cell pulse shapes and timing during the Run 2 of the LHC.

4.1.2 New components

New electronics components have been integrated in this FEC to construct and digitize the Super Cells and also in the Back End part in order to process the Super Cells samples in real time.

The two backplanes of the demonstrator FEC have been removed and replaced by the new version in order to integrate the new LTDBs, to route the Super Cells signals from the FEBs to the LTDBs but also to reroute the old Trigger Tower signals from the LTDBs to the Tower Builder Boards.

The Layer Sum Boards of the Front End Boards plugged into this crate have been replaced by a new version which forms Super Cells with a finer granularity and drives these signals to the LAr Trigger Digital Board. This new version is able to quantify the calorimeters cells with a granularity of 64 to 250 MeV instead of 1 GeV for the previous version.

Two LTDBs have been integrated inside the demonstrator FEC. These boards handle up to 320 Super Cells signals (284 SC for the electromagnetic barrel) and the digitization is performed in parallel with commercial 12 bits ADCs (TI ADS5272) at 40 MHz. The samples of eight Super Cells are multiplexed, encoded in 8B10B, serialized and transmitted at 4.8 Gbps by the last generation FPGA over optical fibers. Two LTDB versions (illustrated on the Figure 4) have been designed with the digital (built by BNL) part or the analog part (built by LAL/CEA) on the mother boards. They deliver a continuous bandwidth of 200 Gbps across 40 optical links to the Back End electronics.

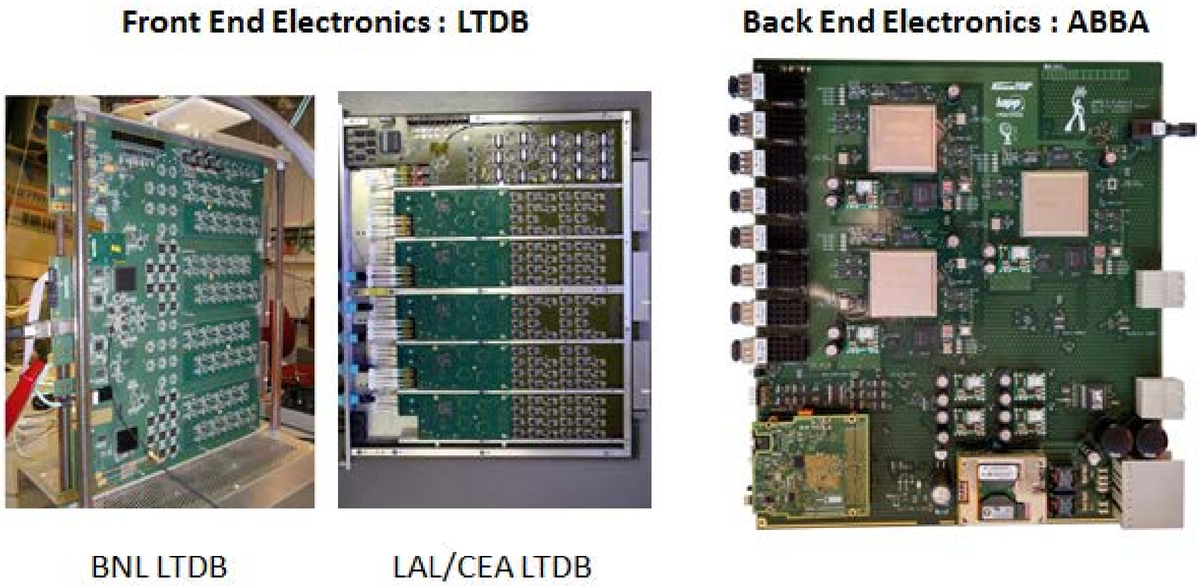

Figure 4 : The new LTDBs and ABBA boards developed for the demonstrator

The readout of the two LTDBs takes place in the USA15 ATLAS counting room with 2 ABBA [9] (ATCA [8] Board for a Baseline Acquisition) boards shown on the Figure 4 and housed in an ATCA shelf. Each ABBA board receives the data from one LTDB over 40 optical links at 4.8 Gbps and processes the Super Cells samples with the last generation FPGA. The continuous incoming streaming of the 320 Super Cells samples is stored in circular buffers with a depth defined by the L1A trigger latency. Once a L1A is received, typically 10 samples per Super Cell corresponding to this bunch crossing are extracted from the circular buffers, packed and read out over the ATCA fabric interface over the 10GbE network with the IPBus protocol. The configuration, the acquisition and the monitoring are performed by a PC connected to the 10 GbE network.

4.1.3 Installation

Before going to the UX15 cavern for the final integration, the overall system for the demonstrator was installed, tested and validated in a test setup located in the ATLAS LAr Electronics Maintenance facility (EMF) lab. The final installation of the demonstrator was made in August 2014 in the ATLAS cavern.

The “I06” Front End Crate covering a part of the electromagnetic barrel was dismounted in order to change the 2 backplanes, replace the Layer Sum Boards on all the Front End Boards and to plug the new LAr Trigger Digital Boards (left part of the Figure 5). Seventy meters of optical ribbons were deployed to link the LTDBs transmitters to the ABBA boards.

An ATCA shelf housing two ABBA boards and a central 10 GbE switch was installed in the ATLAS counting room (right part of the Figure 5). The 10 GbE switch collects the data from the two ABBA boards over the ATCA fabric interface and distributes the UDP packets to a readout PC networked to the Trigger and Data Acquisition system (TDAQ).

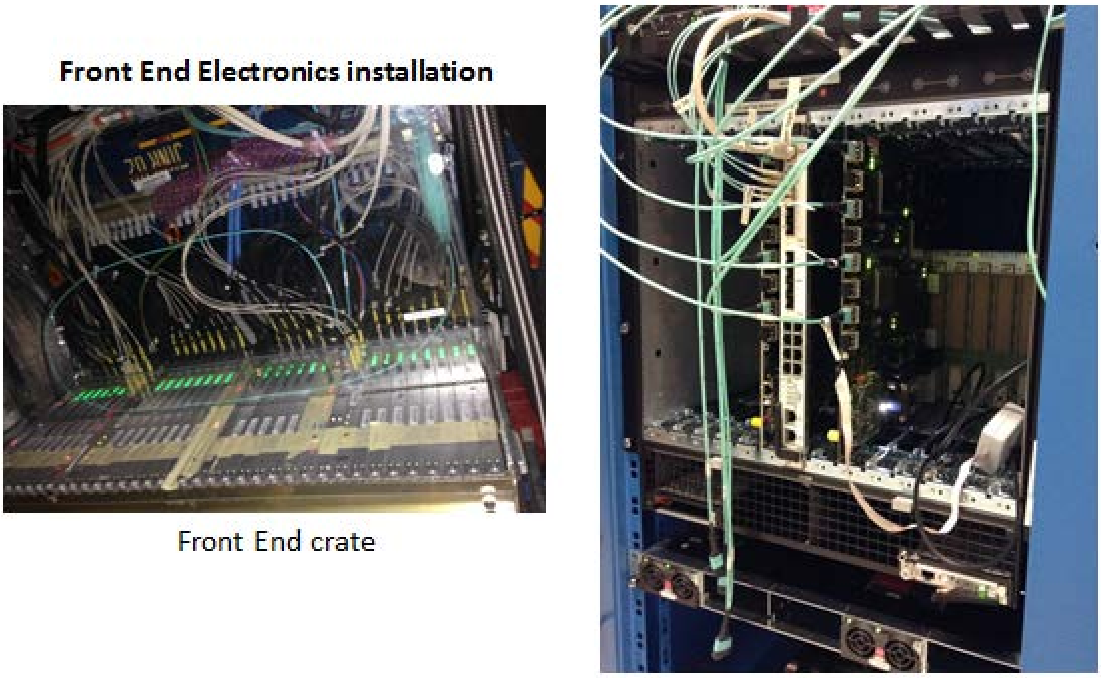

Figure 5 : The installation of the Demonstrator system in the cavern and in the counting room

4.1.4 Acquisition software

The acquisition software is based on the ATLAS TDAQ system. Several PCs are used to configure the LTDBs, to configure and readout the ABBA boards in an asynchronous way through the IPBus protocol and to build a TDAQ event. The IPBus protocol aims to standardize the type of requests delivered by an UDP client.

5. Results

The first test was to verify with the standard readout chain that the demonstrator (LTDB) does not introduce additional noise at the Front End Crate [10].

The pedestal levels for each detector layers were monitored with the readout of the complete demonstrator chain (new backplanes + new Layer Sum Boards + LAr Trigger Digital Boards + ABBA boards.) and the TDAQ software. Figure 6 shows a pedestal run and the RMS of the transverse energy for each sub-detector layers at φ=1.82. The RMS varies from 100 to

200 Mev for the different layers and the jump seen at η=0.8 for the Back layer which reflects the change of the absorber and the electrodes thicknesses and calibration resistors.

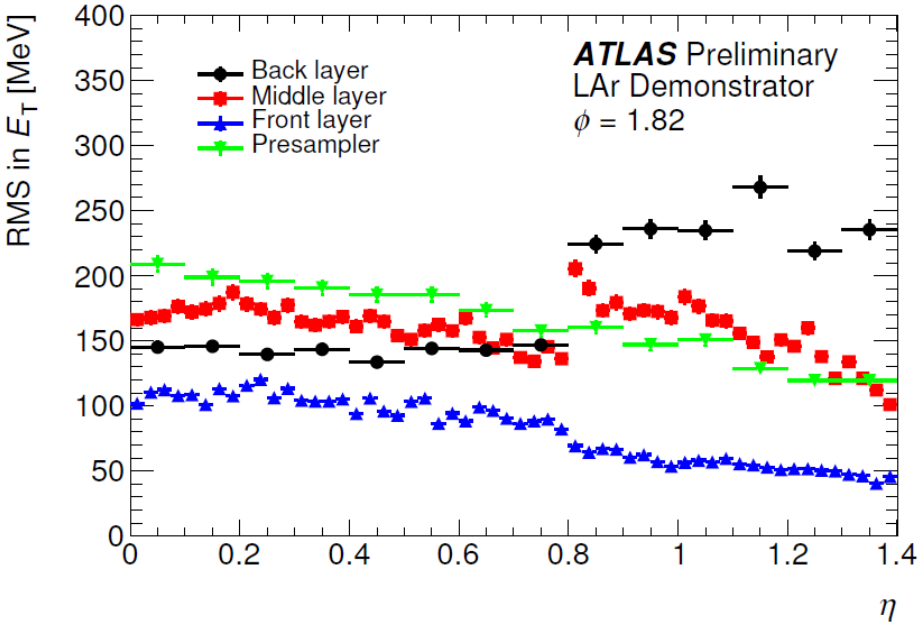

Figure 6 : Super Cells pedestals converted in transverse energy for each sub detector layers [10]

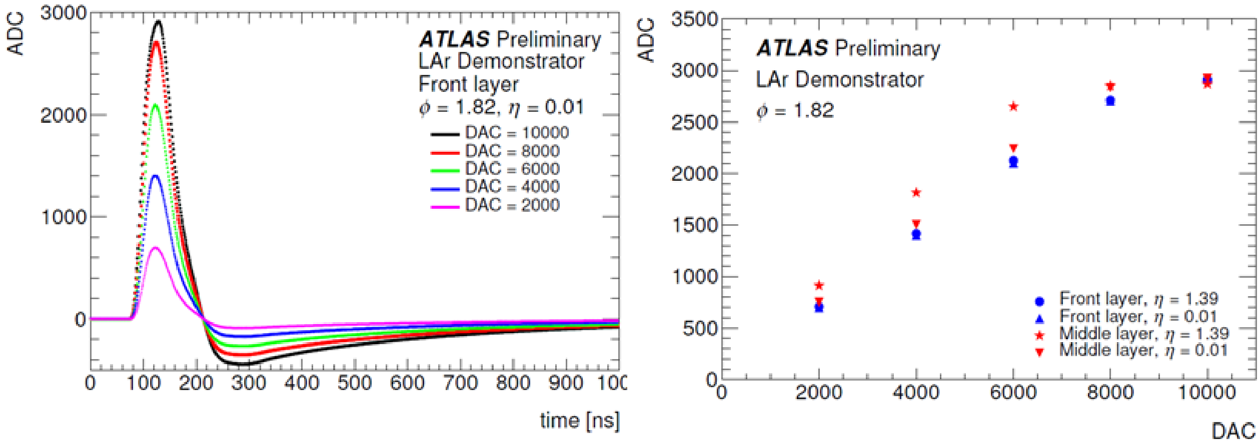

Figure 7 : Calibration pulse shapes for front layer and linearity for each sub-detector layers [10]

In order to verify the pulse shapes and check the linearity, the calibration system was used for injecting signals to the FEBs with different DAC values. The readout was again done with the complete demonstrator readout and the result is presented on the Figure 7.

The left part of the Figure 7 shows different calibration pulse shapes according the calibration DAC values and the right part of the Figure 7 represents the linearity of the calibration pulses according the sub-detector layers. Saturation can be detected above a DAC value of ~8000 and confirms the expected behavior of the Layer Sum Boards saturation above this threshold.

6. Conclusion

A slice of the new trigger scheme has been installed in August 2014 in order to demonstrate the feasibility of the future trigger system. One Front End Crate has been equipped with the new Front End components and the readout has been done over two ATCA boards configured and controlled by TDAQ software.

Different measurements have been done in order to verify that the demonstrator does not affect the current system. The demonstrator readout works in parallel with the regular readout and allows checking the pedestals, the pulse shapes and the linearity using the calibration system for the different sub-detector layers.

The next plans of the demonstrator are to capture pulses coming from real proton-proton collisions during regular LHC running. For that, the trigger selection should be adjusted for the calorimeter region covered by the demonstrator. These data will be analysed in order to tune the coefficients of the optimal filtering algorithm used for the calculation of the energy deposited in the calorimeters cells.

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