The Upgrade of the ATLAS Tile Calorimeter Readout Electronics for Phase II

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Abstract. The Large Hadron Collider at CERN is scheduled to undergo a major upgrade, called the Phase II Upgrade, in 2022. The ATLAS Tile Calorimeter (TileCal) community will do major modifications to the sub-detector to account for the increased luminosity. More specifically, a large proportion of the current front and back-end electronics will be upgraded in order to digitize all signals generated in the Calorimeters. A Demonstrator program has been established, which combines the current and future architectures, as a proof of principle. The insertion of the first demonstrator is planned for the end of 2015.

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1. Introduction

The ATLAS detector [1], one of two general purpose detectors at the LHC, consists of multiple sub-detectors which are designed to detect interesting physics in 40 million bunch-crossings per second. The TileCal, the central region in Fig. 1, is used to measure energies and directions of hadrons, jets, τ and leptons. Particles pass through plastic scintillating tiles which emit light that is guided to photo-multiplier tubes (PMTs). This provides the means to measure energy and direction of hadrons. These light signals are directed to front-end electronics where they are digitised and processed for the first level of triggering. Data from the front-end electronics is transferred off the detector to the back-end electronics where further processing occurs. The ATLAS detector is scheduled to undergo a major upgrade in the year 2022 in order to handle an increased luminosity.

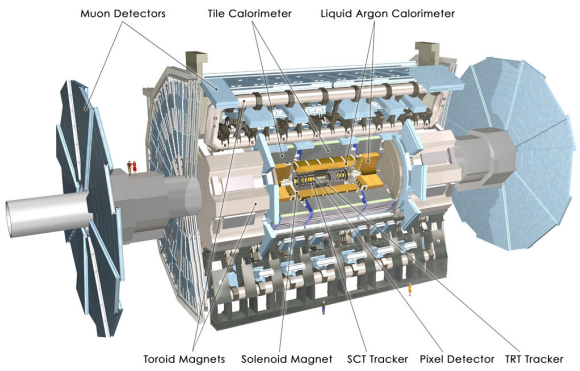


Figure 1: Schematic of the ATLAS detector.

Table 1 illustrates the increase in bandwidth for the TileCAL from the current to future luminosities, which will increase by a factor of 5, providing up to 41 Tbps. As a result the entire front and back-end electronics will be upgraded for the Phase II upgrade [2].

Table 1: Tile Calorimeter Bandwidth Upgrade.

Phase	Present	Upgrade
Number of fibers	256	4096
Fiber Bandwidth	800 Mbps	10 Gbps
Total Bandwidth	205 Gbps	41 Tbps

2. Upgrade of the Readout Electronics

2.1. Current Architecture

The current front-end electronics are located in a super-drawer situated on the outer edge of the Tile Calorimeter. Figure 2 shows the current flow of information. A pulse of light caused by charged particles passing through the scintillating plastic is directed to a PMT using wavelength shifting fibres. The signal is directed to the 3-in-1 cards where two different gains are applied. It is then digitized by an ADC and stored in a pipeline, to wait for a level 1 accept (L1A), on the Digitizer Board. If a L1A is received the data is sent to the interface board where it is formatted and sent at a rate of 100 kHz to the Read of Driver (ROD) located on the back-end. As luminosity increases so does pileup and the amount of data generated. The larger pileup and

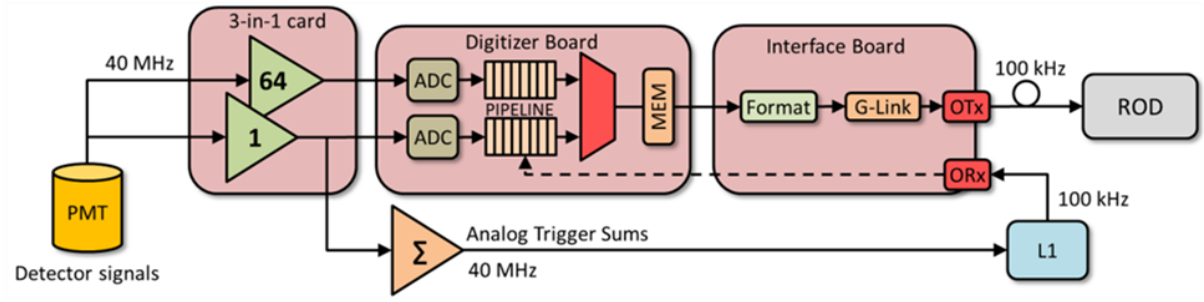


Figure 2: Current read out electronics.

data mean that a better precision and granularity is needed. The radiation levels are expected to increase which can cause errors in sensitive electronics hence radiation hard components are needed. The upgrade allows for the simplification and reduction of maintenance needs by moving a large portion of the front-end electronics off the detector to the back-end. This also reduces the radiation induced errors and provides an opportunity to replace obsolete components.

2.2. Upgrade Architecture

The upgraded front-end electronics are shown in Fig. 3. The components are discussed in more detail below.

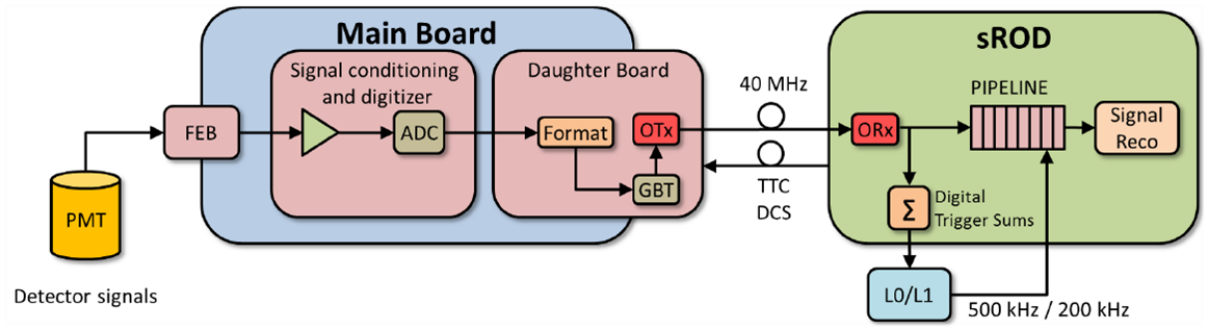


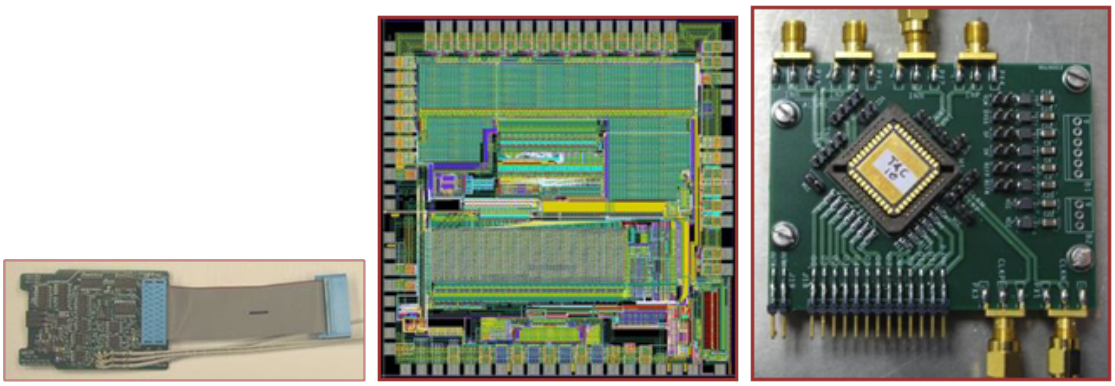
Figure 3: Upgraded read out electronics.

2.2.1. Front-End Boards. There are currently three different front end boards (FEBs) that are being evaluated.

(i) Modified 3-in-1 Boards - It is based on the current design with improvements in radiation hardness, linearity and noise. Shown in Fig. 4a). This board is being designed by the Enrico Fermi Institute, University of Chicago.

(ii) QIE ASIC - This board is a custom Application-Specific Integrated Circuit (ASIC). Shown in Fig. 4b). It is a completely different operating design compared to the 3-in-1 board. It uses a Charge Integrator and Encode (QIE) chip that splits the current into four different ranges with no shaping. This is useful for pile-up as it provides a way to measure every 25 ns. It is a joint effort between the Argonne National Laboratory (ANL) and Fermilab.

(iii) FATALIC - This stands for the Front-end for Atlas TilecAL Inegrated Circuit. Shown in Fig. 4c). This board combines two ASIC solutions (TACTIC and FATALIC). It provides shaping with three different ranges using a 12-bit pipelined ADC. It is also possible to operate at 25 ns. This board is designed at the Laboratoire de Physique Corpusculaire in Clermont-Ferrand (LPC).



(a) (b) (c)

Figure 4: a) Modified 3-in-1 board b) QIE ASIC and c) FATALIC Board

2.2.2. Main Board. The Main board, shown in Fig. 5, is the motherboard for the different components in the drawer. It provides auxiliary functions such as mechanical support and power and is an interface between the different devices. It also allows the monitoring and control of the chosen FEB as well as the low voltage power supplies. The board is divided in the middle along its length in a mirror configuration to provide redundancy.

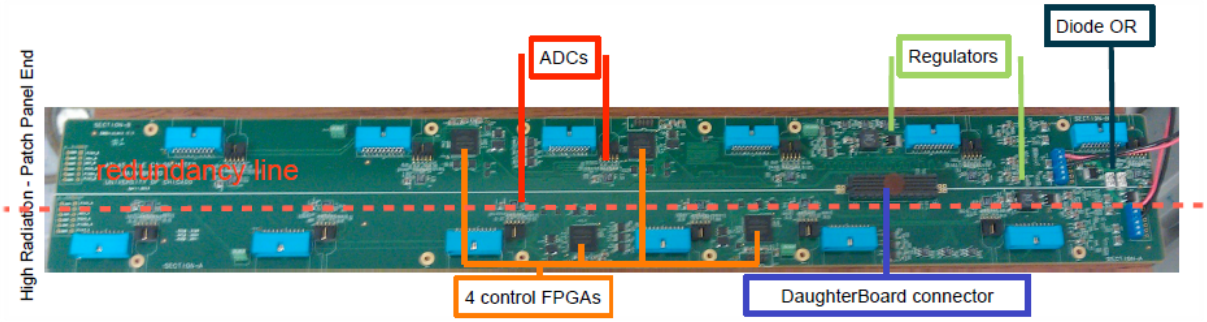


Figure 5: Main board for use with modified 3-in-1 board.

2.2.3. Daughter Board. The Daughter Board (DB), shown in Fig. 7, is connected to the Main Board along the mirror line. The DB provides a high speed communication platform between the detector and the back-end electronics. It is also mirrored down the length of the DB to provide redundancy. The board receives the digitized signals from the main board, packages and sends it to the back-end infrastructure using a QSFP+ optical link at a rate of 40 Gbps (Each link provides 10 Gbps). The board has a bit error rate of less than 10^{-18} which is approximately 1 error in 1000 days.

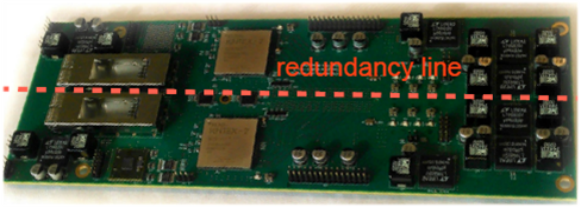


Figure 6: Daughter Board with redundancy line shown.

2.2.4. Super Read Out Driver. The main back-end Read Out Driver (ROD) will be upgraded to receive the increased amount of data. This Super Read Out Driver (sROD) will be the interface between all front and back-end electronics. It will send all Trigger, Timing and Control commands as well as the Detector Control System (DCS) commands to the electronics situated on the detector. The sROD receives and pre-processes the data while storing it in a digital pipeline to wait for the L0/L1 triggering decisions. A prototype has already been built [3]. In order to handle this much data the sROD uses a Virtex7 Field Programmable Gate Array.

Figure 7: Upgraded Read out Driver for the back end electronics.

2.2.5. Back-end Infrastructure. The sROD will be housed in an Advanced Telecommunications Computing Architecture (ATCA) chassis. This is a replacement of the current Versa Module Europa Crates. The ATCA standard will be adopted in ATLAS for the Phase II upgrade in the year 2022 [4]. The ATCA chassis allows intelligent monitoring and control while offering high speed connectivity via a 40 Gbps backplane. Monitoring and Control is achieved via the Simple Network Management Protocol to the Chassis Shelf Manager. The Chassis and all components can be integrated into the existing Detector Control System [5] using a new ATCA-DCS Integration Framework Tool shown in Fig. 8.

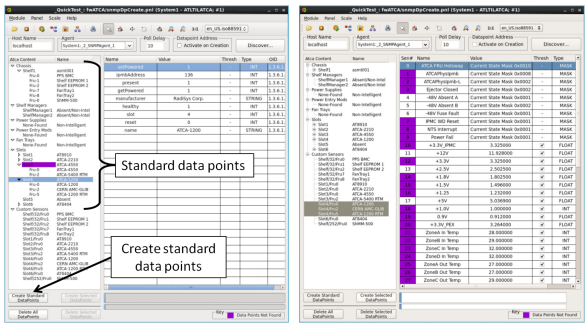


Figure 8: Integration tool to incorporate ATCA Chassis into the Detector Control System.

3. Demonstrator Project

A Demonstrator project [6] has been established in order to test the feasibility and performance of the proposed upgraded electronics. In order to perform the needed tests a prototype hybrid demonstrator will be installed in the detector at the end of 2015. A hybrid between the new

and old read out architectures is needed in order to be backward compatible with the existing system. Figure 9 shows the hybrid readout architecture. The major difference with the hybrid architecture is the analog triggering and the 100 kHz L1A to the sROD. It also makes use of the modified 3-in-1 card but all three will be investigated during beam tests for the final upgrade.

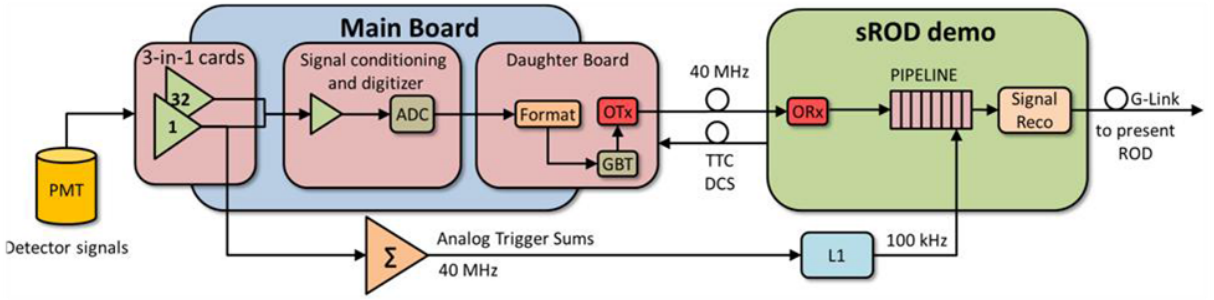


Figure 9: Demonstrator read out electronics.

4. Conclusions

The Phase II upgrade at the LHC will result in an increase in the luminosity by a factor of 5. The associated conditions with such a high luminosity calls for a redesign of the current Tile Calorimeter Readout electronics. The upgrade plan involves the design and insertion of a demonstrator that will evaluate and qualify the proposed upgrade architecture. The demonstrator will completely digitize the signals and transmit them to the back-end at the same rate as bunch crossings (40 MHz). The insertion of the demonstrator will be at the end of 2015.

References

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[3] Carrió F, Castillo V, Ferrer A, Fiorini L, Hernández Y, Higón E, Mellado B, March L, Moreno P, Reed R, Solans C, Valero A and Valls J A 2014 *Journal of Instrumentation* **9** C02019–C02019 URL `http://iopscience.iop.org/1748-0221/9/02/C02019`

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[6] C Bohm on behalf of the ATLAS Tile Calorimeter System 2013 *IEEE Nuclear Science Symposium and Medical Imaging Conference* URL `https://cds.cern.ch/record/1494585/files/ATL-TILECAL-PROC-2012-014.pdf`