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The FE-I4 pixel readout system-on-chip resubmission for the insertable B-Layer project

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The FE-I4 pixel readout system-on-chip resubmission for the insertable B-Layer project

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ABSTRACT: The FE-I4 is a new pixel readout integrated circuit designed to meet the requirements of ATLAS experiment upgrades. The first samples of the FE-I4 engineering run (called FE-I4A) delivered promising results in terms of the requested performances. The FE-I4 team envisaged a number of modifications and fine-tuning before the actual exploitation, planned within the Insertable B-Layer (IBL) of ATLAS. As the IBL schedule was pushed significantly forward, a quick and efficient plan had to be devised for the FE-I4 redesign. This article will present the main objectives of the resubmission, together with the major changes that were a driving factor for this redesign. In addition, the top-level verification and test efforts of the FE-I4 will also be addressed.

KEYWORDS: VLSI circuits; Electronic detector readout concepts (solid-state); Digital electronic circuits

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1 Introduction

The FE-I4 pixel readout design [1] has been implemented in 130 nm technology and is meant for use within future ATLAS pixel upgrades. The chip is capable of coping with high radiation doses (above 250 Mrad) and high hit rates. The samples of the first engineering run (called FE-I4A) have been received in the fall of 2010 and underwent an extensive evaluation and test ever since. Preliminary measurements have been performed on a number of wafers revealing promising results in terms of the LHC pixel detectors performance. The FE-I4 actual exploitation will take place during the next ATLAS shutdown, with the insertion of a fourth pixel layer inside the present pixel detector, the so-called insertable b-layer (IBL) [2]. Due to the somewhat modified ATLAS shutdown timeslot, now planned for 2013, the IBL team had to speed up a number of activities in the agenda. This had a direct consequence on the subsequent production run of the FE-I4 (called FE-I4B), meaning that the submission deadline was pushed forward to summer 2011, leaving barely a few months available for the redesign. Besides choosing and implementing one of the different design options in pixel array and design flaws fixing, the major redesign effort has been driven by new requirements from the ATLAS Data Acquisition Group (DAQ), to allow more flexibility in data stream synchronization. The implied modifications have been also constrained area-wise, primarily to facilitate the top-level integration with the other (unmodified) modules of the FE-I4A. State of the art tools from the appropriate commercial EDA vendors and current industrial practices have been used to set up and execute the design, simulation, verification and test flow and to perform the sign off.

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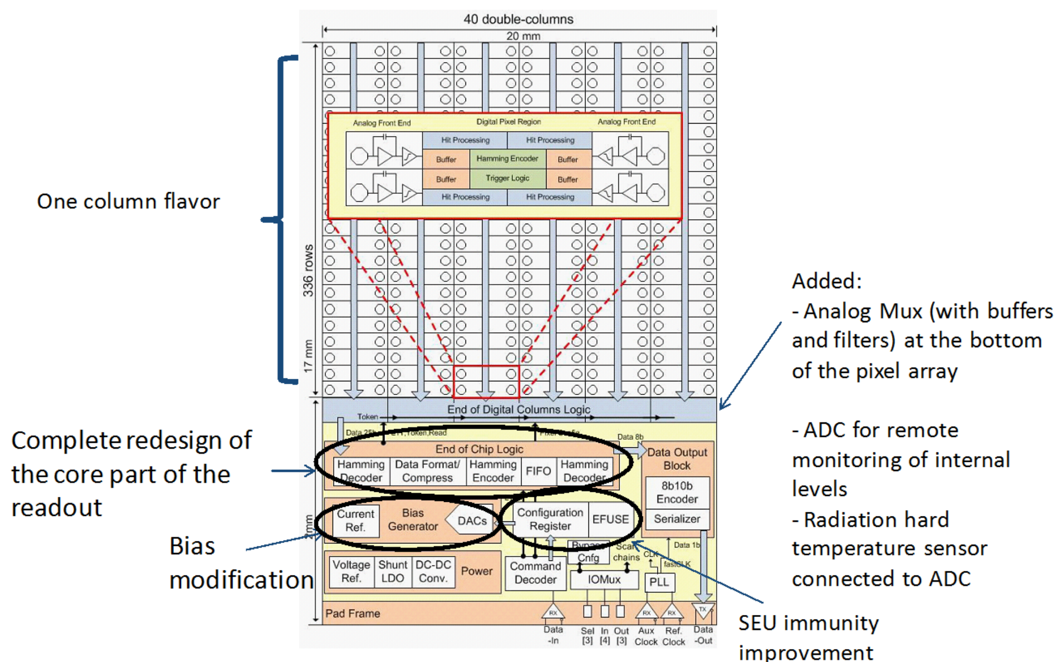

Figure 1. FE-I4A design modification for the FE-I4B submission.

2 The FE-I4 chip

The basic function of the ATLAS FE-I4 chip family is to record the time stamp and the charge of all hit pixels and transfer it outside of the chip [1]. The charge due to the hits are brought to the chip through the coupled external sensors with negative charge collection. The pixels are arranged in the column pairs, which are further divided into 2 by 2 pixel regions. The readout part at the periphery makes extensive use of the triple redundancy to improve the SEU immunity. Figure 1 shows an architecture of the FE-I4A and puts an emphasize on the modified blocks along with the types of modification, resulting in the FE-I4B architecture.

3 Redesign effort in a nutshell

3.1 Prerequisites for the redesign

In order to fit the aggressive resubmission schedule, the changes have been implemented only when they were deemed to be necessary, while staying as close as possible to the FE-I4A version. Adding a new block was justified only in the situation when such an addition by no means compromises the current implementation (this was the case for an ADC and a temperature sensor). While implementing the modifications, backward compatibility with the FE-I4A had to be maintained at every stage of the redesign.

3.2 Major design modifications

The pixel array in the FE-I4A has various column flavours for the sake of evaluation of different implementations. Based on the measurement results of the FE-I4A, one solution for the entire pixel

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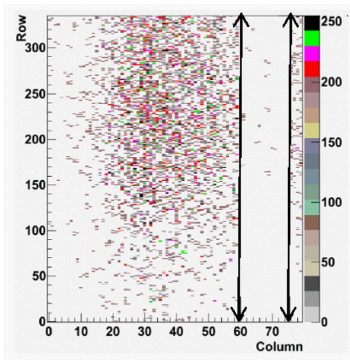

Figure 2. Latch upset map.

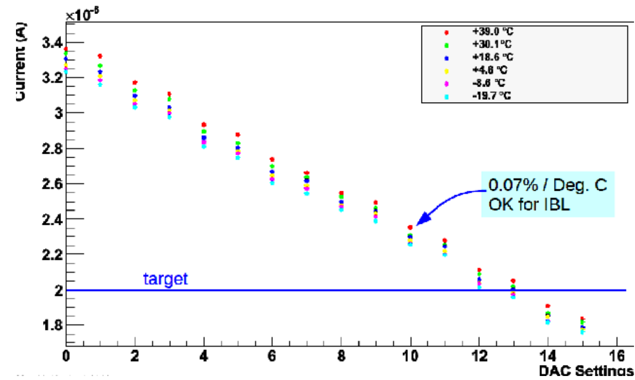

Figure 3. Bandgap current reference measurements.

array has been chosen, summarized in the following:

- All feedback capacitors in the first amplifier stage of the pixel array are unified to metal-to-metal ones as the VNCAPs did not reveal any advantages.

- The pixel memory will make use of the DICE latches with an interleaved layout and a guard-ring [3], as the measurements revealed that they have a far superior performance in terms of SEU compared to the typical DICE cells. These measurement results are obtained with a proton synchrotron (PS) irradiation, and are shown in the figure 2. The columns using the DICE cells with the guard-ring are in the area edged with the arrow lines. The plot is obtained by disabling all pixels in the array and then injecting the charge periodically during the exposure.

- The leakage current during the injection was much higher than expected. To remedy this, all injection transistor switches were replaced with their low-power counterpart from the library, to exhibit smaller sub-threshold leakage current to the ground in the off-state. The simulation showed that the leakage current of the low-power transistors is one order of magnitude smaller compared to the presently used switches.

- The internal nodes of the first pixels in the columns are directed to the pads at the bottom of the chip through analog multiplexers (new blocks). The analog multiplexers are accompanied with buffers and filters and are placed at the bottom of the pixel array.

The measurements had shown that the bandgap current reference had to be readjusted and centered around 2μA (middle DAC settings, figure 3), controlled by the pads. Also, the biasing voltages of the pixel preamplifiers underwent minor modifications, while the safety governor bit was added to the MSB bit of the biasing DAC — to prevent an accidental high current.

The FE-I4B contains two new blocks: a general purpose ADC and a temperature sensor. The ADC has 8 inputs connected to the "points of interests" in the design including the temperature sensor, output of the analog MUX at the bottom of the pixel array, analog ground, etc. Because these new blocks operate rather autonomously, their introduction did not compromise other blocks in the design.

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The core part of the readout, i.e. the End of Chip Logic module (EOCHL) required a complete redesign due to the refined DAQ requirements. These requirements concern the restoration of synchronization between FE-I4 and DAQ detector module in case of an SEU induced configuration failure. The highlights of the new EOCHL in the FE-I4B design are:

- User-programmable Event Size limit function. A 12-bit Event Size Counter (ESC) has been added, counting write cycles to the FIFO. The 8 MSB of this counter are compared to the 8-bit MSBs of the Event Limit register. When they are equal, the readout of this event will be ended. The system will continue with the next L1Req (Data request).
- An Event Count Reset (ECR) has been added to the Read Error Request operation, for the case when the chip is not in the Run Mode. This permits the reset of the EOCHL and digital array before entering the Run Mode so that no random data comes out.
- Bunch and LV1ID counters had to be increased, having a consequence on data header format and additional service records.
- Possibility to suppress duplicate hits coming from the array.

Although the new EOCHL resulted in increased design complexity, while the top-level requirement on layout boundary remained the same, the design team managed to implement the new design meeting both area and timing requirements.

Other modifications of the FE-I4B that will be mentioned here are the configuration register being made more immune to SEU effects (triple redundancy introduced for write logic), and the increase of the threshold level of the prompt radiation burst detector circuitry. This module will be able to reset the configuration memory in the presence of a dose rate exceeding 10^8 Rad/s.

4 Top-level verification and test

Besides the block-level simulations of the modified blocks to verify the new functionality, the FE-I4B design team has put an additional effort to verify the design from the top-level. Two different approaches are used, one being the Open Verification Methodology (OVM), the other is the Mixed-signal top-level verification (figure 4). Both cope with the final chip schematic and are not merely simulations, but they rather link the verification to the subsequent bench-test procedures.

4.1 OVM approach

The OVM is an industry standard adopted by the major EDA players. The suite allows users to write the procedures within the virtual test bench, executing the functions that in reality will be carried out at the bench-test framework designed particularly for the FE-I4 (USBpix or RCE test stands [4]). The commands (stimuli) are processed within the test bench and sent to the model of the chip, while the chip's response is compared to the predefined patterns. The digital part of the chip is modeled with the Verilog netlist, while the analog and mixed-signal part are represented with discrete voltage levels or as black-boxes. The circuit physical parameters, e.g. propagation delay through the interconnecting wires and parasitic capacitances, are extracted from the layout and incorporated into this simulation. The modified blocks, such as the EOCHL and configuration register implementations have been verified in this way.

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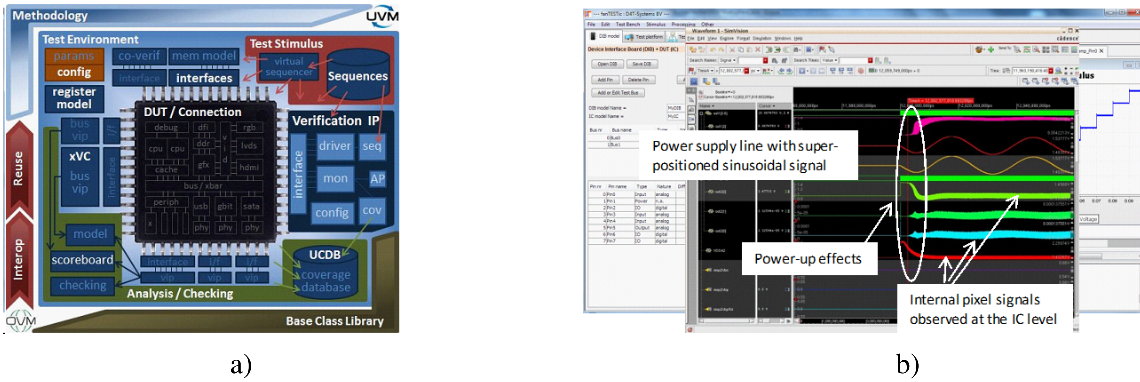
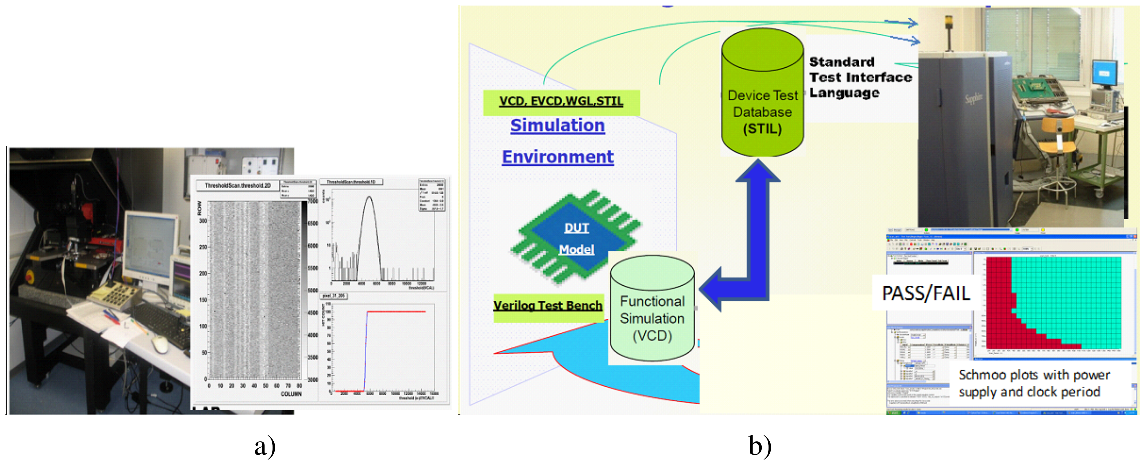


a) b)

Figure 4. Top-level Design Verification a) OVM b) Mixed-Signal top-level simulation charts.



a) b)

Figure 5. a) USBPix Suite b) The infrastructure for structural scan test generation.

4.2 Mixed-Signal approach

The mixed-signal approach complements the OVM digital suite in a way that it tackles the analog signals at the top-level as if the chip was mounted on a bench-test, including the device interface board (DIB). Obviously, the chip could not have been simulated at the full-blown transistor-level netlist. In this case, the parts of the chip had to be replaced with their high-level (RTL Verilog or Verilog-AMS) description or black-boxes if they played no role during a particular functional verification. Nonetheless, the connectivity and the basic functionality of the entire chip are always preserved in this approach. The power-up procedure, the functionality of one pixel within the array and the functionality of the newly added ADC have been verified in such a way. E.g., the waveforms in figure 4b represent the stimuli/response of the top-level FE-I4B output ports after powering-up and the start of the disturbance signal on a power supply.

4.3 Test development

The FE-I4B will undergo a production wafer test upon the final validation. For that purpose, both functional test with the USBPix suite, as well as structural scan test for the digital part of the chip periphery have been foreseen. Figure 5 illustrates both environments. The FE-I4B redesign re-

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quired also a certain effort for the test development, however, this was quick and straightforward in case of the structural scan test, because of the reusable Design-for-test infrastructure being implemented in the FE-I4A [5]. It took not more than two days to deliver and verify the test patterns with the mixed-signal top-level simulation, as if they were running on the tester platform (Credence, figure 5b).

5 Conclusion

The FE-I4B has been taped out in September 2011, less than 6 months from the project kick-off. Despite the accelerated schedule that was brought by the IBL's decision to go for a fast-track to accommodate the updated agenda of LHC shutdown period, the IBL community is confident that their schedule will be met and that the FE-I4 chips will be inserted in the B-layer in 2013.

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