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Towards a Level-1 tracking trigger for the ATLAS experiment at the High Luminosity LHC

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ABSTRACT: At the high luminosity HL-LHC, upwards of 140 individual proton-proton interactions (pileup) are expected per bunch-crossing at luminosities of around 5×10^{34} cm^{-2}s^{-1}. A proposal by the ATLAS collaboration to split the ATLAS first level trigger in to two stages is briefly detailed. The use of fast track finding in the new first level trigger is explored as a method to provide the discrimination required to reduce the event rate to acceptable levels for the read out system while maintaining high efficiency on the selection of the decay products of electroweak bosons along with other high p_{T} physics signatures at HL-LHC luminosities. It is shown that the available bandwidth in the proposed new strip tracker is sufficient for a region of interest based track trigger given certain optimisations. Further methods for improving upon the proposal are discussed.

KEYWORDS: Particle tracking detectors (Solid-state detectors); Performance of High Energy Physics Detectors; Trigger concepts and systems (hardware and software).

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Contents

1. Introduction

Over the period 2010–2012, the LHC [1] delivered over 20 fb^{-1} of integrated luminosity to the ATLAS [2] and CMS [3] detectors at $\sqrt{s} = 7$ and 8 TeV. Analysis of this dataset has resulted in the discovery of a Higgs-like boson and over 300 publications by ATLAS. Despite these successes, many physics channels remain statistically limited as through the collision of composite protons, the physics reach of the LHC at a given energy point is determined by the parton luminosity. For increasingly large particle masses, the corresponding parton luminosity is small requiring large datasets in order to observe possible new physics in low cross section processes. The current LHC programme is expected to deliver 300 fb^{-1} by 2019 at which point the machine and detectors will undergo major upgrades for the HL-LHC project [4]. This is expected to run between 2023-2033 and amass a dataset of 3000 fb^{-1}. This significantly larger dataset will yield improved statistical precision on Higgs decay modes with small branching ratios and extensive searches for new signatures predicted by SUSY models at multi-TeV energy scales [5].

Higher instantaneous luminosity are to be attained in part through manipulation of the beams with crab cavities, this will result in an increased number of individual pp interactions occurring per bunch-crossing, referred to as pileup. At HL-LHC luminosities of 5×10^{34} cm^{-2}s^{-1}, the mean number of pileup interactions per bunch crossing $\langle \mu \rangle$ is expected to to be ~ 140.

Retaining a high efficiency on the selection of $W^{\pm}$ and Z decays is vital for an experiment probing electroweak physics such as ATLAS. Upon extrapolation, the expected rate of electron and muon candidates passing the current first level (L1) trigger is of the order 150 and 50 kHz, respectively, whereas the planned overall trigger budget (including all other physics signatures, jets, τ, $E_{\mathrm{T}}^{\mathrm{miss}}$) at L1 during the HL-LHC is around 200 kHz.

The current event discrimination at L1 is based on low-granularity calorimetric information and fast muon systems which both use custom electronics to issue a L1 trigger decision within 2.5 μs. Tracking information from the Inner Detector (ID) is only available in the software based High Level Trigger (HLT) once the entire detector front end has been read out.

In this document, the methodologies and feasibilities regarding the use of tracking information at L1 to improve lepton discrimination and hence reduce the L1 rate are discussed.

2. The New L0 and the L1 Track Trigger

In order to obtain increased rejection power before the full detector readout is requested, it is envisaged to add a new L1 hardware layer to the trigger, with the current L1 being re-designated to L0. L0 will operate with an increased latency window of 6 μs and rate of $\sim$ 500 kHz while the L1 decision will need to be broadcast within 20–30 μs at around 200 kHz to stay within the constraints of legacy muon electronics whose replacement is not certain due to their inaccessible location inside the toroidal magnet systems.

A key proposal for this new design is the inclusion of a L1 track trigger (L1TT). Using technologies similar to ATLAS Fast Tracker project [6], L1TT will utilise track pattern banks to quickly (around 6 μs) identify particles with $p_{\mathrm{T}} \gtrsim 2$ GeV based upon supplied hits from the new Inner Tracker (ITK). Studies have shown that even for modest track reconstruction resolution, the matching of e and τ candidates to the calorimeter and μ candidates to the muon spectrometer will reduce rates by a factor 3–10 with only small ($\sim$ 10%) losses in efficiency [5]. Such additional rejection could not be obtained by continuing to use only muon trigger chambers and low granularity calorimeter information at L0/L1.

3. ATLAS Inner Tracker project

The full ATLAS ID will need to be replaced for the HL-LHC due to radiation damage and to cope with the increased occupancy. A fully silicon design is proposed whose baseline layout consists of 4(6) pixel layers and 5(7) strip layers in the barrel(end-cap), respectively. An eight fold increase in the number of pixels and twelvefold increase in the number of strips will result in an occupancy less than 1% through the ID for the extreme case of $\mu = 200$ [5].

The readout for the new pixel detector is based on the FE-I4 integrated circuit (ASIC) most recently used in the ATLAS insertable b-layer project [7]. This chip supports multi-MHz full detector readout which exceeds the requirements of the default L0/L1 strategy.

The front-end readout chip for the strip detector is the ABC130, an ASIC using a 130 nm CMOS process. The first revision of this chip was received for testing in late 2013. In the barrel, ten ABC130 chips are to be mounted per hybrid and for the studies presented these communicate to a Hybrid Chip Controller via two daisy chains of five chips, each running at 160 Mbps. Bi-directional readout adds redundancy and protect against chip failure by allowing ABC130s upstream of a chip failure to be addressed in the opposite direction.

The design of the HCC is not yet finalised and flexibility regarding its functionality is still possible. Each HCC will communicate at 160 Mbps to the End of Stave (EoS) where data are transmitted via a Multi-Gigabit Transceiver (GBT) link, in addition HCC prioritisation is possible

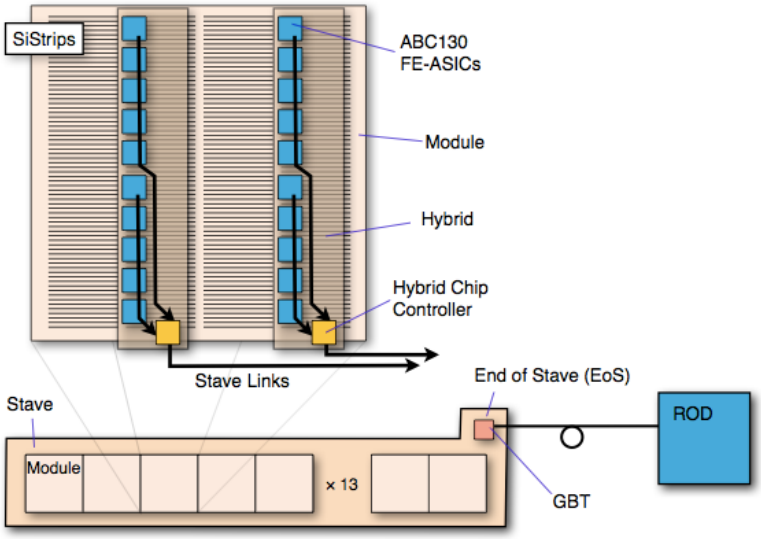

Figure 1. Design proposal for a ITK strip module. Front-end ABC130 ASICs are connected via daisy-chains of (typically) 5 chips to their HCC, data are read from the HCC to the EoS links where packets are transmitted either to L1TT or to the read out system over GBT links.

for data packets destined for L1TT over packers for L1 full-readout. This design is summarised in Figure 1.

4. Data Flow in L0 and L1

In the baseline proposal, data are initially processed at a coarse granularity in the muon sector logic and L0 calorimeter triggers, these supply Regions of Interest to the L0 central topological trigger. For events passing the L0 logic, an L0 accept is broadcast to the detector front end and L1 trigger systems.

In the ITK strip detector, data are moved from synchronous primary buffers clocked at the 40 MHz bunch crossing rate to asynchronous secondary buffers while the L1TT maps calorimeter and muon RoIs into Regional Readout Requests (R3s). These R3s are broadcast to the ITK front end where data fragments addressed to the R3s are read from the secondary buffers and transmitted to the L1TT. The data are matched to the L1TT pattern banks and found tracks are delivered to the L1 central trigger processor. Here the final L1 decision is made using full granularity calorimeter information, refined muon information and the L1TT tracking information. Upon issue of a L1 accept, all data for the event is read out from the front end. In the ITK strip detectors the data are fetched from the secondary buffers. This system is illustrated in Figure 2.

5. ITK strip readout latency simulation

The practicality of the ITK strip detector configuration is investigated using discrete event simulation [8]. Hits are distributed in a simulated ITK strip detector according to the expected occupancy for $\mu = 200$ with a 25 ns LHC fill pattern. For each L0 accept, it is assumed that 10% of the ITK

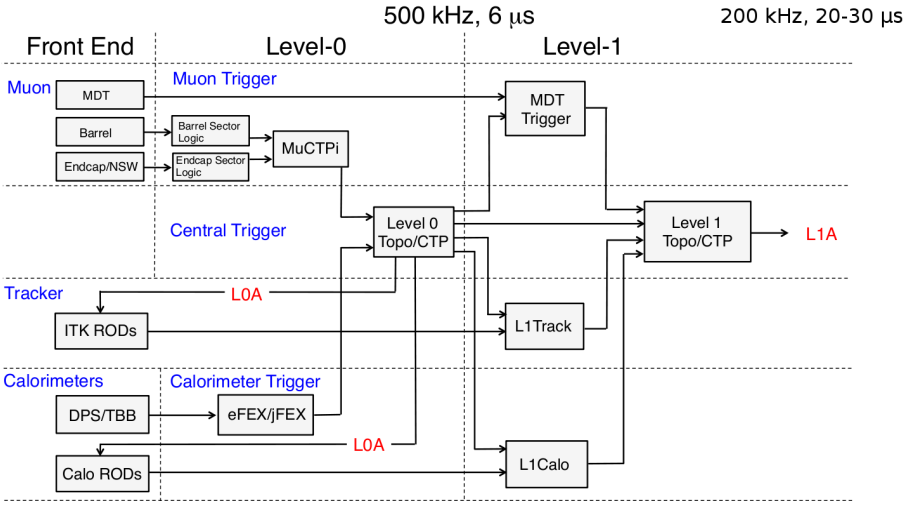

Figure 2. Baseline layout of the split L0/L1 ATLAS HL-LHC trigger. Data from RoI passing the L0 trigger are supplied from the ITK to the L1TT allowing for fast track finding.

will be read out into L1TT in R3s. The latency to readout 95% of data packets for all R3s was investigated. For the inner strip modules (with highest occupancy), prioritisation of R3s on the HCC was shown to enable 95% R3 readout within 6 μs up to an L1 rate of 240 kHz. This configuration is however insufficient for mid-petal end-cap hybrids where up to 12 ABC130 chips per module results in rings 4–6 possessing six chips in at least one daisy chain. The 95% R3 latency for the worst performing "Hybrid6" is observed to always exceed the nominal 6 μs latency budget for an L1 rate $>$ 100 kHz, with a non-linear dependence on the L1 rate. The parameter space for the end-cap Hybrid6 is investigated in Figure 3 as a function of both the L1 and R3 rates [8]. The nominal configuration lies in a unstable region with very little flexibility to increase either rate without causing unacceptable increases in latency. This is mitigated by reading out the ABC130 chips in both directions (four effective daisy chain links, this results in a maximum bandwidth of 640 Mbps between the ABC130s and their HCC) and by doubling the HCC to EoS link speed to 320 Mbps for this hybrid. With these changes, sub 6 μs are restored over the entire considered parameter space.

6. Alternative design proposals

Alternative connectivity of the HCC chips to their ABC130 readout chips is under investigation. A star network layout for example would only require two more differential links from the HCC than the current proposal. By directly connecting the ABC130s to the HCC and moving packet building to the HCC, larger packets are built with data from multiple ABC130s. This will minimise header information and allow a larger fraction of the packet to be used in delivering the data payload. Compression techniques are also more effective on larger packets and together this may make more optimal use of the available bandwidth.

Other design proposals include a self-seeded mode of operation able to locate tracks without using RoIs. Massive data reduction is required on the front end to stay within bandwidth limitations and therefore only hits from tracks with $p_{\mathrm{T}} > 20$ GeV are read out. Data reduction methods include

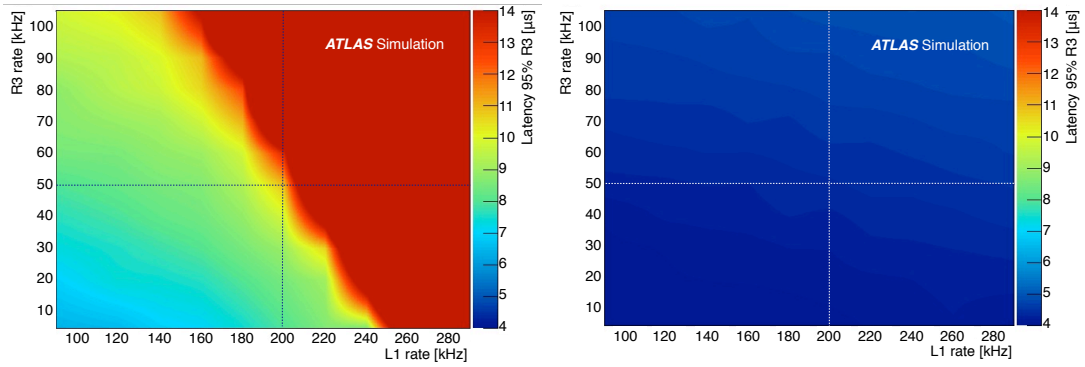

Figure 3. Latency to read out 95% of all R3 packets for the worst performing end-cap "Hybrid6" as a function of both the L1 and R3 rates (R3 rate here is 10% of the L0 rate) for the standard configuration with HCC prioritisation, a 32 deep HCC FIFO, two daisy chain links per HCC and a 160 Mbps link to the EoS (left) and for the similar case but with four (two bi-directional) daisy chain links and a 320 Mbps link (right). Nominal configuration denoted by dotted lines.

a fast cluster finder built into the ABC130 chips to locate high p_{T} particle hits through correlation between the top and bottom stave layers.

7. Conclusion

Work is ongoing to profile the requirements and expected performance of different architectural designs for the ATLAS trigger in the HL-LHC. It is shown that based on discrete event simulation, the baseline ITK strip detector will not exceed the available bandwidth for a 500 kHz L0 fractional readout of 10% of the ITK in RoIs and a 200 kHz readout rate of the entire ITK.

Other readout proposals, such as a seed-less design forgoing the RoI approach and optimisations of the RoI approach at the packet building level are in addition being investigated.

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