PROCEEDINGS OF SCIENCE

Firmware development and testing of the ATLAS IBL Read-Out Driver card

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The ATLAS Experiment is reworking and upgrading systems during the current LHC shutdown. In particular, the Pixel detector is inserting an additional inner layer called Insertable B-Layer (IBL). The Read-Out Driver card (ROD), the Back-of-Crate card (BOC), and the S-Link together form the essential frontend data path of the IBL's off-detector DAQ system. The strategy for IBL ROD firmware development focused on migrating and tailoring HDL code blocks from Pixel ROD to ensure modular compatibility in future ROD upgrades, in which a unified code version will interface with IBL and Pixel layers. Essential features such as data formatting, frontend-specific error handling, and calibration are added to the ROD data path. An IBL DAQ testbench using a realistic frontend chip model was created to serve as an initial framework for full offline electronic system simulation. In this document, major firmware achievements concerning the IBL ROD data path implementation, tested in testbench and on ROD prototypes, will be reported. Recent Pixel collaboration efforts focus on finalizing the hardware and firmware tests for IBL. The time plan is to approach a final IBL DAQ phase by the end of 2014.

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1. Introduction

The Large Hadron Collider (LHC) at CERN is currently undergoing a long shutdown. During this phase a fourth silicon Pixel layer called the Insertable B-Layer (IBL) had been successfully installed as the new innermost detector layer of ATLAS [1]. This detector layer uses a new generation of hybrid pixel detector in order to overcome the readout inefficiency suffered by existing Pixel layers at higher LHC energy levels and luminosity. IBL's front-end readout ASICs (FE-I4 [2]) provide larger active areas and a higher readout bandwidth. A new off-detector readout system was designed for IBL to accommodate higher bandwidth requirements and new DAQ electronics were built [3]. By adopting up-to-date processors and a novel calibration methodology, the readout electronics for IBL have become highly integrated and offer enhanced performance compared to their predecessors used for the Pixel DAQ. The DAQ components for IBL are described in the following section.

2. Trigger and DAQ system for IBL

The IBL data acquisition is managed by the ATLAS Trigger and DAQ system (TDAQ) along with other Pixel layers [4]. The TDAQ structure of the IBL is shown in figure 1. The Level-1 TDAQ for IBL is a VMEx64-based system consisting of 15 pairs of new Read-Out Driver (ROD) and Back-of-Crate cards (BOC) (14 for IBL staves, 1 for Diamond Beam Monitor), a Timing-Trigger-and-Control Interface Module (TIM), and a Single Board Computer (SBC). The ROD is

the main off-detector readout and control processor unit. The BOC is the electrical-optical converter card interfacing between the ROD and an IBL stave [5]. The high-level interaction between a ROD, a BOC, and an IBL stave is illustrated in figure 2. In addition to the new off-detector readout electronics, the DAQ system uses an external server farm (FitServer) for fitting and data analysis during detector calibration.

During LHC operations, Level-1 triggers are sent to the IBL staves to retrieve events at a rate of 100 KHz, and serialized hit data is returned from the front-end to the off-detector ROD-BOC at 160 Mbps per link. Hit data comprises the hit location - row and column numbers of the pixel matrix, and a 4 bit timer-over-threshold (ToT) value corresponding to the hit energy. After front-end data is processed by ROD-BOC, it is sent to the Readout Buffer Input cards (ROBIN) in the Readout Subsystem (ROS) via S-Link[1] interface awaiting Level-2 triggers and further processing. The desired data for analysis at this level is selected based on regions of interest (ROI), defined by Level-1 tagged features. Level-2 triggers request ROI data for all ATLAS detectors to be retrieved from the ROBINs and send data to a higher level event building server farm. After ATLAS-wide events have been built, they are selected by Level-3 triggers for the final "raw data" storage.

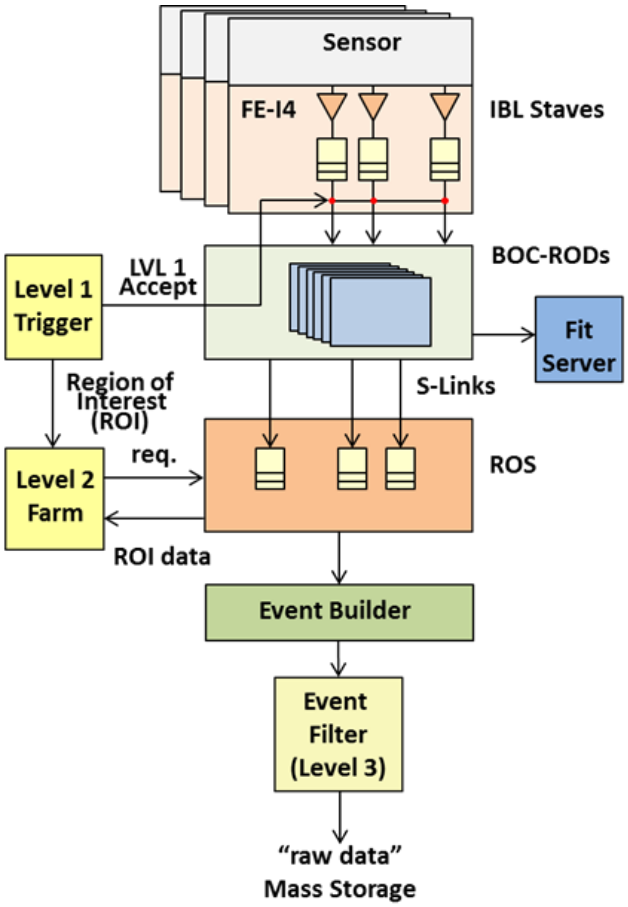

Figure 1: Overview of the ATLAS Trigger and DAQ system for IBL

[1] S-Link: CERN's custom data transmission protocol based on a FIFO-like user interface

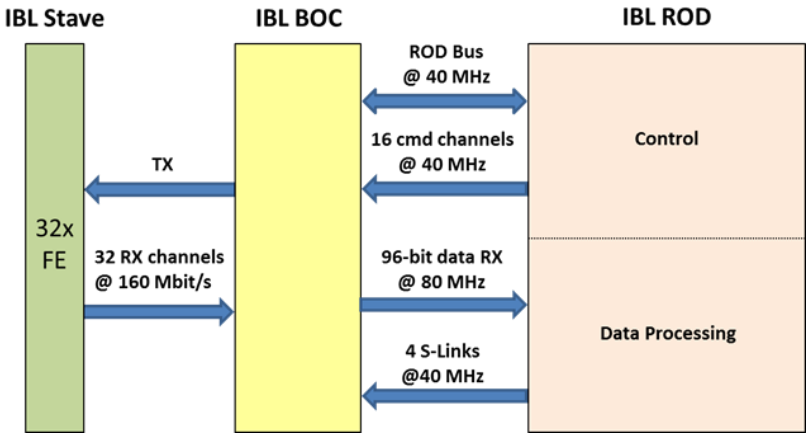

Figure 2: ROD-BOC-IBL communication diagram. The IBL BOC recovers and decodes 8b/10b serial data from the front-end and send byte-level-multiplexed (in groups of 4 FEs) to the ROD on eight 12-bit buses.

3. IBL ROD card

The new IBL ROD card is shown in figure 3 [6]. It is based on the previous Pixel ROD, but is now equipped with modern FPGAs for detector control, calibration, and readout data processing. The main FPGAs on the ROD include a Xilinx Virtex-5 FPGA (master) and two Xilinx Spartan-6 FPGAs (slaves). Each slave FPGA implements the ROD datapath and receives data from the corresponding slave FPGA on the BOC. An embedded PowerPC (PPC) on the Virtex-5 is used to control ROD operations. The master and slave FPGAs are equipped with Gbit Ethernet for control and data transfer at higher rates compared to the VME, which is limited at 7 Mbyte/s.

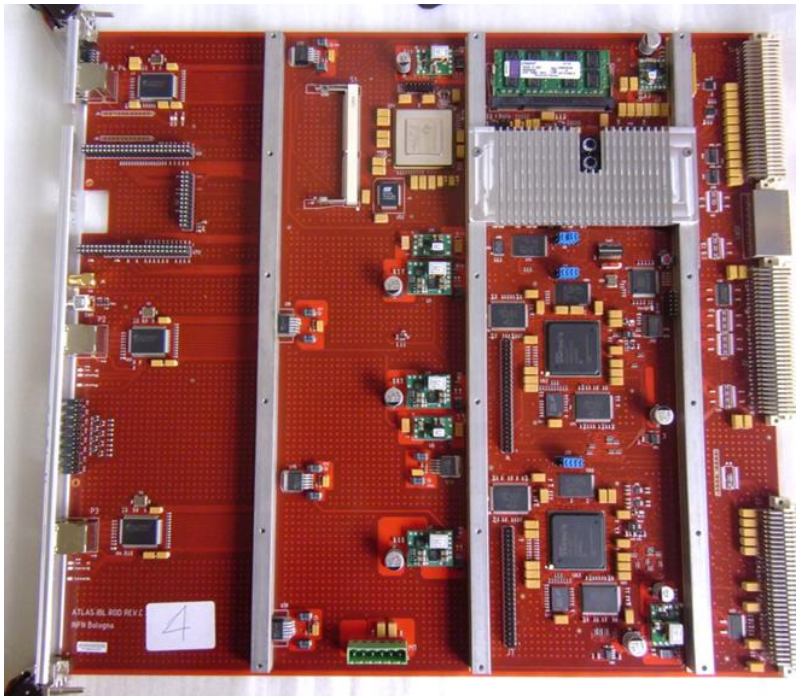

Figure 3: Photo of a RevC IBL ROD card equipped with Gbit Ethernet for the main FPGAs

4. IBL ROD firmware structure

4.1 Control and data flow

The high-level ROD control signal and data interactions are shown in figure 4. When the ROD is operating in calibration mode, the PPC configures the histogrammer and executes calibration scans to the detector stave. During normal data-taking mode the triggers are distributed by the TIM. The ROD asserts a busy signal to the trigger system when data backpressure from S-Link or internal buffer overflow occurs inside the ROD slave.

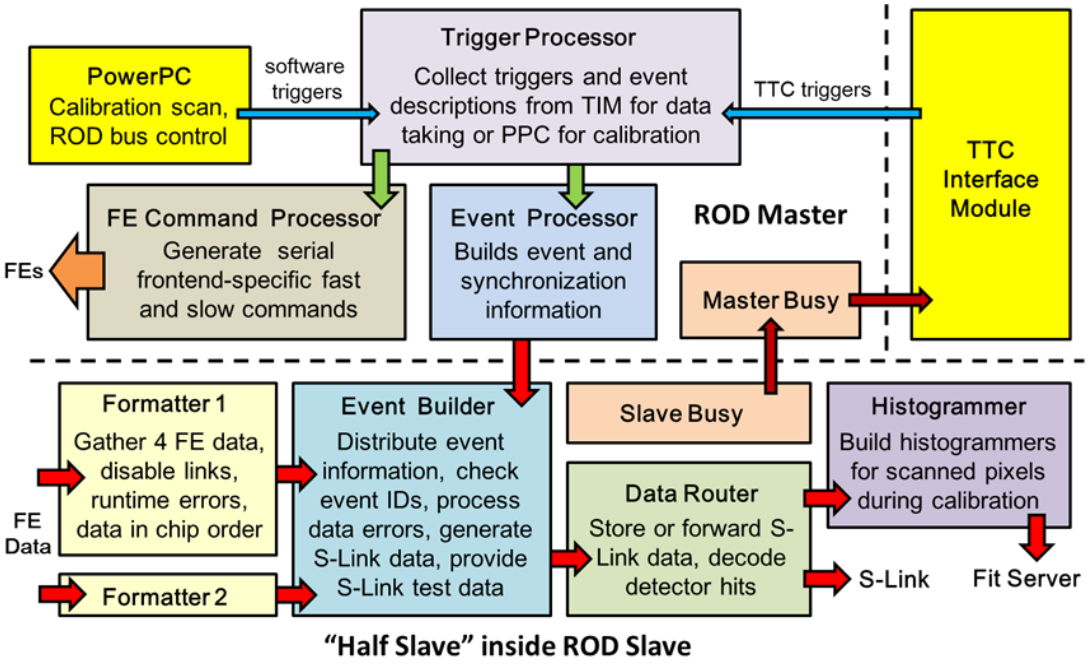

Figure 4: High level view of ROD data-taking operation.

4.2 Detector calibration

The goals of detector calibration are to set uniform readout thresholds in all channels as well as reject noisy readout cells prior to real LHC data-taking. Each ROD slave FPGA implements two histogrammer blocks. A single histogrammer is used to generate per-pixel histograms of occupancy, the ∑ToT, and ∑ToT² values necessary for fitting analysis. Each histogrammer handles up to eight FE-I4s with a total of 215,040 pixels; it stores and updates the computed histograms in the external SSRAM. When a histogram build is completed, the embedded MicroBlaze microprocessor in the ROD slave transfers the results through direct memory access (DMA) to the external DDR2-RAM and further transfers the histogram off to the FitServer via TCP/IP. Currently the ROD can perform histogram updates at a speed of 100MHz, using the logic shown in figure 5.

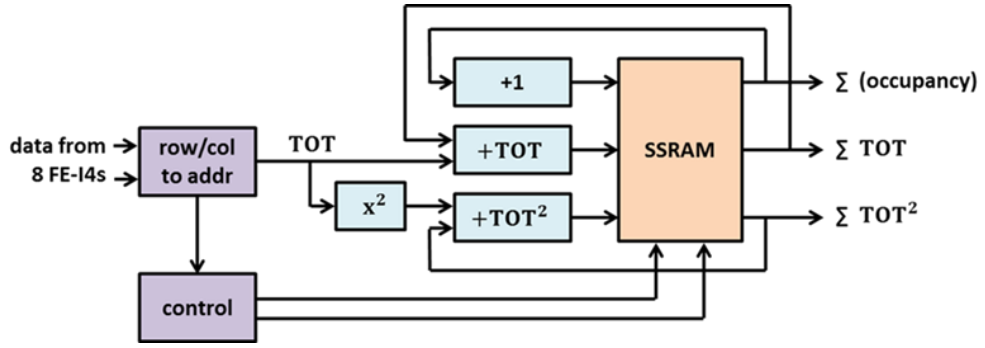

Figure 5: High level view of ROD histogrammer operation.

4.3 Slave firmware layout

Figure 6 shows the official firmware layout inside a ROD slave FPGA. It represents a ROD datapath that can handle data from up to 16 FE-I4s in parallel. The firmware design consists of highly modular VHDL code blocks. The slave datapath processes data in real time at 80 MHz and utilizes many de-randomizing buffer elements within its design.

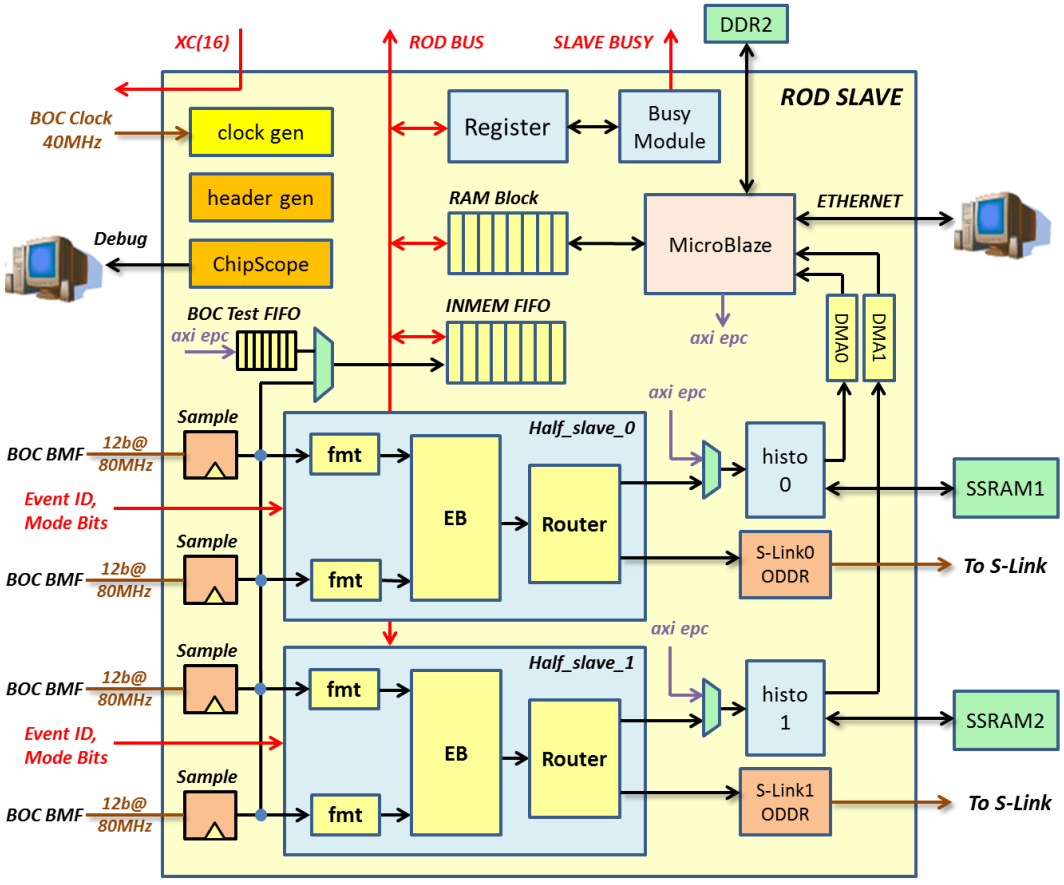

Figure 6: Schematic layout of the IBL ROD slave firmware [7]. The red lines represent signals between ROD slave and master. The brown lines represent interacting signals between ROD slave FPGA and BOC slave FPGA.

5. Datapath simulation and firmware testing

5.1 Testbench simulation with realistic front-end model

Since real FE-I4s and readout hardware are scarce among developers, a ModelSim testbench implementing a single realistic FE-I4 model and the ROD slave firmware has been realized. The front-end model was synthesized from the HDL codes used during the FE-I4 development. This testbench setup, shown in figure 7, concerns only the off-detector readout datapath without the TIM and ROD master. All FPGA embedded software components were excluded in order to reduce simulation time. Due to the limited memory of the machine used for simulation, only one realistic FE-I4 model was used. Its serial data output was replicated 16 times by the simplified BOC firmware to provide full data inputs to a ROD slave. The 8b/10b decoder and the BOC-to-ROD multiplexer block provided sufficient BOC slave functionality. In addition to datapath firmware, two VHDL packages were created to accommodate the ROD control path in the absence of the ROD master firmware and the PPC.

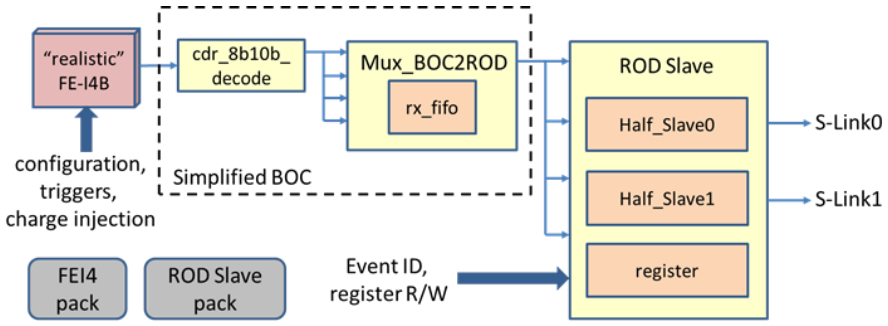

Figure 7: Testbench setup used to verify ROD slave datapath functionality.

The FE-I4 model can be triggered under several modes. It is also capable of generating service records which are not available in existing front-end data emulators. Figure 8 illustrates the response of the model under different trigger stimuli. The Level-1 event counter inside the model worked as expected in the normal Level-1 Accept trigger mode and in the external trigger mode. Figure 9 shows the correct S-Link data generated by the slave Event Builder and decoded hits from a single digital time-over-threshold injection (5 enabled Formatter links) at the output of the slave Router.

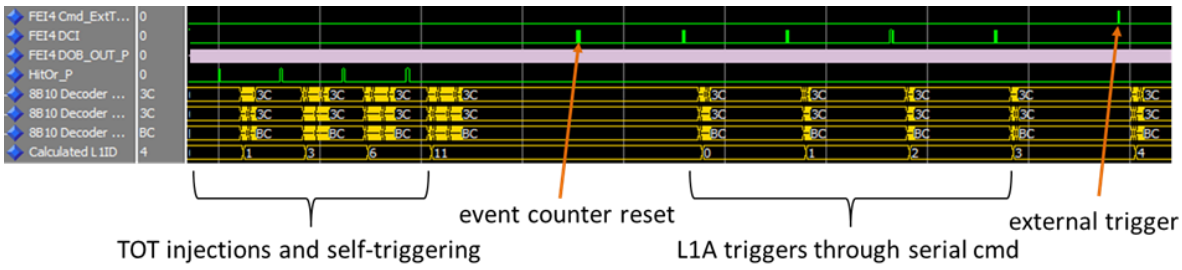

Figure 8: The realistic FE-I4 model responds to different triggering modes that are available.

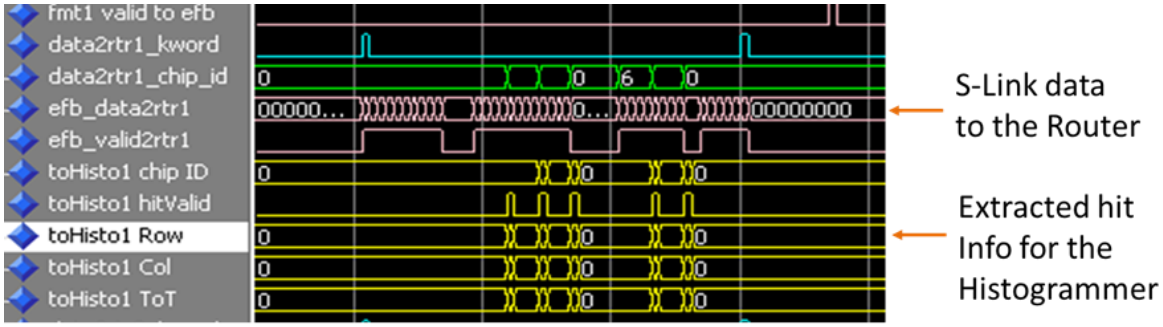

Figure 9: S-Link data generated from injected TOT for 5 enabled front-end links at the output of the Event Builder (pink signals). Hit information decoded from the S-Link data and forwarded to the histogrammer (yellow signals).

5.2 Readout chain tests

Hardware testing including the ROS input buffer hardware ROBIN was also performed for the datapath firmware at CERN. Two different data sources were used during the ROS readout chain test: S-Link test data generated by the ROD slave, and the FE data emulators located on the BOC slave FPGAs. The readout chain of this test involves the TIM, BOC, ROD, S-Link, and ROBIN. In the case of readout tests using emulated FE data, TIM triggers were sent to all 32 simple FE-I4 emulators inside the BOC. While the readout electronics can process triggers at a rate greater than 200 kHz during the test, event arrivals to ROBIN at such a rate quickly resulted in buffer overflows. Eventually, a successful ROS readout test for 16 million emulated events at a triggering rate of 50 kHz was conducted. No data corruption was observed by the ROS. Since the IBL off-detector electronics must produce S-Link data in the same way as the Pixel readout, the ROS readout tests could ensure the correct IBL integration into the ATLAS Experiment.

6. Conclusion

In conclusion, the major firmware blocks for the IBL ROD are in place. By adopting modern FPGAs as front-end data processors, the new ROD was able to achieve higher levels of integration compared to the Pixel ROD. The ROD datapath functions have been verified in a simulation testbench that implemented a realistic FE-I4 model, as well as in hardware readout chain testing. At the present moment, developments of advanced features in ROD and their testing are ongoing for the IBL DAQ community. Next steps in the ROD development will include the firmware adaptation for reading out other Pixel layers and creating built-in tests for datapath diagnosis.

Acknowledgements

We would like to thank the FE-I4 developers for providing the front-end source code as well as colleagues who helped putting together the FE-I4 model.

References

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