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Tests of the First Three-Dimensionally Integrated

Maj,P (AGH) *et al*

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Tests of the First Three-Dimensionally Integrated Chip for Photon Science

P. Maj[1] G.Carini[2], G. Deptuch[3], P. Grybos[1,], P. Kmon[1], D. P. Siddons[4], R. Szczygiel[1], M. Trimpl[3], R. Yarema[3]

[1]*AGH University of Science and Technology, Krakow, Poland*
Al. Mickiewicza 30, 30-059 Krakow, Poland
E-mail: piotr.maj@agh.edu.pl,
[2]***SLAC, Menlo Park, CA, USA***
[3]***FNAL, Batavia IL, USA***
[4]***BNL Upton NY, USA***

We report on the results from testing of the first three-dimensionally integrated readout chip for pixel detectors, which application is in X-ray Photon Correlation Spectroscopy (XPCS) experiments on light sources. The chip was designed in the 130nm Tezzaron/GF process as a two-tier device with effectively 12 metal layers of routing. It counts about 1,700 transistors in total in 80x80um^2 pixels. The chip explores broadly the benefits of the 3D integration for pixel detectors, like full separation of analog and digital parts by placing them accordingly on distinct tiers, improved power distribution by using back-side located pads and almost no periphery for achieving 4-side buttability. VIPIC1, as that is the name of the chip, was designed by FNAL in collaboration with AGH-UST. The tests are underway on the singulated devices from the first successfully bonded wafer pairs. Correct operation of all components tested so far was observed. This includes: full sparsified readout that is based on a priority encoder, pipelined in-pixel hit acquisition with two alternately switched event counters, programming interfaces for permanent setting and disabling of a pixel and acquisition of hits from the analog part with full sensitivity to settings of discriminator thresholds. Current work is focused on measurements of pixel-to-pixel deterministic offsets, electronic noise and calibration of gain using injection of test charges. Every pixel features multiple connections across two-tier boundary. No faults were observed in the 3D bonding interface as well as the connectivity carried by through silicon vias was observed to be achieved on all dies that were qualified as good after wafer thinning. Despite of the long waiting for the first 3D chips, the test results are encouraging for the three-dimensional integration technology as a cost and performance efficient alternative to the aggressive node down scaling.

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1. Introduction

A Vertically Integrated Pixel Imaging Chip, called VIPIC [1], was designed for X-ray Photon Correlation Spectroscopy (XPCS) experiments at synchrotron light sources. The chip is therefore optimized for a small pixel size of 80 μm x 80 μm and it provides fast readout (time resolution in continuous, dead-time-less readout equals to 10 μs).

VIPIC was designed in collaboration with Fermi National Accelerator Laboratory (FNAL) and it was fabricated in a Multi-Project Wafer (MPW) run using the 3D-IC technology provided by Tezzaron Semiconductor. Digital and analog tiers were processed on a standard 0.13 μm bulk CMOS process with 6 metal layers and the 3D integration was done by Tezzaron Semiconductor and Ziptronix. Successfully connected chips were available in Jun 2012.

2. Design

VIPIC consists of two tiers designed in a standard 0.13 μm technology process. Through Silicon Vias (TSVs) are 6 μm deep, 1.3 μm in diameter and the minimum spacing between them is 3.8 μm. The wafers are vertically connected using copper fusion bonding technology using a properly designed pattern of small-size dots on the metal 6 layer, which forms a bonding interface between the tiers. The core of the VIPIC chip is a matrix of 64 x 64 pixels with 80 μm x 80 μm pixel size. The analog and digital blocks are placed on separate layers to effectively limit crosstalks from the digital blocks to the analog front-end. The analog tier contains a matrix of 64 x 64 pixels with analog blocks (CSA, amplifiers, discriminator and trim DAC) and the digital tier contains a matrix of 64 x 64 pixels with digital blocks (and additionally the digital input-output periphery). There are 15 (some of them are differential) connections between the tiers in each pixel to distribute the power supply, bias references, data for register settings and the discriminator output. All these connections are doubled for better yield.

2.1 Analog

The analog front-end (Fig. 1) consists of:

- two charge sensitive amplifiers (CSA and CSA_REF),
- two AC coupled stages of amplifiers (AMPI and AMP II),
- one discriminator DISCR with differentially applied threshold.

There are additional blocks like TRIM DAC, to equalize thresholds on an individual pixel basis, a charge injection circuit, and analog reference blocks. The configuration register allows setting the feedback resistance, switching on and off the differential operation of the input stage and correcting the effective discriminator threshold.

2.2 Digital

As far as the organization of the digital side is concerned, the chip is divided into 16 groups of 4 x 64 pixels (Fig. 2). Each of these groups consists of a sparsifier, a serializer and an LVDS output driver working with the frequency of up to 100 MHz. The readout within each group is zero-suppressed. The sparsification circuitry (similar to one used in the Mephisto chip

[2]), allows a dead-time free readout. Each pixel contains a 5-bit long counter, which is designed for the operation at a high frame rate and therefore it should not overflow at the nominal operation of 10 µs per frame. The chip is specified to cope with 10 µs readout time at the mean occupancy of 3.8 x 10^8 photons / cm^2 / s.

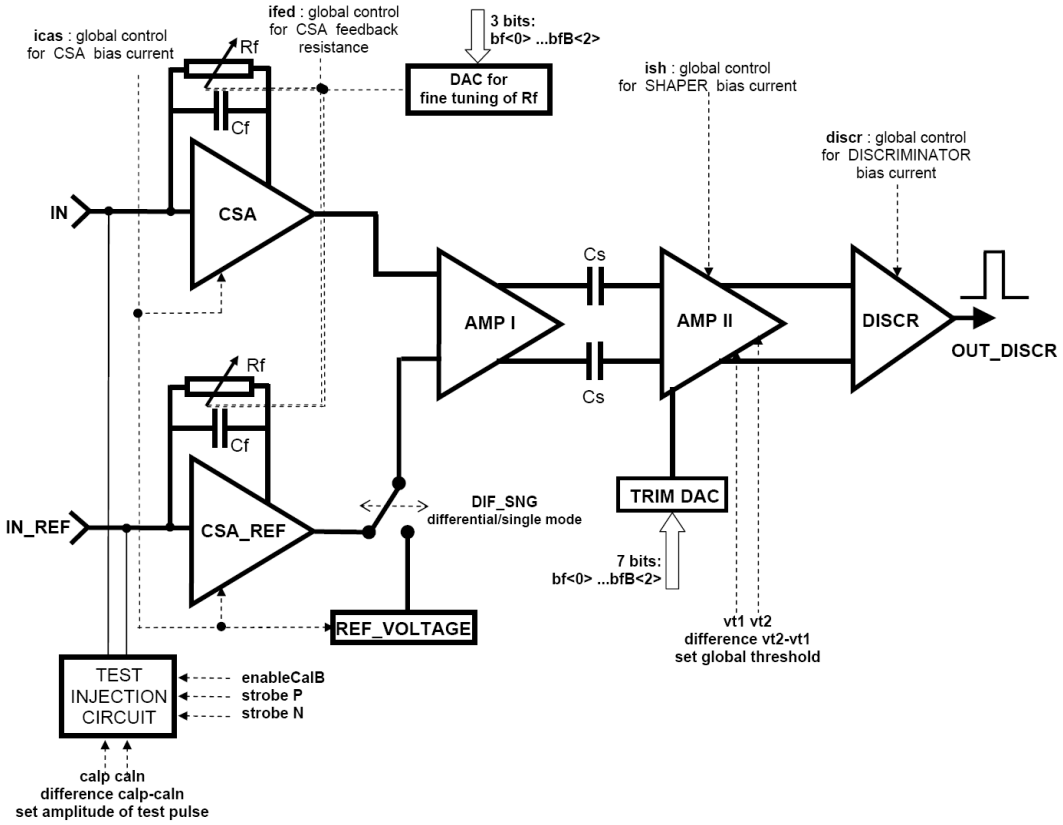


Figure 1. Schematic diagram of the analog blocks of a single pixel

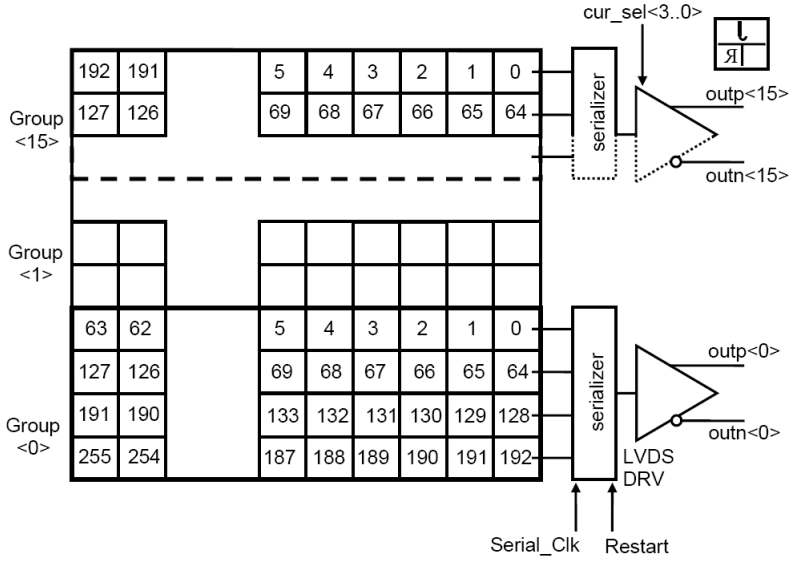
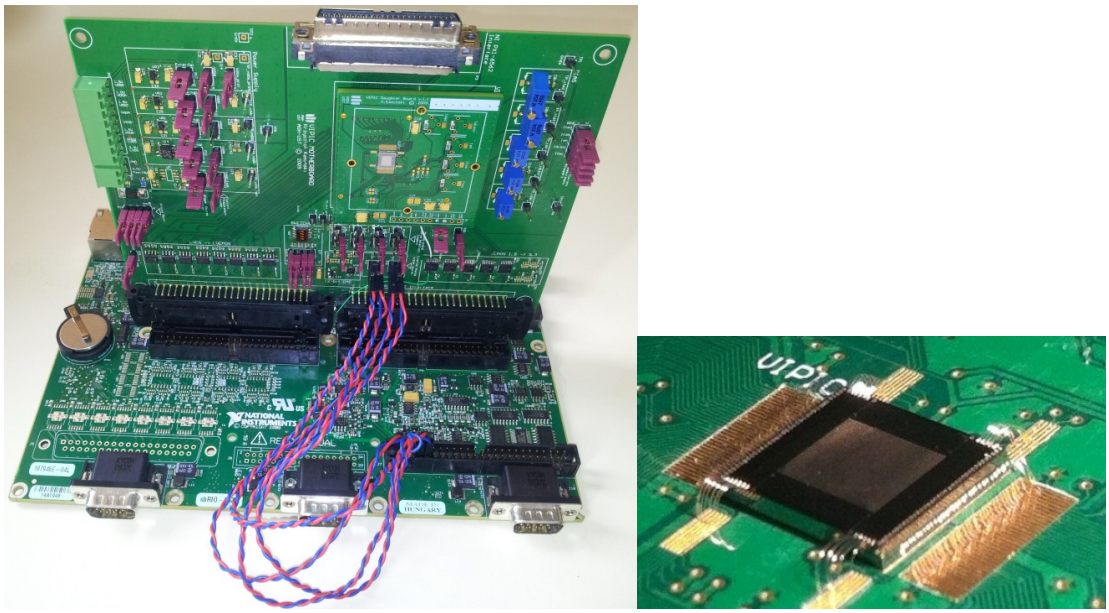


Figure 2. Schematic diagram of the digital blocks of the VPIC

3. Test results

Two different bonding arrangements of the digital and analog tiers were processed and were successfully achieved by Tezzaron and Ziptronix. One option yielded a thinned analog tier connected to a standard digital tier, and a second option yielded a thinned digital tier bonded to a standard analogue tier. Only the option with a thinned analog tier was tested, because wire bonding is possible (option with thinned digital tier requires bump-bonding to the PCB) in this case. The testing system for VIPIC (Fig. 3) is based on two PCBs – one used for the IC and decoupling capacitors and second, motherboard, contained logic levels translators and LVDS to TTL converters, bias currents adjustment resistors, daughterboard insertion slot and communication interface connectors. The communication interface and virtual 32-bit long counters are implemented in a FPGA, which allows the operation in a zero-dead time mode (also called a continuous readout to take data without interruption from the device under test) and sending data through DMA to the higher level software, working on a Real-Time operating system. All the software is written in LabVIEW 2012 with the use of the FPGA and RT modules.
The following tests were performed for the VIPIC IC:

- total power consumption and bias levels measurements,
- verification of the digital part functionality,
- measurements of threshold spread and correction range,
- preliminary tests of analog blocks, estimation of gain and noise,
- tests in continuous readout mode.



a b

Figure 3. The VIPIC testing setup (a) and the IC wire-bonded to the daughter PCB (b)

3.1 Tests of digital blocks

Two registers (called SET and RESET), which are implemented in the digital back-end, allow setting pixels to operate in three modes:

- blocked (RESET = 1, pixel is not responsive),
- enabled (RESET and SET = 0, pixel is responsive if hit is registered),
- always responsive (SET = 1, pixels is responsive even if the data is zero).

The sparsifier implemented in the ASIC yields a binary address of hit pixels. Successful tests of this functionality prove that the priority encoder works as expected in each of 16 readout groups and it is possible to set a Region of Interest (ROI – see fig. 4), and also all addresses are reported for all 4096 pixels set to the always responsive mode. As the a chip is wire-bonded on the analogue tier to the PCB , the successfully operating registers, that are placed on the digital tier, provide a proof that TSVs and the bonding interface made on the metal 6 layer for power supplies and registers clock and data lines are built properly.

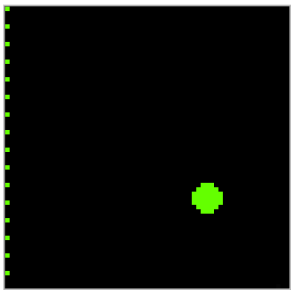


Figure 4. Image generated by addresses of pixels set to be always responsive (ROI).

3.2 Tests of analog blocks

An internal calibration pulse with externally controlled amplitude can be used for the tests of the analog front-end. The basic testing procedure is relies on varying the discriminator threshold voltage and reading the number of pulses at the discriminator output. The counters are only 5-bit long and therefore for the gathering enough of statistical population, each step of the threshold scan procedure was repeated 1000 times and the counts were being summed up in external counters. The tests of the pulse processing chain showed proper operation of the CSA and of the two amplifiers. The tests results, consisting an injection of varied test charge magnitudes are shown in fig. 5.

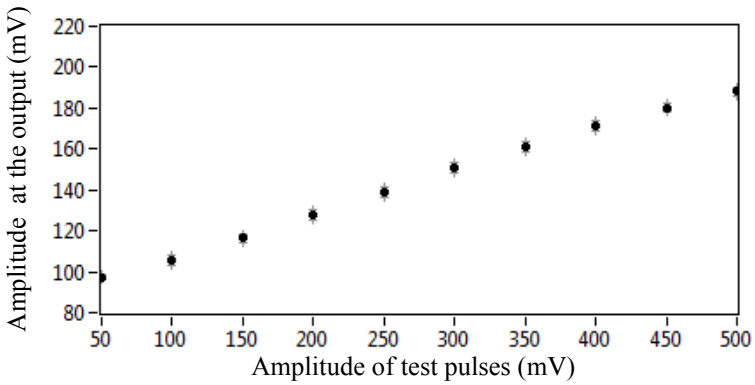


Figure 5. Response of VIPIC for different amplitude of input pulses

The analog blocks can be adjusted for minimizing the spread of DC levels at the discriminator input by proper setting of the Trim DACs. To check the Trim DAC ranges we loaded the Trim DAC registers with minimum and maximum values and measured the DC levels at the discriminator inputs. The result of this test is shown in fig 6, where two separated groups measured with extreme Trim DACs setting can be seen. The fact, that all pixels fully respondedto loading of these values allowed to conclude that all connections between tiers related to DACs must be functional.

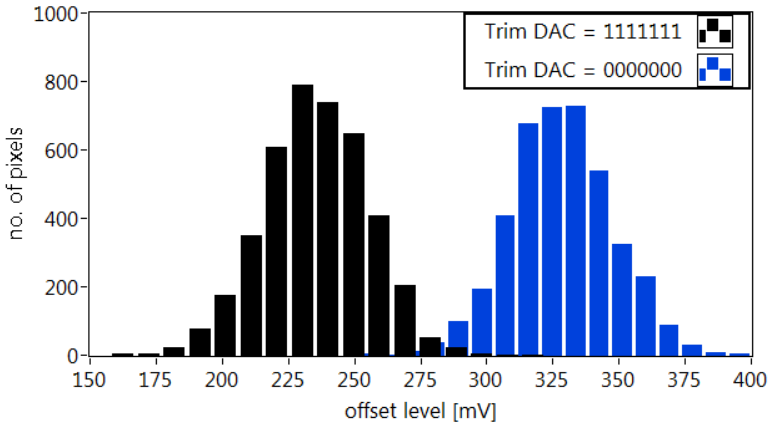


Figure 6. The histogram of the offset at the input of discrimminator for two extremal settings of trim DAC (0 and 127).

4.Summary

Preliminary results of the first three-dimensionally integrated chip for the photon science look very promising as both tiers (analogue and digital) were successfully connected without mistakes. Each pixel shows proper operation of both analogue and digital blocks and the communication between them with more than 30 bonding interface terminal per pixel and more than 120 000 in the whole matrix and TSVs carried signals to the tiers was proved.

5.Acknowledgments

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