

A new portable test bench for the ATLAS Tile Calorimeter front-end electronics certification

J. Alves¹, F. Carrió², H. Y. Kim³, I. Minashvili⁴, P. Moreno², R. Reed⁵, V. Schettino⁶, A. Shalyugin⁴, C. Solans⁷, J. Souza⁶, G. Usai², A. Valero²

1- LIP Portugal, 2- IFIC Spain, 3- UTA USA, 4- JINR Russian Federation, 5 - UW South Africa, 6- UFJF Brazil, 7- CERN

Abstract—This paper describes the upgraded portable test bench for the Tile Calorimeter of the ATLAS experiment at CERN. The previous version of the portable test bench was extensively used for certification and qualification of the front-end electronics during the commissioning phase as well as during the short maintenance periods of 2010 and 2011. The new version described here is designed to be an easily upgradable version of the 10-year-old system, able to evaluate the new technologies planned for the ATLAS upgrade as well as provide new functionalities to the present system. It will be used in the consolidation of electronics campaign during the long shutdown of the LHC in 2013-14 and during future maintenance periods. The system, based on a global re-design with state-of-the-art devices, is based on a back-end electronics crate instrumented with commercial and custom modules and a front-end GUI that is executed on an external portable computer and communicates with the controller in the crate through an Ethernet connection.

Key words—TileCal, Front-end electronics, MobiDICK, Test bench.

I. INTRODUCTION

The Large Hadron Collider (LHC) [1], at CERN is the most powerful particle collider in the world. The main goal of LHC is to collide two beams of protons or heavy ions travelling in opposite directions. These collisions, at 14 TeV in the center of mass, occur at four points, exactly at the locations of four detectors: ALICE, ATLAS, CMS, and LHCb. ATLAS is a general purpose detector and the Tile Calorimeter (TileCal) is its central hadronic calorimeter [2]. It provides accurate measurement of the energy and position of particle jets resulting from proton-proton collisions, missing transverse energy and assists in the identification of low momentum muons. The TileCal front-end electronics are responsible for shaping, amplifying and digitizing the analog signals from the photomultipliers and send data to the back-end electronics. A test bench, called *Mobile Drawer Integrity Checking System* (MobiDICK) [3] is used to check the integrity of the front-end electronics of the Tile Calorimeter. In this paper an upgraded version of MobiDICK is described. This paper is structured in 5 sections. In section II, the TileCal front-end electronics is described. Section III is dedicated to a short description of the previous test bench which has been used to test the TileCal front-end electronics in the last years. In section IV the new test bench developed to replace the old

one is described. Finally, in section V, there are the final considerations and conclusions about this work.

II. TILECAL FRONT-END ELECTRONICS

The TileCal is a sampling calorimeter which makes use of layered laminate steel (in plates of various dimensions) as absorber medium and scintillating tiles as active material. The basic structure of TileCal is a *cell*. It consists of alternating layers of steel and tiles. The tiles are placed in planes perpendicular to the LHC colliding beam and are staggered in depth. The calorimeter readout is divided in four cylindrical partitions: two central sections (Long Barrels LBA and LBC) and two endcaps at higher pseudorapidity (Extended Barrels EBA and EBC).

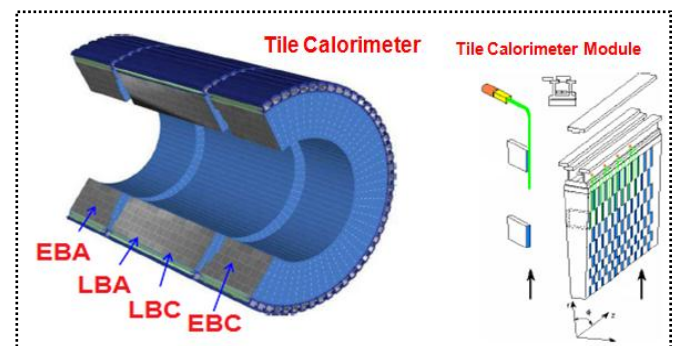


Fig. 1: TileCal.

The front-end electronics of TileCal is organized into compact structures called drawers. A combination of 2 drawers forms the so called super-drawer. Each super-drawer is associated with a module of the TileCal, and is able to collect information from 32 channels of the Extended Barrels or 45 channels of the Long Barrel. In the LHC experiments, ionizing particles that cross the TileCal produce photons in the scintillators, and the number of these photons is proportional to the energy deposited by the particles. These photons are absorbed and carried by Wavelength Shifting Fibers (WLSFs) and then feed a set of photo-multiplier tubes (PMTs). The PMTs convert the light signals into electrical pulses, which serve as input signals to the 3-in-1 cards in the front-end electronics (fig. 2). These cards perform the conditioning and processing of those analog signals, and send them to the digitizer system where they are digitized and organized in packets of data before being fed to the back-end electronics [4].

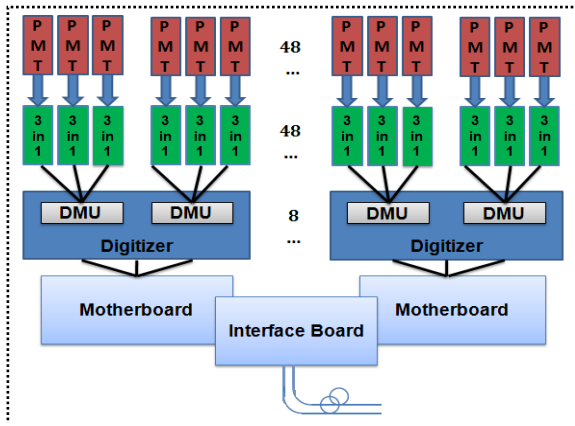


Fig. 2: TileCal Front-end Electronics.

The motherboard is a key component in a super-drawer, it provides low voltage power and digital control signals to four digitizer boards, one Interface Board and to the circuits needed for trigger summation and distribution. One super-drawer has two motherboards, which include all the electronics used for reading a full TileCal module. An Interface Board collects the sampled data from all the digitizers, serializes and transmits them to the back-end electronics using optical links [5]. This process is illustrated in fig. 2.

III. PREVIOUS TEST BENCH

A 10-years-old test bench has been used in the last years to certify the TileCal front-end electronics. The previous system (MobiDICK3) is contained in a custom aluminum box with dimensions 50x33x41 cm and the total weight about 20 kg (fig. 3).



Fig.3: Previous Test Bench.

The aluminum box contains a VME (Versa Module Europa) crate hosting a set of electronics boards. The system is controlled using a laptop, which is the interface to the operator [5]. The architecture of the previous system is presented in fig. 4.

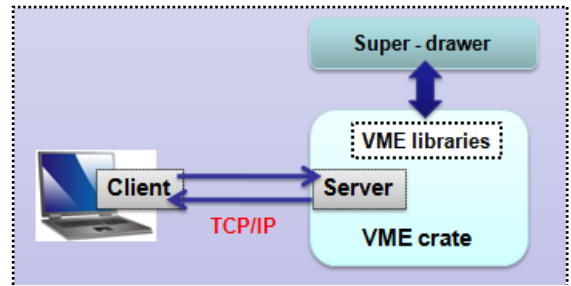


Fig. 4: Architecture of the Previous Test Bench.

The previous test bench is composed by a hardware and a software component. The hardware consists of a set of VME cards, which provides all the required functionalities to test a super-drawer. These hardware components and their functionalities are presented in Table I.

TABLE I
HARDWARE COMPONENTS OF THE PREVIOUS TEST BENCH

Module	Functionality
Server Processor (RIO2)	Central part of the system
CANbus interface	Communications with the front-end electronics
TTC system	Generates commands to the front-end, trigger and configuration.
Trigger ADC board	Digitizes trigger analog signals for muon and hadron selection
HVLED	Provides a -830 V high voltage input to the PMTs on the front-end electronics
LED driver	Delivers a voltage of 20 V able to light two LEDs in continuous or pulsed mode (20 ns pulses)

The software of the previous test bench is composed by two parts: The server running in a VME processor and a client running on a laptop. The server is a C program running under *LynxOS*. It performs all the electronics tests under requests of the client and sends back the results to the client. The client is a C++ program running on the laptop, under Linux, and it is the interface between the user and the system. It sends requests to the Server to perform the electronics tests and receive the results. These two parts communicate using TCP/IP (Ethernet connection) based on client/server architecture [5].

IV. NEW TEST BENCH

In this section the new version of MobiDICK is presented. In this new version new technologies to implement all the functionalities required to certify the front-end electronics of TileCal were used. In the following sub-section the motivation that led us to develop this new test bench is presented.

A. Motivation

The main reasons which led us to develop a new test bench are:

- At the present time there are three available units. A fourth one is required for the long LHC shutdown of 2013 to test the four TileCal barrels at the same time.

- There is no replacement for some old VME modules of the previous system.
- Size and weight reduction was required to improve the portability of the system.
- It was needed a new system to evaluate new technologies for the future upgrades.

B. Architecture

The new version of the described test bench is based on a reconfigurable system. A Xilinx evaluation board equipped with a Virtex-5 FPGA replaces the VME crate of the previous system. The functionalities of the VME components of the previous system are implemented using an embedded system, programmable logic and some custom electronic boards [5]. The architecture of this new test bench is presented in fig. 5.

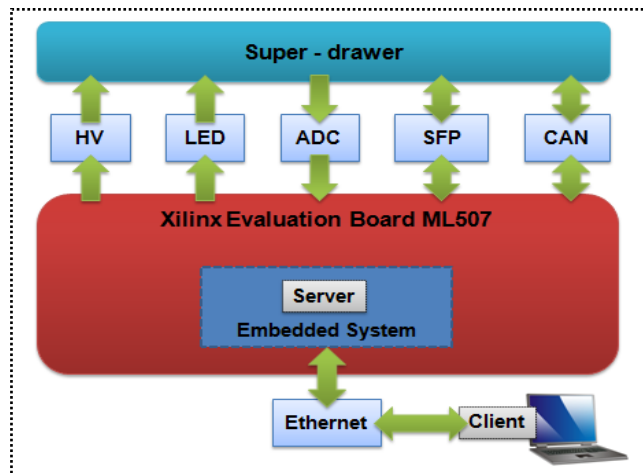


Fig. 5: Architecture of the New Test bench MobiDICK4.

As the previous system, the new test bench has two components: hardware and software. The hardware comprises the motherboard (Xilinx ML507), some custom electronic boards, a power supply system and a SFP (Small Form-factor Pluggable) module. The software has a client/server architecture. In this new test bench, the server runs in an embedded system implemented in the motherboard's FPGA. The client (the interface to the operator), runs on a laptop.

C. Hardware Components

Motherboard: a Xilinx ML507 board equipped with a Virtex-5 FPGA. The resources of this platform are: a PowerPC 440 RISC microprocessor, 4.25 Gbps GTX transceivers and a 10/100/1000 Ethernet MAC. It also includes 256 MB of DDR2 RAM and configuration storage, such as platform flash devices or a Compact Flash card-based system configuration controller (System ACE Controller) [6].



Fig. 6: Xilinx ML507.

HV board: provides a -830 V power supply to the PMTs of the super-drawer. Implements a high voltage power supply that is activated using a relay controlled by TTL (Transistor-transistor Level).

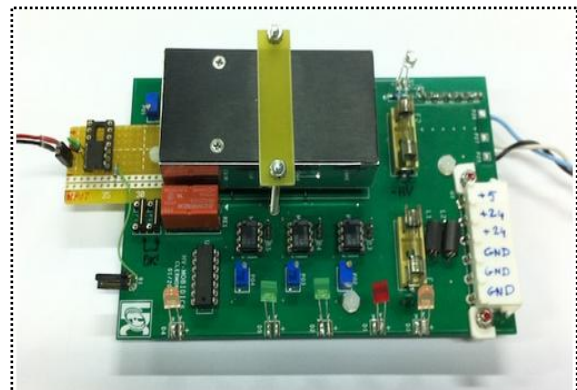


Fig. 7: HV Board.

LED board: provides a 20 V pulses required to calibrate the readout channels of the super-drawer. A monostable operated by TTL generates these pulses used to drive the LED board [5]. The purpose of this board is to check the response of the super-drawer to a light pulse similar to the one produced by particles in the scintillating tiles [3].

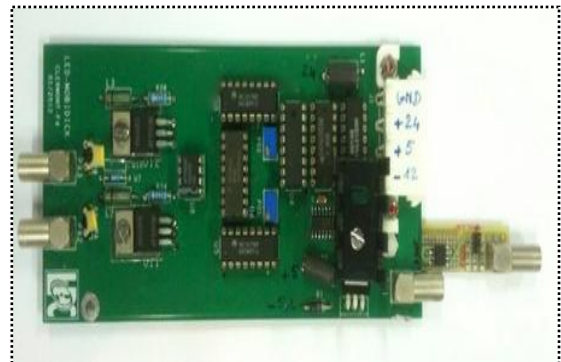


Fig. 8: LED Board.

Power supply distribution: a commercial ATX power supply is used to supply the LED, ADC boards and the CAN component. A LS150-24 AC/DC converter supplies the HV board and a transformer provided by Xilinx is used to supply the ML507 board.

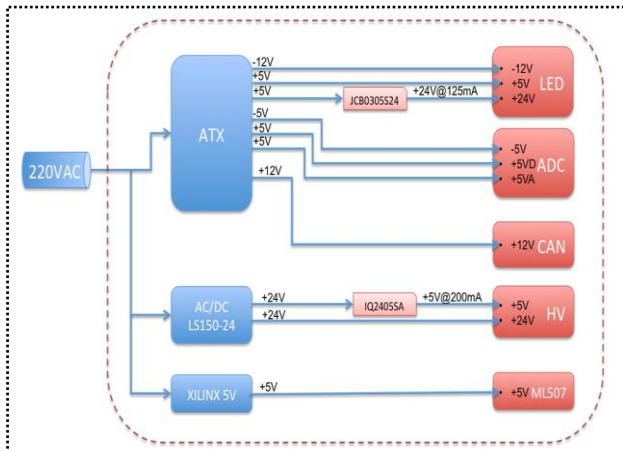


Fig. 9: Power Supply Distribution.

ADC board: custom board that digitizes analog trigger outputs (hadron and muon selection) of the super-drawer with a 40 MHz local oscillator. A four-layer PCB which hosts two Texas Instruments 8-channel 12-bit ADC (Analog-to-Digital Converter) chips (ADS5271), the analog differential input stages for every channel, clock oscillator and buffers. These are 8-Channel, 12-Bit, 50MSPS analog-to-digital converters, which implement serial LVDS (Low Voltage Differential Supply), input and output interfaces. The board populates the analog input stages for every channel needed for accommodating the trigger differential signals into the input voltage range of the ADC; it also implements an anti-aliasing filter for the digital conversion. In order to synchronize the digitization in both converters, a clock distribution network has been placed on the board as well. It consists of a 40 MHz clock oscillator and a clock buffer for cleaning the signal and adapting it to the ADC logic levels. The output channels are connected with similar length traces to two connectors that provide these signals to IO expansion connectors in the Xilinx ML507 board [5].



Fig. 10: ADC board.

ADC Board Test Results

In one of the MobiDICK tests, signals coming out of trigger cables of TileCal are digitized using the ADC board.

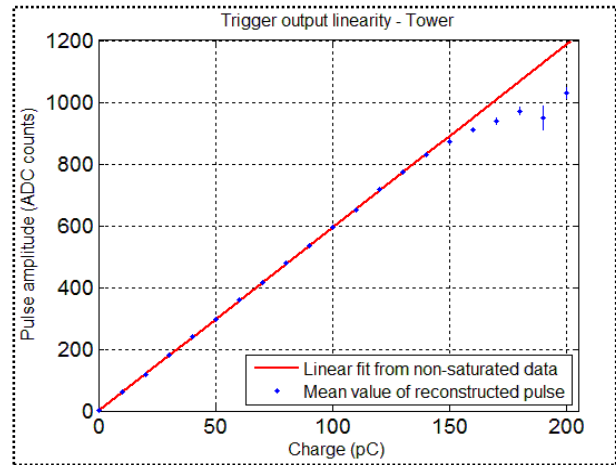


Fig. 11: Linearity plot of the ADC Board.

Fig. 11 shows the response measured by the ADC board in ADC counts versus the injected charge in pC. The ADC board is capable of reconstructing signals up to 200 pC from the tower signals of the super-drawers.

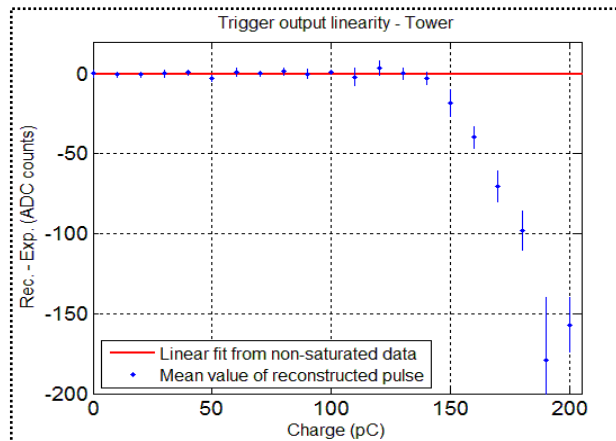


Fig. 12: Difference between the reconstructed response and the expected response extracted.

Fig. 12 shows the difference between the reconstructed response and the expected response extracted from a linear fit to the data of the previous plot. The deviation is of the order of 10% for charges below 200 pC which is within the specifications of the tests.

SFP Module: Optical connector that provides optical fibers' connection to the Interface Board of the super-drawer. Two optical fiber connections to super-drawer are used to send commands and receive digital data sent by the front-end electronics. The reception of the digital data is supported by S-Link protocol [7],[8], which uses G-Link devices as physical layers. In the back-end electronics of TileCal is implemented an ASIC G-Link receiver HDMP-1032, which is used to receive and de-serialize the data sent by a G-Link transmitter, the HDMP-1032 in the front-end electronics. A VHDL custom IP core was developed to emulate the functionality of the G-Link receiver. This custom IP core receives the serialized data through SFP, de-serializes it using the Xilinx GTP Transceiver available in the FPGA. The G-Link emulator also includes a

VHDL CRC (Cyclic Redundancy Check) module to check the integrity of the received data.



Fig. 13: SFP module.

CAN: two CAN bus interfaces are used to communicate with the super-drawer in a specific test. Two commercial adapters and a custom cable are used to convert the RS232 ports of the motherboard (ML507) to the CAN bus interface of the super-drawers. The RS232 ports are used to send and receives commands which are transformed into the CAN protocol using these adapters [5].



Fig. 14: Serial-CANbus Adapter.

D. The Embedded System

In the Virtex-5 FPGA, available on motherboard, is implemented an embedded system, which runs the server software responsible for performing electronic tests to the super-drawer.

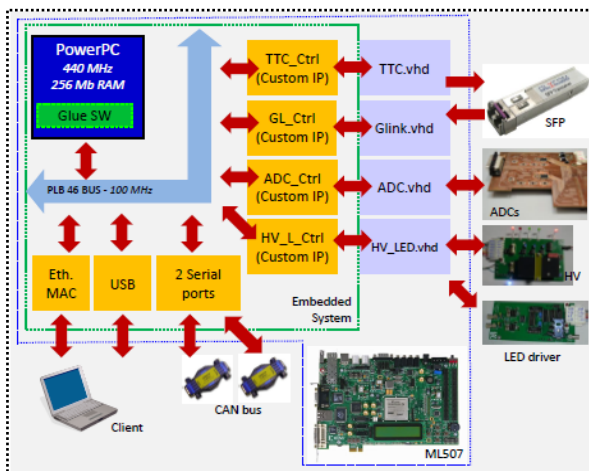


Fig. 15: The Embedded System of MobiDICK4.

In fig. 15 the embedded system of the new test bench is presented. This system is implemented around the PowerPC

microprocessor running at 440 MHz. The Operating System for the microprocessor is a Busybox Linux version with kernel 2.6, which was chosen mainly because there is an important community supporting the microprocessor and there are available drivers for Xilinx IP cores. An automatic boot of the whole system (bitstream + kernel + root file system) is performed from the Compact Flash using the System ACE Controller. The ELDK 4.2 (Embedded Linux Development Kit) [9] cross compiler tools are used for building the Linux OS image and for developing the software applications. The connection between the microprocessor and the peripherals is implemented using a 100 MHz Processor Local Bus 4.6 (PLB). The peripherals are IP cores: either commercial and provided by Xilinx, or custom IP cores developed to fulfill specific needs. The custom boards of the test bench are interfaced to the embedded system by VHDL firmware modules implemented on the FPGA and required libraries for the applications that run on the server [5].

E. Software Component

The software of the MobiDICK4 has a client-server architecture. The server runs on the embedded microprocessor in the FPGA, it is responsible to handle the requests (commands) sent by the client, execute them and send back the results. The client running on a laptop sends requests to the server to perform the required electronic tests. It provides a Graphical User Interface to the user. A glue software replaces the VME libraries of the previous test bench [5]. Fig. 16 shows the client-server architecture of MobiDICK4.

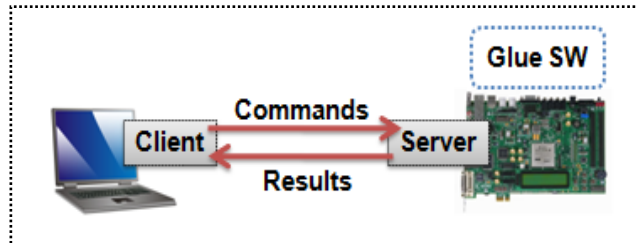


Fig. 16: MobiDICK4's Software.

F. Mechanics, Assembly and the First Prototype

The new test bench system is fully contained in an aluminum box with dimensions: 35x40x20 cm. The weight is about 4 kg. A LCD 16x2 is mounted in the box's external part to present the status of the system to the operator. A custom IP core was developed and integrated in the embedded system, which allows writing characters on the LCD display through software applications running on the embedded microprocessor. In fig. 17 the first prototype of the new test bench described in this paper is presented.



Fig. 17: First Prototype of the New Test Bench.

V. CONCLUSION

A new portable test bench to certify the front-end electronics of the Tile Calorimeter of ATLAS is presented. This new system is an upgraded version of the 10-year-old system, able to evaluate new technologies planned for the ATLAS upgrade and with additional functionalities with respect to the previous system. The new test bench, called MobiDICK4, is implemented around a reconfigurable device, a Virtex-5 FPGA in a Xilinx ML507 board. The MobiDICK4 includes a server and a client. The client runs in a laptop and sends commands to the server, requesting electronics tests to the front-end electronics, while the server runs in an embedded system implemented in a FPGA of the motherboard (Xilinx) ML507 and is responsible for handling the requests, performing the electronics tests and sending back the results to the client.

ACKNOWLEDGMENT

The authors thank all people who have contributed to the development and conclusion of this new test bench.

REFERENCES

- [1] *The Large Hadron Collider*, The LHC Study Group, CERN/AC/95-05, 1995.
<https://cds.cern.ch/record/291782/files/cm-p00047618.pdf>
- [2] *Tile Calorimeter Technical Design Report*, CERN/LHCC 96-42, 15-12-1996.
http://atlas.web.cern.ch/Atlas/SUB_DETECTORS/TILE/TDR/TDR.html
- [3] David Calvet and Vincent Giangiobbe, "Performance of the TileCal super-drawers from a global analysis of the MobiDICK tests", ATL-TILECAL-PUB-2008-007 (April 2008).
<https://cds.cern.ch/record/1026732/files/tilecal-pub-2008-007.pdf>
- [4] Romeo Bonnefoy, David Calvet, Robert Chadelas, Michel Crouau, Franck Martin, "MobiDICK: a mobile test bench for the TileCal super-drawer", ATL-TILECAL-2004-003 (March 2004).
<https://cds.cern.ch/record/681350/files/tilecal-2004-003.pdf>
- [5] P. Moreno, J. Alves, D. Calvet, F. Carrió, M. Crouau, K. HeeYeun, I. Minashvili, S. Nemecek, G. Qin, V. Schettino, C. Solans, G. Usai, A. Valero, "A new portable test bench for the ATLAS Tile Calorimeter front-end

electronics", TWEPP 2012 Topical Workshop on Electronics for Particle Physics (Oxford), 2012

Journal of Instrumentation, Vol. 8, Feb. 2013 (P Moreno et al 2013 JINST 8 C02046 doi:10.1088/1748-0221/8/02/C02046, <http://iopscience.iop.org/1748-0221/8/02/C02046>)

[6] ML505/ML506/ML507 Evaluation Platform User Guide, UG347 (v3.1.2) May 16, 2011, Xilinx, Inc.
http://www.xilinx.com/support/documentation/boards_and_kits/ug347.pdf

[7] Owen Boyle, Robert McLaren & Erik van der Bij, *The S-Link Interface Specification*, 1997.
<http://vanderby.web.cern.ch/vanderby/s-link/spec/spec/s-link.pdf>

[8] Attila Racz, Robert McLaren & Erik van der Bij, *The S-Link 64 bit extension specification: S-Link64*, 2003.

[9] <http://www.denx.de/wiki/DULG/ELDK>