The ATLAS Insertable B-Layer (IBL) Project

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Abstract

Preparing for the high luminosity LHC phase, the ATLAS experiment will upgrade its Pixel Detector with the installation of a new pixel layer. The new sub detector, called the Insertable B-layer (IBL), will be installed during the LHC first shut down in 2013-2014, in between the innermost current pixel layer and the beampipe.
To cope with the high radiation and pixel occupancy due to the proximity to the interaction point, a new read-out chip FE-I4 and two different silicon sensor technologies, planar and 3D have been developed. Furthermore, the physics performance should be improved through the reduction of pixel size and a new mechanical support using lightweight staves.
Two pre-series staves were made in order to qualify the assembly procedure, the loaded module electrical integrity and the read-out chain before going into production.

Keywords: ATLAS, Pixel Detector, 3D, IBL, FE-I4, Stave

1. The ATLAS Insertable B-Layer

1.1. The ATLAS Pixel Detector

The ATLAS detector [1], an experiment at the CERN Large Hadron Collider (LHC), is a general purpose particle detector designed to explore new frontiers of particle physics. It is composed of several subdetectors assuring globally the particle reconstruction and identification, making the ATLAS experiment sensitive to a wide range of signatures.

The innermost part of the detector assuring the particle tracking, operational since 2009 with a recorded integrated luminosity of 27 fb^{-1}, is composed by several subsystems with different detector technologies. Closest to the interaction point, three pixel layers assure a high P_T resolution and vertex reconstruction (Pixel Detector [2]), which is essential to cope with the high pileup at LHC ($<\mu>$=19 pileup event/bunch cross at $\sqrt{s}$ = 8 TeV).

After successful operation in the last three years, the LHC machine will be upgraded during the 2013-2014 long shutdown to increase the instantaneous luminosity and the collision energy to $\sqrt{s}$ =14 TeV. To ensure the long term physics performance coping with a high occupancy environment and pileup, a detector upgrade will be necessary [3].

1.2. The Insertable B-Layer

The Insertable B-Layer pixel detector will be the fourth layer added to the present Pixel Detector between a new beam pipe and the current inner Pixel Detector layer (B-layer). The present beam pipe will be replaced by a smaller one, with an inner radius of R=23.5 mm, allowing for the installation of the IBL at an average radius of 34 mm and an envelope of only 9 mm [4].

The IBL is composed of 14 staves (64 cm long 2 cm wide and tilted in ϕ at 14 degrees) equipped with 32 front-end chips per stave and sensors facing the beam pipe (η coverage of 2.5). Hermeticity in the transaxial (R-ϕ) plane is ensured by about 20% stave-to-stave overlap as is shown in Figure 1. The overall design has been targeted to reduce the material budget of the total IBL package down to 1.6% X_0, minimizing the particle scattering at low radius.

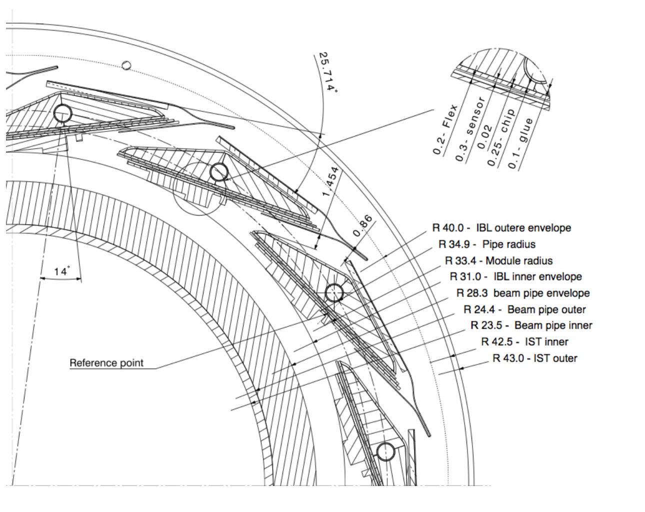

Figure 1: Transversal cut of the IBL detector and beam pipe.

Each IBL stave will be populated with planar pixel technology (12 double chip modules) in the central region and 3D technology (4+4 single chip modules) in the outer one (forward region).

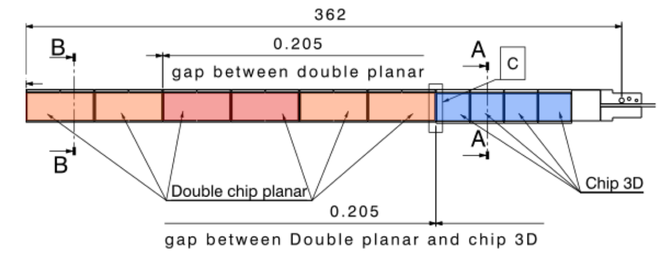

Figure 2: Half stave layout and sensor technologies. Module powering sectors are indicated with different colors. The stave being fully symmetric, one side is not represented

2. The IBL readout and sensor technologies

2.1. New FrontEnd FE-I4

The new IBL front-end (FE) readout FE-I4 has been designed in 130 nm CMOS technology, with an active area of up to 90% [5] (compared to <75% on the current pixel FE, FE-I3[6]). The FE-I4 readout chip, with a total size of 20.2x18.8 mm^2 (5 times larger than the FE-I3), consists of 26880 pixel cells organized in a matrix of 80 columns (50 μm pitch) by 336 rows (250 μm pitch)

An analog pre-amplification before the pixel comparator, designed for low currents (double stage), reduces the activity in the digital region (Figure 3).

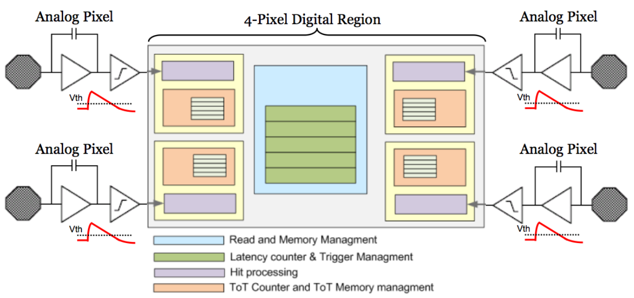

Figure 3: Schematic of the analog and digital 4 pixel matrix functionality

The design relies on a local memory-based architecture (2x2 pixel blocks) with 5 ToT[1] memories (4 bits) per pixel, to accommodate the higher hit rate while keeping the busy/waiting inefficiency in the order of 10^{-3}. The hits are locally stored with a maximum latency of 5 bunch crosses, and only sent if an L1 trigger matches the latency of the event, reducing the DC bus traffic and consequently the power consumption which is targeted to 200 mW/cm^2.

Beyond the large size and high rate capacity, the FE-I4 radiation tolerance has been improved by implementing thin oxide core transistors, showing efficiencies > 87% after 200 MRad irradiation [5].

[1]Time over Threshold, in LHC bunch cross units (25 ns)

To reduce the material budget, the thinned FE is attached to a support wafer (glass substrate) before electroplating under-bump metallization and micro-bump deposition. After hybridization the support wafer is removed, leading to a FE thickness of only 150 μm.

2.2. Sensors technology

Silicon 3D n-in-p (processed with double-side technique by FBK[2] and CNM[3]) and Planar n+-in-n (processed by CiS[4], as for the present Pixel Detector) were retained for the IBL, motivated by their high efficiency after irradiation to NIEL[5] of $5 \times 10^{15} n_{eq}/cm^2$ and schedule constraints.
Both technologies are assembled with FE-I4 readout chips. The planar sensor layout allows for double chip configuration thanks to its high yield while the 3D sensors are connected to one single chip.

Double chip sensors are fabricated at CiS with a reduced thickness with respect to the current Pixel Detector of 200 μm, limiting the material budget while reducing the depletion voltage especially after bulk radiation.

In the back plane, a central pad assures the high voltage distribution surrounded by an optimized arrangement of thirteen guard rings avoiding edge effects [7]. The pixel length in the edge region is two times longer (500 μm) and ovelaps with the guard rings in order to maximize the sensitive parts and extend the active region, up to 200 μm from the cutting edge (Figure 4).

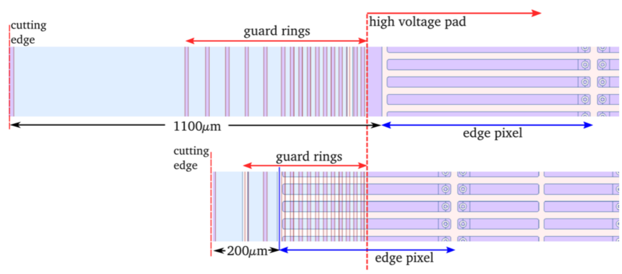

Figure 4: Planar Pixel sensor edge pixel and guard rings for the current Atlas pixel (top) and new IBL design (bottom)

3D sensors produced in FBK and CNM, have micro machined electrodes doped by a thermal diffusion process (n$^+$ columns on the front side, p$^+$ from the back side). One of the main differences between both manufacturers is the column depth, full traversing columns (FBK) or double type double face (CNM), as shown in Figure 5.

[2]Fondazione Bruno Kessler (FBK), Via Sommarive 18, 38123 Povo di Trento, Italy.
[3]Centro Nacional de Microelectronica (CNM-IMB-CSIC), Campus Universidad Autonoma de Barcelona, 08193 Bellaterra (Barcelona), Spain.
[4]CiS Forschungsinstitut fur Mikrosensorik und Photovoltaik GmbH, Konrad-Zuse-Strasse 14, 99099 Erfurt, Germany
[5]Non ionizing energy loss

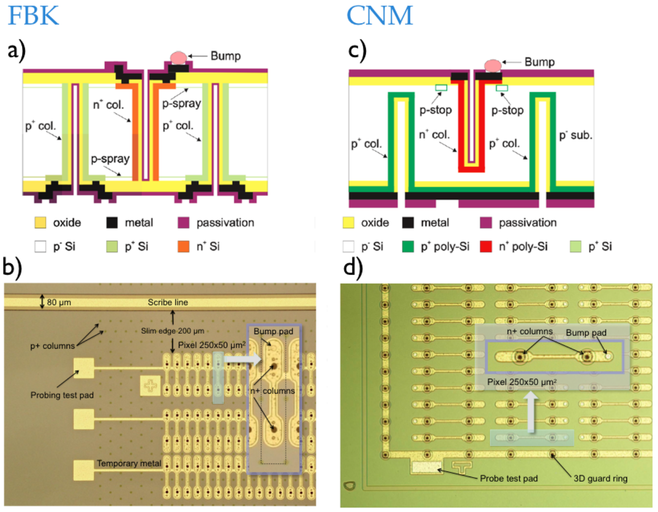

Figure 5: Schematic column design for FBK (a) and CNM (c). Details of: pixel, probing pad and edge resistive columns/ guard rings, are shown for FBK (b) and CNM (d)

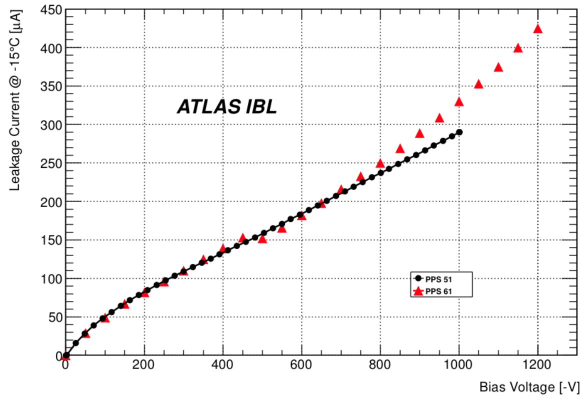

Figure 6: I-V curves for CiS module at -15^{o}, after irradiation to a fluence of $6 \times 10^{15} neq/cm^2$ [8]

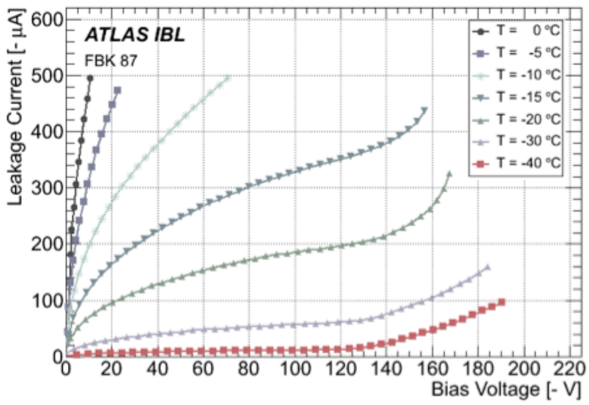

Figure 7: I-V curves for FBK module at different temperatures, after irradiation to a fluence of $5 \times 10^{15} neq/cm^2$ [8]

The FBK slim edge fence consists of 4 resistive rows of p$^+$ columns that stop the depletions, as opposed to the CNM n$^+$ 3D guard ring approach. Despite the sensors' differences, both designs will be used indistinguishably. The ~70 μm electrode separation makes a low operation voltage (<160 V after irradiation) possible, while reducing the drift distance allowing for an efficient tracking at high η.

2.3. *Module qualification after irradiation*

With a maximum expected integrated luminosity of 500 fb^{-1}, the radiation tolerance of the IBL is of special concern. Both planar and 3D modules have been irradiated and qualified up to doses of 750 MRad and 250 MRad, with a 25 MeV proton beam at KIT[6] and neutron reactors at TRIGA[7] respectively.

The I-V curves for each of the IBL sensor technologies after irradiation are shown in Figures 6 and 7. Post-irradiated samples show an ohmic behavior, as expected from heavily radiation damaged material, but no breakdown is observed. Due to their ohmic behavior, thermal contact to the cooling surface is of critical importance to avoid thermal runaway, specially at high voltage operation.

Figure 8 and 9 show the equivalent noise charge as a function of the bias voltage (V_b), for different FE-I4 tunings, showing no significant variation after irradiation, for both technologies, which is needed for low threshold operation. After irradiation at 1 kV bias voltage, the planar sensors operate in the quasi-avalanche regime, showing an increase in the sensor noise.

Samples were exposed to a ^{90}Sr source, measuring ToT value as a function of the V_b, shown in Figures 10 and 11. For non-irradiated samples no V_b dependance is observed after depletion. Charge collection after irradiation is of ~90% for planars

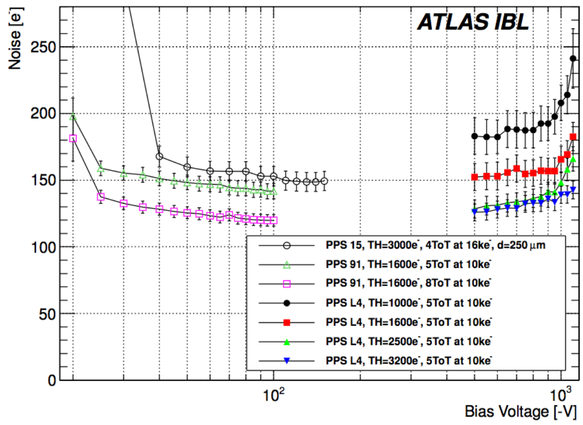

Figure 8: Noise as a function of V_b for CiS modules at different ToT tunings, before and after irradiation [8]

and ~70% for 3D, increasing with the bias voltage as expected due to the charge multiplication at bias being much higher than the depletion voltage.

[6]Karlsruhe Institute of Technology, Karlsruhe, Germany

[7]TRIGA reactor, Jozef Stefan Institute, Ljubljana, Slovenia

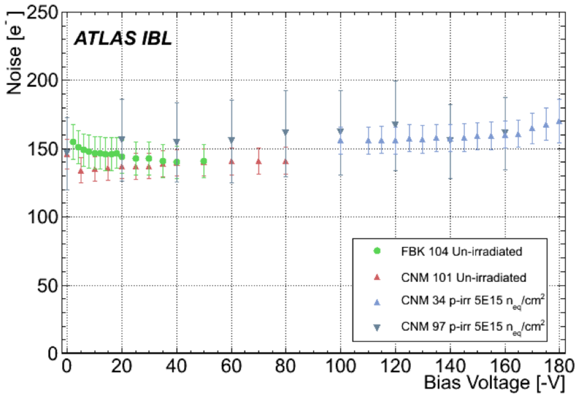

Figure 9: Noise as a function of V_b for FBK and CNM modules at -15^o, before and after irradiation [8]

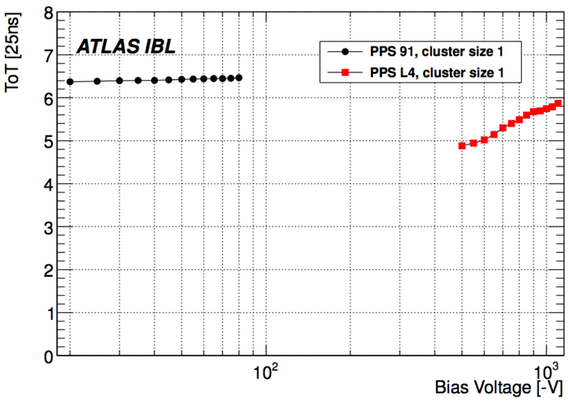

Figure 10: ToT charge collection in BC units, using a ^{90}Sr, of planar sensor before irradiation (PPS 91) and after irradiation to $5 \times 10^{15} n_{eq}/cm^2$ (PPS L4) as a function of depletion voltage [8]

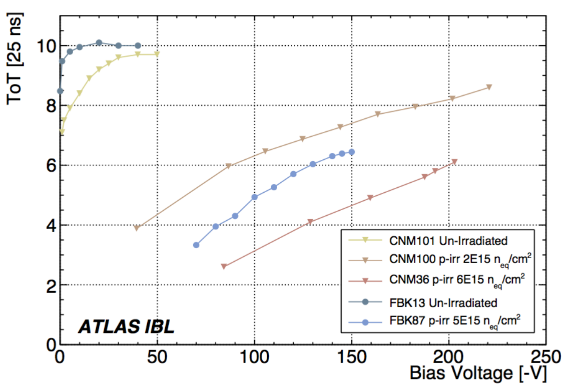

Figure 11: ToT charge collection in BC units, using a ^{90}Sr, of 3D sensor before irradiation and after irradiation as a function of depletion voltage [8]

IBL modules performance has been extensively studied in test-beams, understanding and optimizing their operation. Particle tracking accuracy, was measured thanks to an external tracks reconstruction from the EUDET telescope and hit matching, showing an RMS of only 15 μm [8]. Tracking reconstruction for edge pixels and hit efficiency after irradiation, confirms that both technologies have only 200 μm inactive area from their edge.

3. Stave assembly process and first prototypes

3.1. Stave assembling

IBL stave components are produced in several ATLAS institutes, and shipped to University of Geneva where the final stave assembly is performed. To ensure good performance, all components follow a strict quality assurance (QA) when received, and all along the module loading, assembly and wire bonding operations. Although 24 staves will be produced, due to the limited reworkability of the components after assembly, the QA is of crucial importance to ensure the best performance of the final IBL detector.

After flex gluing and a connectivity check, the stave and flex assembly is delivered to the Production Center clean rooms. A metrology of the face plate, before and after thermal-cycling[8], is performed to verify the mechanical integrity before module loading.

Simultaneously, modules from production sites are received and tested with an USBpix setup [9]. The module reception test verifies digital and analog FE response, as well as pixel noise and crosstalk, pointing out any possible damage happened during the shipment. In addition, to fully qualify the modules, an optical inspection is done and an I-V is performed.

The selected modules are loaded onto the stave with a 70 μm thermal grease layer and two epoxy glue dots per front-end to hold each module. Each module is electrically connected via the flex wing which is first glued and in the second step wire bonded. Each module is then electrically accessible via temporary PCB and flex savers mounted at the two extremities (Figure 12).

The final assembly is thermally cycled and a metrology survey is performed to check that the mechanical specifications are fulfilled. An electrical test of the full functionality of the stave, similar to the modules reception test, is performed before shipment to CERN, where an extensive burn-in and QA tests will be undertaken before the final integration around the beam pipe.

3.2. Prototype staves: test and results

The behavior of the integrated parts has been studied with the Stave 0-a and Stave 0-b, the first two functional and complete staves. Between the production of the two staves 0, several jigs and components were upgraded fixing potential problems and improving procedures while targeting for the highest production quality.

Although single module operations were well understood, extensive tuning tests and trigger scans have been performed

[8]Thermal-cycles performed to the staves consist of 10 cycles from -40^o to + 40^o, with controlled humidity

on the two staves 0, to characterize their behavior with the new common power scheme and command lines.

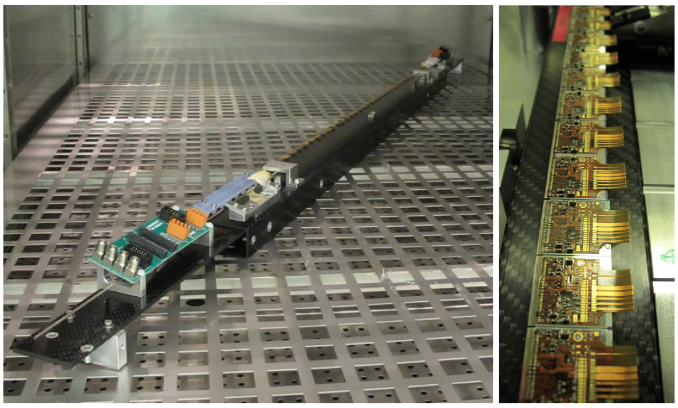

Figure 12: Stave 0-a before loading (left) and after loading (right). Non attached wings can be seen on the side of the carbon fiber stave, as well as the stave PCB-saver on the edges, all supported by the stave handling frame

Threshold mean values are shown in Figure 13. Module reception test threshold spreads can be explained due to the use of configuration files from production sites, while using different operational temperatures and setups. However, stave results were obtained after stave tuning, showing a great FE to FE homogeneity and low threshold dispersion.
Noise values (Figure 14) remain constant and under IBL specification for each FE, showing that no damage is done to the modules during production.

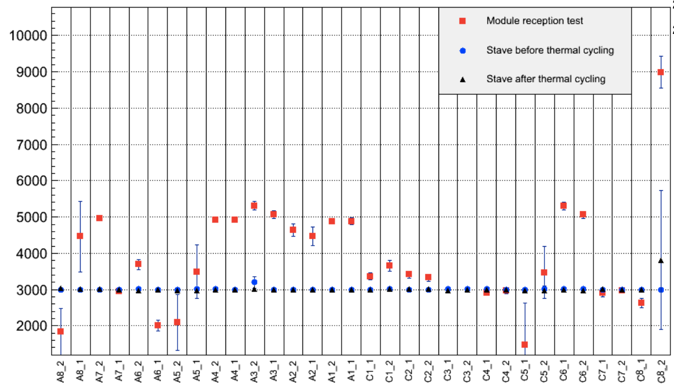

Figure 13: Threshold mean value and dispersion (error bars) of Stave 0-b FE during reception test (squares), after loading before thermal-cycling (circles), after loading after thermal-cycling (triangles)

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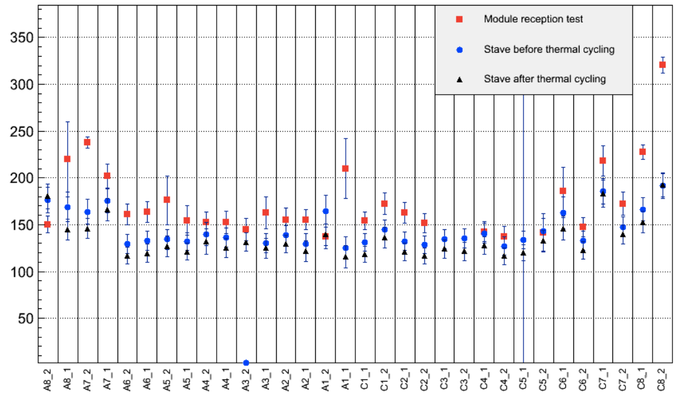

Figure 14: Noise mean value and dispersion (error bars) of Stave 0-b FE during reception test (squares), after loading before thermal-cycling (circles), after loading after thermal-cycling (triangles)

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