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A new portable test bench for the ATLAS Tile Calorimeter front-end electronics

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ABSTRACT: This paper describes a new portable test bench for the TileCal sub-detector of the ATLAS experiment at CERN. The system is used for the certification and quality checks of the front-end electronics drawers. It is designed to be an easily upgradable version of the current 10-year-old system, able to evaluate the new technologies planned for the upgrade as well as provide new functionality to the present system. It will be used during the long shutdown of the LHC in 2013-14 and during future maintenance periods.

KEYWORDS: ATLAS Tile Calorimeter; FPGA; ADC; Test bench; Embbeded system.

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Contents

1. The ATLAS Tile Calorimeter

1.1 Background

The Large Hadron Collider (LHC) [1] is nowadays the most powerful particle accelerator in the world. It has been built in the CERN facilities in Geneva (Switzerland), and is designed to study proton beam collisions at 14 TeV in the center of mass. It comprises four experiments: ALICE, CMS, LHCb and ATLAS , the last one being a general purpose particle detector composed of many subsystems.

The ATLAS Tile Calorimeter (TileCal) [3] is the central section of the hadronic calorimeter of the ATLAS experiment [2]. It provides accurate energy and position measurements for jets of hadrons associated with final state quarks and gluons, as well as for tau leptons and isolated hadrons. It also contributes in particle identification and in muon momentum reconstruction.

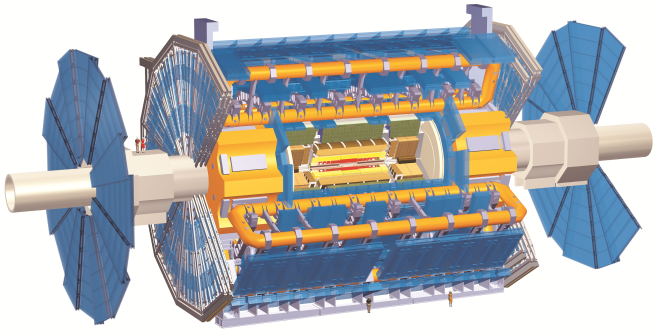


Figure 1. ATLAS

1.2 Front-end electronics

TileCal is a sampling calorimeter, with steel as the absorber medium and scintillating tiles as the active material. The calorimeter readout is divided in four cylindrical partitions: two central sections (Long Barrels LBA and LBC) and two endcaps at higher pseudorapidity (Extended Barrels EBA and EBC). These four partitions are azimuthally segmented in 64 wedges (modules) where the scintillating plastic tiles that produce light in the interactions with the particles are arranged in 3D geometrical cells.

One module hosts up to 45 photomultiplier tubes (PMTs), that convert the light collected in their correspondent cells to an electrical pulse. This is digitized on a subsequent step. The total number of read-out channels is 9856. Data of these channels are transmitted to the back-end electronics for processing.

The PMTs and front-end electronics are housed at the outermost region of the modules in so-called super -drawers. The PMTs are each equipped with a 3-in-1 card which provides pulse shaping, and calibration. A set of four Motherboards running the length of the superdrawer provide power and control for the 3-in-1 cards as well as power to boards used for L1 trigger summation and distribution. Analog signals from the 3-in-1 cards are sampled by eight digitizer boards equipped with TTCrx [4] chips and pipeline memories. An Interface board collects the sampled data from the all the digitizers, serializes and transmits them to the back-end electronics using optical links.

2. Current Test Bench

2.1 Introduction

MobiDICK (Mobile Drawer Integrity Checking system) [5] is a test bench designed to certify the TileCal super-drawers during maintenance periods. The functionality of the test bench involves transmitting commands to the super-drawers and reading data from its readout channels, trigger analog outputs or CANbus integrators. In regular data taking conditions, these operations rely on a set of hardware, which is based on modular VME [6] electronics, and is located in a separate cavern with the rest of the so-called back-end electronics.

2.2 Hardware

During maintenance periods access to the front-end electronics is possible and all external connections are removed. In order to provide in situ certification, a portable test bench has been designed to substitute all the back-end functionality.

Previous versions of the test bench were based on a portable custom aluminum box which contained a crate populated with the necessary VME boards to operate the super-drawers and a laptop as user interface.

The main boards used on that test bench were:

- Rio2 VME processor card: It is the central part of the system, being the master of the VME bus and controling the rest VME cards. It hosts the server part of the test bench software.
- HOLA SLINK cards: It is the optical interface for recieving fast digital data from the super-drawers data. This card implements a standard S-LINK with a forward and a return channel. For the optical transmission a Small Form Factor Pluggable (SFP) connector is used.
- VME CANbus interface: One TVME200 and two TIP816 modules form the system for the CANbus communication. The TVME200 works as a VME platform, holding two TIP816 units, which are independent CANbus interfaces. These two modules are then connected to a custom-made board which provides the +12 V power supply of the VME backplane needed for the CANbus interface in the super-drawer.
- The TTCvi and TTCex: These modules are responsible for the generation of TTC signals and their transmission to the front-end. The TTCvi is a VME card that generates the configuration and trigger commands to the super-drawer readout electronics The TTCex converts the electrical signals generated by the TTCvi into optical signals compatible with the super-drawers readout electronics. These signals are sent to the front-end electronics using optical fibers.
- The trigger ADC: A CAEN V792 VME ADC digitizes the signals from the super-drawer adders after they have been converted from differential to single-ended form by the DIFF2ADC module.
- The HV power supply and LED driver: These two systems are physically implemented on the same custom PCB. A DC/DC converter supplies -830 V necessary for the PMT operation. The second system is an LED driver which delivers 20 V for lighting two LEDs in either continuous or 20 ns pulsed mode. They are controlled by the DIFF2ADC board.

2.3 Software

The MobiDICK software is based on a client/server architecture that communicates using TCP/IP.

The server is written in C and runs on the VME processor board under a LynxOS [7]. It performs the electronic tests upon request of the client software. To do so, it controls the different VME modules and custom boards described on the previous section. Once the tests have been performed, it sends back the results to the client.

The operator interfaces the system through the client software, which is a C++ program that runs on the Linux-based laptop. The client requests the tests to the server, receives the results and displays them to the operator in a friendly way.

2.4 Need for a new test bench

The main reasons for the design of a new test bench are the following:

- At the present time there are three available units. A fourth one is required to test the four TileCal partitions at the same time. New tests must be perfomed on the front-end electronics after maintenance operations during the long shutdown of 2013-2014.
- There is no replacement for some old VME modules, for example the VME processor board.
- Enhanced portability would facilitate the certification of the superdrawers. The design of the new test bench equipment aims to reduce its total size and weight.
- The development of new hardware for the test bench will lead to the evaluation of new technologies for the future upgrade of the TileCal electronics.

3. MobiDICK4

The basic idea behind MobiDICK4 is the substitution of the VME system (crate and modules) of the previous test bench versions with programmable logic. The functionality of the VME modules is emulated using an embedded system together with the programmable logic and some custom made PCBs. In order to simplify the design, an FPGA evaluation board has been preferred to be used as core of the system rather than designing from scratch a custom FPGA-based board. Figure 2 shows a basic diagram of the MobiDICK4 system.

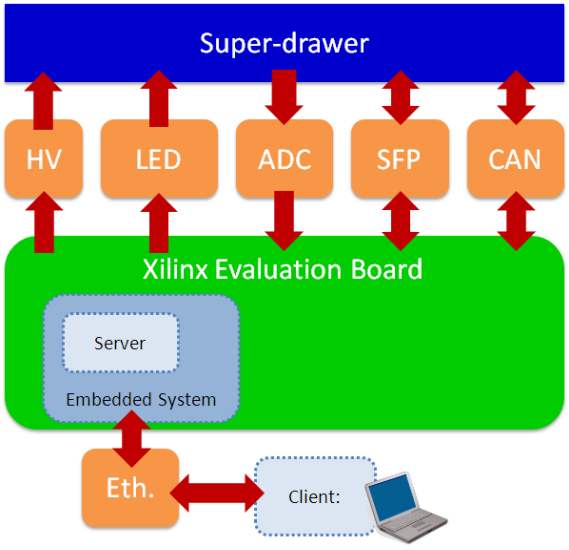


Figure 2. MobiDICK4 schema

3.1 Motherboard

The motherboard of MobiDICK4 is a Xilinx ML507 [8], [9] evaluation platform, which is based on a Virtex-5 device. Besides the programmable logic, this FPGA populates hardwired resources very useful to the test bench purposes, as a PowerPC 440 RISC microprocessor, 4.25 Gbps GTX transceivers or a 10/100/1000 Ethernet MAC among many others.

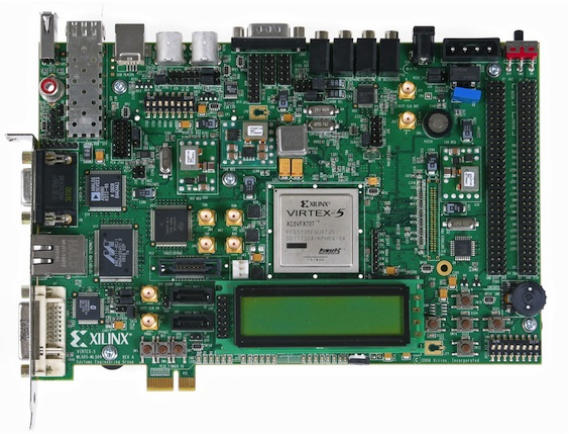


Figure 3. Xilinx ML507 evaluation platform

The ML507 also includes 256 MB of DDR2 RAM, as well as configuration storage solutions like platform flash devices or a CompactFlash card-based system configuration controller (System ACE Controller). To communicate to the outside world, the motherboard integrates serial ports, a SFP connector socket, RJ45 and USB host and peripheral connectors. Figure 3 shows a picture of the ML507 evaluation platform.

3.2 Power distribution

The power distribution system is based on two main units: a commercial AC/DC converter and a custom PCB populated with many DC/DC converters. Together, they provide the different voltages to the rest of the devices of the test bench.

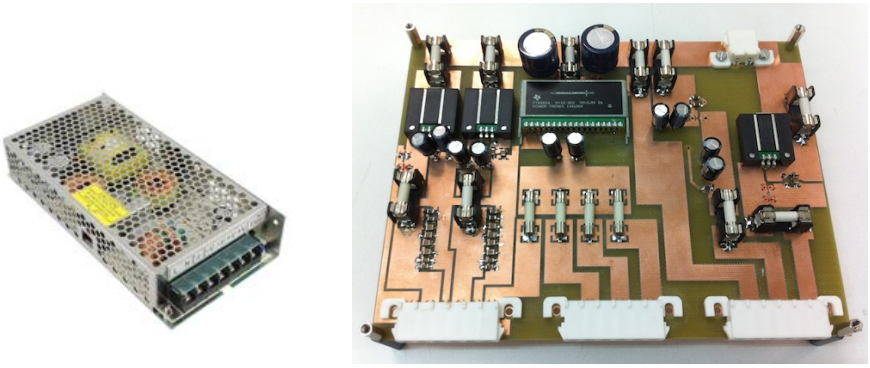
The first step on the power distribution is the TDK-LAMBDA LS150-24 AC/DC converter. It delivers a DC voltage of +24 V and a current up to 6.5 A.

In the subsequent step, the custom PCB, called Power Distribution Board, implements many non-isolated DC/DC converters in order to obtain different voltages:

- PT78NR105H: -5 V @ -1 A for the analog supplies in the ADC chips
- PT78HT205H: +5 V @ 2 A for the analog supplies in the ADC chips
- PT6883A: +5 V @ 5 A for the digital circuitry of the motherboard, LED driver, HV board and the digital supplies in the ADC chips
- PT9SR112H: +12 V @ 1.5 A for the fans installed on the aluminum box
- PTN78000A: -12 V @ -1.5 A for the LED driver board

- Direct +24 V for the LED driver and the HV board

Figure 4 shows pictures of the LS150-24 AC/DC converter as well as the custom Power Distribution Board.



(a) LS150-24 AC/DC (b) Power Distribution Board

Figure 4. Components of the power distribution system

3.3 Trigger ADC board

A custom board receives and digitizes the analog trigger outputs of the super-drawer for the hadron and muon selection at the LHC 40.08 MHz clock rate. It is a four-layer PCB that hosts two Texas Instruments ADS5271. These are 8-Channel, 12-Bit, 50MSPS analog-to-digital converters, which implement serial LVDS input and output interfaces. The PCB populates the analog input stages for every channel needed for accomodating the trigger differential signals into the input voltage range of the ADC, it also implements an anti-aliasing filter for the digital conversion. In order to synchronize the digitization in both converters, a clock distribution network has been placed on the board as well. It consists of a 40.08 MHz clock oscillator and a clock buffer for cleaning the signal and adapting it to the ADC logic levels. The output channels are connected with similar length traces to two connectors that provide these signals to IO expansion connectors in the Xilinx ML507 board. The Trigger ADC board is shown in figure 5.

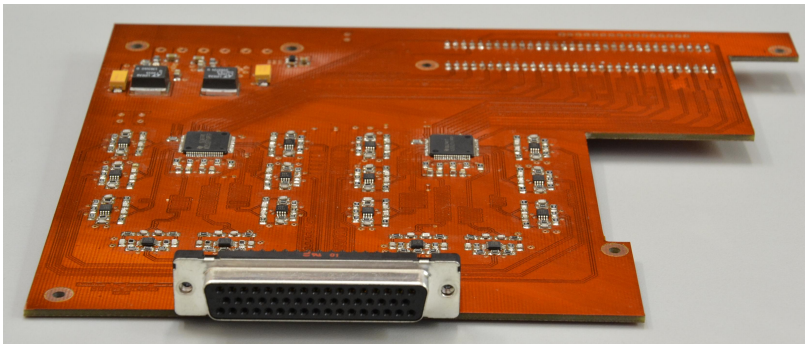
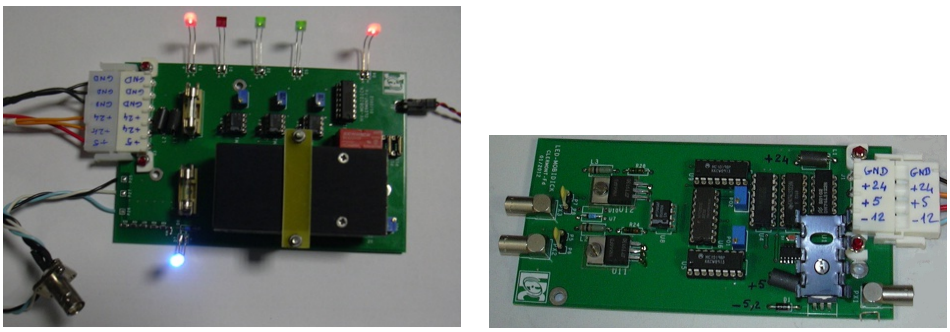


Figure 5. The Trigger ADC board

3.4 HV and LED driver

A new version of the HV board has been produced for the MobiDICK4 system. This new custom board implements a high voltage power supply that is activated using a TTL controlled relay. It has two independent voltage inputs of +5 V and +24 V, and provides an output of -830 V for the operation of the PMTs on the front-end.

A second custom board implements the functionality of the LED driver. A monostable operated by a TTL input generates a pulse that is used to drive the LED with 20 ns pulses necessary for calibration of the super-drawer readout channels. Recall here that on the previous versions of MobiDICK, the HV and LED driver were implemented on the same board. These boards are displayed on figure 6.



(a) New HV board (b) New LED driver

Figure 6. HV and LED driver boards

3.5 CANbus

Two CANBus interfaces are available to communicate with the HV and integrator ADC in the super-drawers. RS232 ports of the motherboard are used to send and receive commands and transform them into the CAN protocol using a commercial adapters [10]. These two CANBus adapters replace the TVME200 card which holds the TIP816 in the previous test bench version.

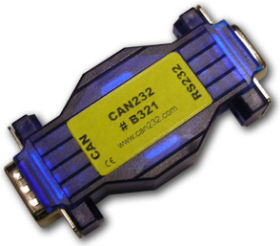


Figure 7. CANbus commercial adapter

3.6 The embedded system

An embedded Linux with Kernel version 2.6.39 has been chosen as the OS for the PowerPC, mainly because of the wide support for the microprocessor and the availability of drivers for Xilinx IP

cores. An automatic boot of the whole system (bitstream + kernel + root file system) is performed from the CompactFlash using the System ACE Controller. The ELDK 4.2 cross compiler tools [11] are used for building the Linux OS image and cross-compiling applications for the PowerPC architecture.

The processor is connected to its peripherals using a PLB 4.6. These peripherals are modeled as IP cores, some of which are commercial and provided by Xilinx and the rest being HDL-written custom IPs, developed to satisfy the test bench specific needs.

The different custom boards of the test bench are interfaced to the embedded system by means of HDL firmware modules in the FPGA in one side, and required libraries for the applications that run on the server on the other side.

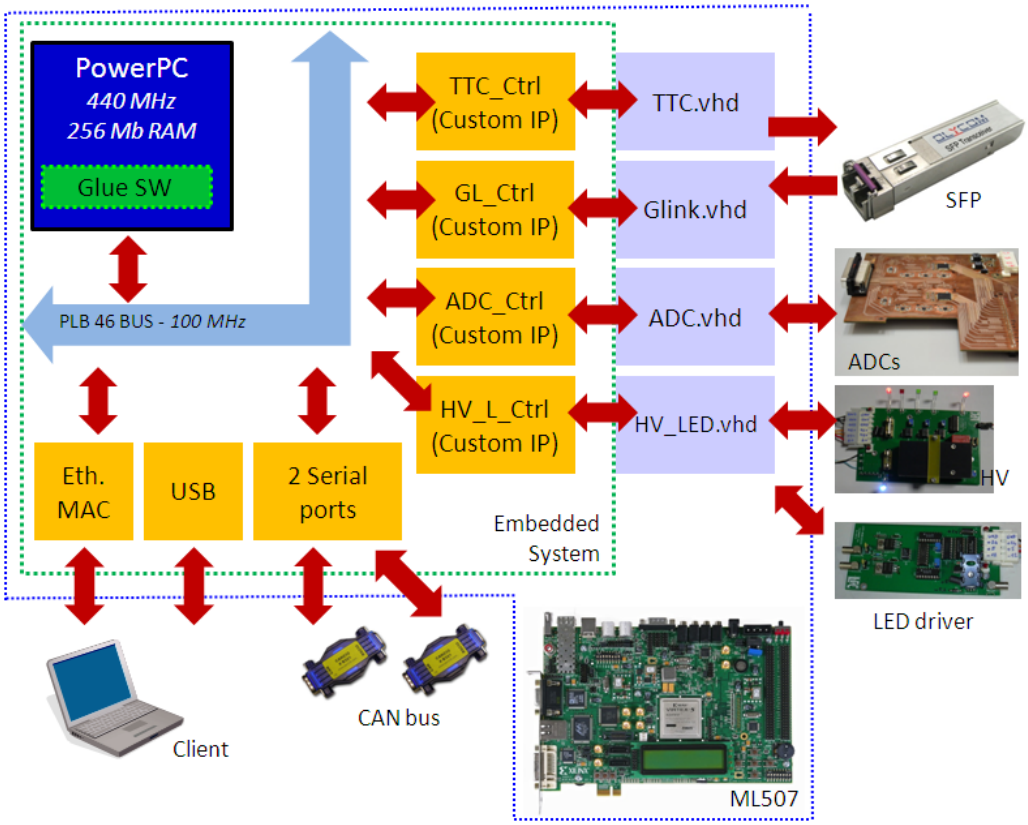


Figure 8. MobiDICK4 embedded system

3.7 Software

The software follows the client-server architecture of previous test bench versions . Now the server runs on the FPGA embedded processor instead of the VME processor. Glue software substitutes the VME libraries.

The tests performed by the system on the super-drawers are divided into eleven sets, in the following order: CommMB, Adder, DigShape, DigNoise, Integ, CommHV, DigNoiseHV, Opto, NominalHV, IntegHV, DigShapeLED.

- Motherboard Communication: This is a simple test designed to check the communication with the front-end. The motherboard TTCrx address is verified.
- Trigger Output: This test measures the signal provided by the analog summation cards in response to a known charge applied by the charge injection circuit (CIS) to these cards one by one.
- Digital Shape: The purpose of this test is to compare the ouptut pulse shape of the PMTs to the reference pulse of the CIS. Two different charges are injected in order to check the high gain and the low gain circuits. This test also tries to detect a missconnection between 3-in-1 card and digitizer channel.
- Digital Noise with and without HV: These tests have been designed to measure the digitizers noise and to check the data integrity. Ten seconds of data at a 100 KHz rate are acquired. The BCIDs of each TileDMU, and all CRCs are checked on the fly by a HDL algorithm. The pedestal average level and RMS for each channel are also verified.
- Integrator Linearity with and without HV: Here it is desired to check the linearity and noise level of the ADC-I and of the charge integrator circuit of the 3-in-1 cards. The pedestal RMS is calculated and verified. A DAC configured to provide an increasing value is connectedd to the charge integrator circuit input. The signal on the charge integrator circuit output is digitized, and the linearity of the resulting curve is checked.
- HV Communication: This test checks the communication with the high voltage distribution electronics. The communication with the HVmicro card is established and its satus register and software version is verified. The values of the voltages and temperatures monitored by the HVmicro are measured. The serial numbers of the HVmicro and the HVopto are crosschecked with those stored in the super-drawer database.
- Opto and Nominal HV: Two tests certify the functionalities of the high voltage distribution electronics. The HV switches are verified, as well as the HV output values for each channel.
- Digital Shape with LED: The purpose of this test is the same as the one for Digital Shape, but using a LED instead injecting the charge. The LED driver outputs are connected to two small boxes containing a blue LED that will excite the PMT. The pulse applied to the LED is synchronized with the trigger signal sent to the super-drawer. The digitizers data are then read out and analyzed.

3.8 Conclusions

During the foreseen shutdown of the LHC in 2013, maintenance tasks will be performed to the front-end electronics. The super-drawers will have to be certified prior the start of their operation in data taking conditions. MobiDICK is the test bench designed to perfom all the necessary tests to verify the super-drawers. Since there are three units of this test bench, and the four TileCal partitions have to be tested at the same time, a new MobiDICK is required. The obsolescence of some electronic parts present on the first versions of the test bench makes mandatory a new approach in the design of MobiDICK. This has been achieved in MobiDICK4 substituting the

modular-electronics-based system of the previous versions with a programmable logic platform. The functionality of the test bench has been obtained building a complete system on programmable chip, and the obsolete parts as well as many other modules have been emulated using hardware description languages. Some new libraries have been developed and the existing software has been re-written when needed in order to adapt it to the new hardware.

Acknowledgments

The authors want to thank all pepole who have contributed to the development of this new test bench, especially those who spent many hours and put a lot of effort to push this project through.

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