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DOCTORAL THESIS

Design and Characterization of an Analogue Amplifier for the Readout of Micro-Pattern Gaseous Detectors

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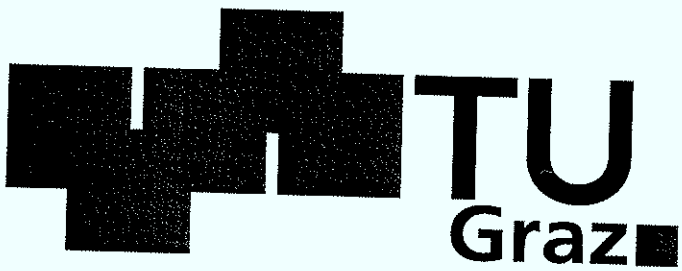

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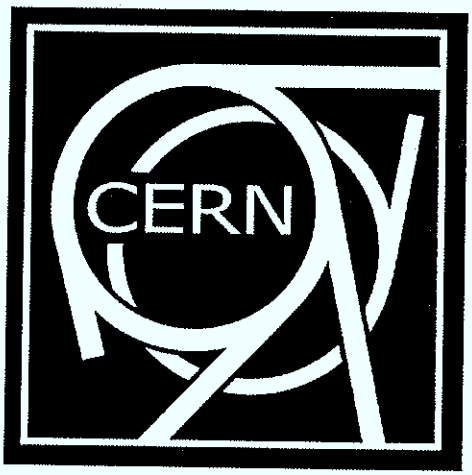

This work has been carried out through the Austrian Doctoral Student Program at the European Organization for Nuclear Research, CERN, Geneva, Switzerland

Abstract

This doctorate deals with the development of integrated analog preamplifiers for the readout of micro pattern gaseous detectors. Because of the small detector signals the noise performance of the readout electronics is of greatest significance. The design of analog preamplifiers constitutes a trade-off between bandwidth, noise, power consumption, radiation hardness and chip area.

A prototype IC consisting of 12 channels was produced in a 0.13 µm CMOS technology. Each channel is comprised of a single ended preamplifier followed by a fully differential shaping amplifier that produces a 4^{th} order semi Gaussian pulse. Channels with different peaking time, conversion gain and preamplifier architectures were implemented. Among these a novel rail to rail preamplifier architecture for low voltage operation.

Part of the thesis work was the design of a printed circuit test board and the characterization of the prototype ICs. The measurements show very good correlation with the simulated values and the circuit fulfills all specifications.

Current state-of-the-art detector readout systems consist of sensitive analogue circuitry, ADCs and high-speed digital processing whereas the low-noise preamplifiers are still kept separately. New R&D is therefore needed to develop cost-effective single chip solutions with a higher degree of integration and programmability and reduction of the power consumption.

Starting from the prototype IC, a programmable 16 channel preamplifier/shaping amplifier was designed as analog front-end for a general purpose charge readout chip.

Kurzfassung

Die vorliegende Doktorarbeit beschäftigt sich mit der Entwicklung von analogen integrierten CMOS Vorverstärkern für die Auslese von Micro Pattern Gasdetektoren. Aufgrund der kleinen Detektorsignale ist das Rauschverhalten der Ausleseelektronik von besonderer Bedeutung. Der Entwurf eines analogen Vorverstärkers stellt einen Trade-Off zwischen Bandbreite, Rauschen, Leistungsverbrauch, Strahlungshärte und Chipfläche dar.

Ein Prototypchip mit 12 Kanälen wurde in einer 0,13 µm CMOS Technologie gefertigt. Die einzelnen Kanäle bestehen aus einem Vorverstärker (single ended) gefolgt von einem differentiellen Pulsformer vierter Ordnung. Die Kanäle unterscheiden sich in Verstärkungsfaktor und Anstiegszeit der Impulsantwort. Verschiedene Vorverstärkerarchitekturen wurden implementiert. Darunter eine neuartige Rail to Rail Architektur für niedrige Versorgungsspannungen.

Teil der Arbeit ist die Charakterisierung des Prototyp-ICs und das Design eines Testboards. Die Messergebnisse zeigen gute Übereinstimmung mit den simulierten Werten, und der Prototyp-IC erfüllt alle gestellten Anforderungen.

State of the Art Auslesesysteme bestehen aus hoch sensitiven analogen Vorverstärkern mit nachfolgenden digitalen Signalprozessoren, wie in Kapitel eins beschrieben. Die gemeinsame Integration von Analog- und Digitalelektronik ermöglicht die Implementierung von schnellen, kosteneffizienten Auslesesystemen mit einer hohen Anzahl von Kanälen bei gleichzeitig kleinem Leistungsverbrauch.

Ausgehend von dem Prototypchip wurde ein programmierbarer Chip mit 16 Kanälen als analoges Frontend für einen General Purpose Charge Readout Chip entwickelt.

Summary and Outlook

This doctorate is within the framework of the R&D activities of the Electronics Design (ED) group at CERN Physics (PH) Department and is carried out under the supervision of Dr. Luciano Musa (CERN) and Univ.-Prof. Dr. Hans Leopold (Graz University of Technology).

The next generation of experiments in hadron physics must be able to measure and identify interesting rare reaction products amongst a very high background of non-interesting events. The high luminosity and multiplicities that will be provided by new facilities at CERN, GSI and BNL, require development of detector techniques based on large area, high granularity and high speed.

Gaseous detectors have been widely used in the field of high energy physics up to now. Features like cost efficiency, fast signals, good energy and spatial resolution make them indispensable for modern detector systems like the Large Hadron Collider (LHC) experiments. Over the last decades many different particle multiplication methodologies have been developed. The use of Multi Wire Proportional Chambers (MWPC) for particle multiplication is still state of the art. An example is the ALICE (A Large Ion Collider Experiment) Time Projection Chamber (TPC) at CERN. Modern lithography and etching technologies triggered the development of Micro Pattern Gaseous Detectors (MPGD). These are high granularity detectors with small distances between anode and cathode. GEM (Gas Electron Multiplier) and MICROMEGAS (MICRO MEsh GAseous Structures) are two examples of these new MPGD.

Small signals generated by detectors are amplified by means of highly sensitive low noise analog circuitry. Current state-of-the-art readout systems consist of analogue preamplifiers and high-speed digital signal processing whereas the low-noise preamplifiers are still kept separately.

This thesis focuses on the design of analog front-end electronics and consists of the following main steps:

- Research on analog front-end electronics for detector readout
  - Feasibility study of a shaping filter in the discrete time domain
  - Feasibility study of a charge sampling circuit
  - Studies on the analog front-end for a general purpose charge readout chip
  - Studies on a programmable PreAmplifier and Shaping Amplifier (PASA)

- Development of a PASA prototype in a 0.13 µm CMOS technology
  - Specification of the algorithms to be implemented by means of simulation based experimental data

- Development of Matlab and Spice models for the functional verification of the circuit
- Circuit design (schematic and layout)
- Low power optimization of the various circuits elements
- Test of the circuit

- Design of a programmable PASA in a 0.13 µm CMOS technology

The demand of high granularity, high speed, low cost and low-power electronics calls for a close integration of analogue and digital circuits. Therefore, a major research challenge is to integrate high-speed digital electronics with low-noise analogue electronics in a single chip. R&D is needed to develop a cost-efficient single chip solution with higher degree of integration and programmability. This new IC, a General Purpose Charge Readout Chip, has to be very flexible in order to be able to cover as many different applications as possible. To cope with this requirement programmability has to be added to the analog signal processor which results in an increase of complexity. Various different architectures were investigated:

Sensitivity to Input Signals of both Polarities

It is absolutely necessary for a general purpose charge readout chip that its analog front-end is capable of processing input signals of both polarities. Therefore a circuit was developed that allows setting the internal DC voltages according to the expected input signal polarity.

Conversion Gain

The primary object of changing the conversion gain is to make the circuit suitable to a wide range of detectors. It is mandatory to adapt the gain of the first stage to the expected maximum input charge to avoid saturating the amplifier. Due to process imperfections gain calibration is of great significance to achieve a homogenous behavior of all channels. Therefore a circuit was developed that allows calibrating the conversion gain.

Peaking Time

The choice of the correct peaking time is a trade off between several factors like noise, pulse pile-up, time resolution and charge collection time. There is no doubt that different applications have the need of different and constant peaking times over all channels. Modifying the peaking time changes the cut off frequency of the shaping filter that can be realized by an active RC-filter or a GmC filter. The RC-filter profits from higher linearity and the GmC approach promises a wider tuning range of the cut off frequency. At this point, we should not neglect that if one considers the shaping amplifier as an anti-aliasing filter, accurate shaping can also be performed by the digital processor.

Feasibility Study of a Shaping Filter in the discrete Time Domain

A switched capacitor filter would allow very accurate shaping. The filter's frequency behavior is mainly determined by the ratio of capacitors and the clock frequency which could be varied according to the desired shaping time. Unfortunately this approach suffers from the demand for a high clock frequency, especially at short shaping times. A switched capacitor circuit is by definition a sampled data system that has to be preceded by an anti-aliasing filter that would additionally increase the complexity and also the power

consumption. Filtering in the discrete time domain can also be performed by the digital processor.

Resistance of Feedback Resistor

The demand for low noise pushes the value of the discharging resistor into the mega ohm region. To realise a highly ohmic path a transistor that is biased in weak inversion or operates in the linear region is used. The feedback resistance can be modified by changing the biasing conditions of the feedback element. The choice of the feedback resistance is a trade-off between noise performance and possible counting rate.

Rail to Rail Preamplifier

The classical single ended folded cascade amplifier is widely used in the field of low noise analog electronics for the readout of detectors. Especially at low supply voltages like 1.5 Volt in the 0.13 µm CMOS technology severe restrictions in terms of allowable voltage swings arise. In order to fully exploit the available voltage room, a rail to rail preamplifier was developed. This extra voltage swing increases the circuit's high pulse rate capability.

Feasibility Study of a Charge Sampling Circuit

The charge sampling circuit was developed with the idea of having a circuit which gives information about the charge released by the detector within one clock cycle. Simulations have shown that this approach shows comparable charge resolution. Limitations in terms of time resolution can be overcome by modifying the basic principle.

Prototype

The prototype circuit consists of a single ended charge sensitive amplifier that is followed by a fully differential 4^{th} order shaping filter that produces a semi Gaussian pulse with a peaking time of 100 ns. The circuit is designed in a 0.13 µm IBM technology. In order to reduce the complexity and gather some more experience with the new technology a non programmable architecture was chosen. It is sensitive to the opposite signal polarity like the actual preamplifier and has very similar pinout. Small modifications of the ALICE-FECs (Front End Cards) are necessary to use the prototype-IC for the readout e.g. of GEM (Gas Electron Multiplier) detectors.

The available silicon area of the prototype run was 3 mm^2. Due to this limitation only 12 of the previously planned 16 channels were implemented. The prototype circuit is based on 5 different channel-architectures that differ in preamplifier architecture, peaking time and gain:

- 7 channels — pmos folded cascode preamplifier, 100 ns shaping amplifier
- 1 channel — thin oxide pmos regulated folded cascode preamplifier, 100ns shaping amplifier
- 2 channels — pmos input rail to rail preamplifier, 100 ns shaping amplifier
- 1 channel — pmos input rail to rail preamplifier, triple gain, 100 ns shaping amplifier
- 1 channel — pmos folded cascode preamplifier, 50 ns shaping amplifier

40 dies were fabricated and packaged by an external company.

Part of the thesis work has been the design of the test board and the characterization of the prototype circuits. The measurements show very good matching with the simulated values and the circuit fulfills all given specifications.

Starting from the first prototype, the design of a new chip is currently in progress. The submission is planned for the 2nd quarter of 2007. The programmable amplifier includes some of the programmability features presented in this thesis and offers a standby mode.

Specifications of the Programmable Charge Amplifier:

- Conversion gain: Programmable in the range of 10-30 mV/fC
- Peaking time: Programmable in the range of 30-100 ns
- Signal polarity: Programmable for positive and negative pulses
- Power consumption: < 8 mW/channel (<1 mW in standby mode)
- Area: 0.2 mm^2/channel
- Number of channels 16
- Technology CMOS 130 nm

This circuit will be employed for the readout of the Large Prototype TCP of the International Linear Collider in the year 2008. Furthermore, this new circuit will become the analog front-end for the General Purpose Charge Readout Chip described above.

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Chapter 1

Introduction

1.1 Gaseous Detectors

Gaseous detectors have been widely used in the field of high energy physics up to now. Features like cost efficiency, fast signals, good energy and spatial resolution make them indispensable for modern detector systems like the Large Hadron Collider experiments. Over the last decades many different particle multiplication methodologies have been developed. The use of Multi Wire Proportional Chambers (MWPC) for particle multiplication is still state of the art. An example is the ALICE (A Large Ion Collider Experiment) Time Projection Chamber (TPC) at CERN.

1.1.1 Time Projection Chamber – TPC

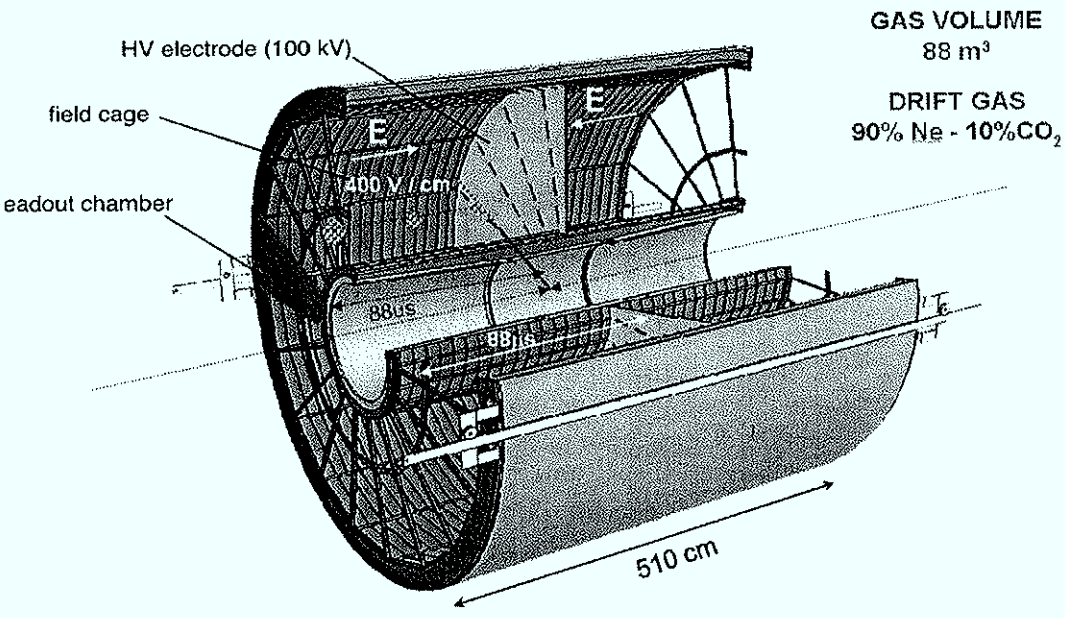


Figure 1 Alice TPC

The TPC is the main part of the Alice tracking system. Because of the low mass, the detection medium has very little influence on the particle that has to be detected. This is an example for nondestructive detection of charged particles. A charged particle traversing the detector produces primary electrons by ionizing gas atoms. The applied electric field makes

electrons to move towards the anode whereas the positively charged ions drift towards the cathode. The electrons are detected in highly segmented readout chambers. By applying center of gravity algorithms information about the exact point of arrival is obtained. Through measurement of the arrival time the three dimensional particle track can be reconstructed.
The TPC allows particle identification because the collected charge at the pad plane is a function of the primary particle's energy loss.

1.1.2 Energy Loss

A charged particle traversing a medium looses energy in many different ways. Interactions due to the strong and weak force are much less probable than interactions due to the electromagnetic force. The incoming charged particle leads to excitation and ionization of the medium. The contribution of other effects like Bremsstrahlung, Cherenkov and transition radiation to the total deposited energy is negligible in gas detectors. The energy loss is a statistical process that was described by Bethe and Bloch in the framework of relativistic quantum mechanics. The average differential energy loss per unit length is given by: [1]

$$-\frac{1}{\rho}\frac{dE}{dx} = K\frac{Z}{A}\frac{1}{\beta^2}\left[\ln\left(\frac{2mc^2\beta^2 E_M}{I^2(1-\beta^2)}\right) - 2\beta^2\right] \tag{1.1}$$

$$K = \frac{2\pi N z^2 e^4}{mc^2} \tag{1.2}$$

$$E_M = \frac{2mc^2\beta^2}{1-\beta^2} \tag{1.3}$$

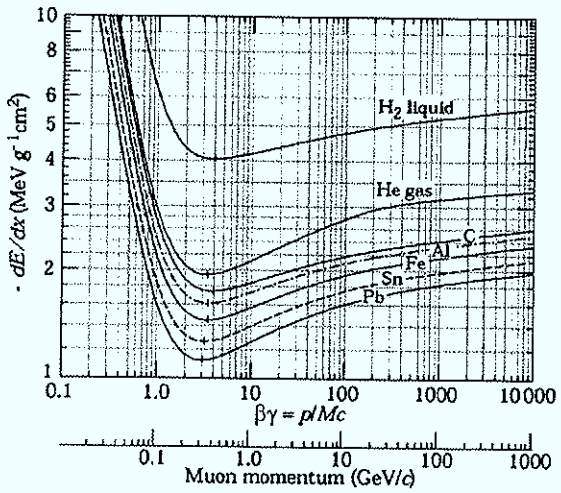


Figure 2 Energy loss [3]

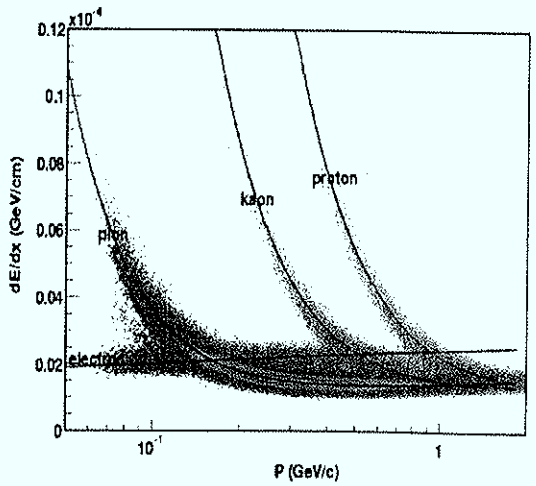


Figure 3 STAR TPC; Energy loss [4]

N	Avogadro number
m, e	Electron mass and charge

Z, A, ρ	Atomic number, mass and density of the medium
E_M	Maximum allowed energy transfer
z, β	Projectile's charge and velocity (in units of the speed of light, c)

1.1.3 Multi Wire Proportional Chamber (MWPC)

A common feature for many detectors is that they can be regarded as capacitive sources from a signal processing point of view. Moving charge in electric fields induces a current on the capacitor electrodes:

$$i = \frac{dQ_S}{dt} = \frac{QE}{V_B}\frac{dr}{dt} = \frac{QE}{V_B}v \qquad (1.4)$$

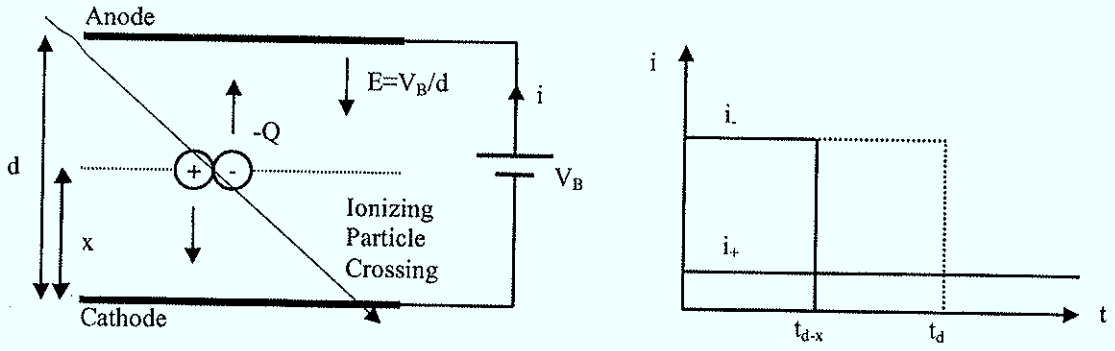


Figure 4 Signal formation in a detector

The charge deposited is given by the integral of the current:

$$Q_S = Q_{S+} + Q_{S-} = \int_x^0 \frac{QE}{V_B}dr + \int_x^d \frac{-QE}{V_B}dr = \frac{QE}{V_B}x + \left[\frac{-QE}{V_B}(x-d)\right] = Q \qquad (1.5)$$

The signal consists of an electron- and an ion-induced part. Due to higher mobility, electrons drift much faster to the anode than ions to the cathode. Note that the total charge deposited equals Q.

In many detectors the energy loss is not big enough to generate a signal that can be directly detected by the readout electronics. In such cases the primary electrons have to be further amplified. One of the possible solutions is given by the multi wire proportional chamber. The primary electron drifting towards the anode gets into regions of high electric fields. Ionizing collisions take place if the electron's energy is larger than the ionization energy of the gas. Furthermore through the excitation of gas atoms UV photons provoke photo electrons. An avalanche process is generated that is characterized by the multiplication factor (M). For a cylindrical proportional chamber the electric field around the anode wire is given by: [5]

$$E(r) = \frac{V_B}{\ln\frac{b}{a}}\frac{1}{r} \quad (1.6)$$

$$V(r) = \frac{V_B}{\ln\frac{b}{a}}\ln\frac{r}{a} \quad (1.7)$$

a Anode wire radius
b Cathode radius

$$dq = \frac{Q}{V_B}\frac{dV}{dr}dr \quad (1.8)$$

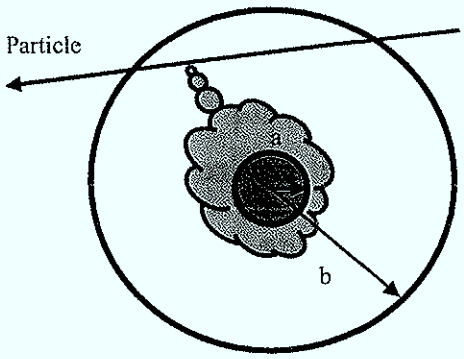


Figure 5 Cylindrical proportional Chamber

Assuming that the entire avalanche process takes place at the distance λ from the anode wire, the deposited charge is given by:

$$Q_- = \frac{MQ}{V_B}\int_a^{a+\lambda}\frac{dV}{dr}dr = \frac{MQ}{\ln\frac{b}{a}}\ln\frac{a+\lambda}{a} \quad (1.9)$$

$$Q_+ = \frac{MQ}{V_B}\int_{a+\lambda}^{b}\frac{dV}{dr}dr = \frac{MQ}{\ln\frac{b}{a}}\ln\frac{b}{a+\lambda} \quad (1.10)$$

$$Q_S = Q_+ + Q_- = MQ \quad (1.11)$$

The electric field is only high enough to initiate the avalanche process close to the anode wire. The distance that electrons drift towards the anode wire is much shorter than the way of the ions. In this case the induced signal is dominated by the ion drift.

1.1.4 Alice TPC Readout

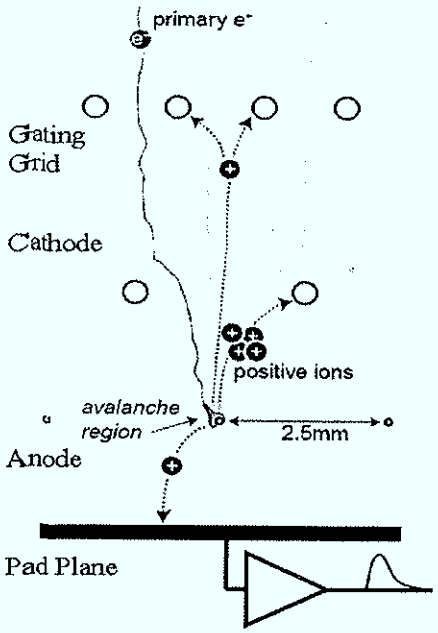


Figure 6 Alice TPC –MWPC [6]

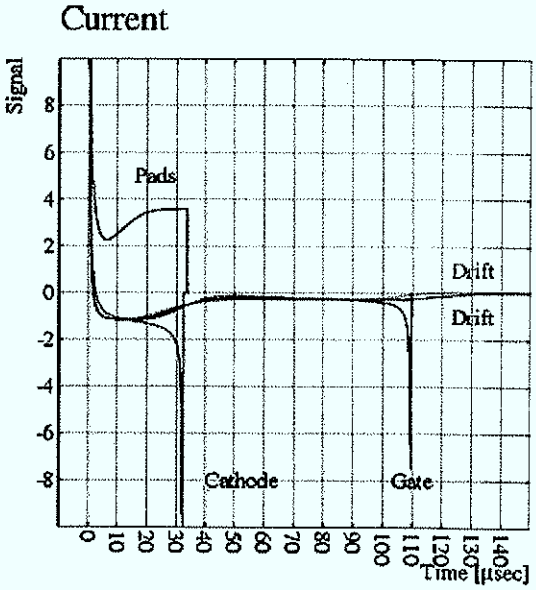


Figure 7 Induced current signal [7]

Figure 7 shows simulation results for the induced current signal at pad, cathode and gate wire. The pad plane is used for the readout. An avalanche process starts at approximately 400 μm from the anode wires. The electron induced signal has a rise time of some ps whereas the ions take between 30 and 110 μs to reach their destination. The ion induced current has a long tail with a rather complex shape.
Printed circuit boards (front end cards) that are connected to 128 pads are used to process the detector data. Figure 8 depicts the front end card that is comprised of 8 CSA (PASA) followed by digital signal processors (ALTRO). Each PASA IC has 16 channels. The ALTRO contains an ADC, a multi event buffer and a digital processor that performs tail cancellation, zero suppression, baseline correction and data formatting.

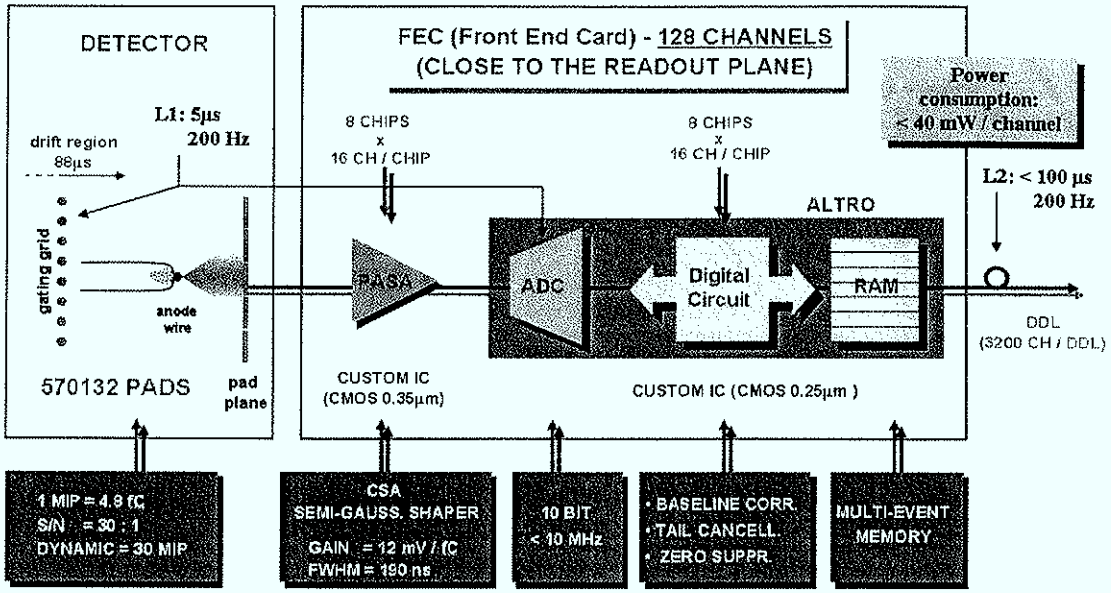


Figure 8 Front-end electronics architecture [7]

Several front end cards are connected to the RCU (Readout Control Unit), another printed circuit board that ships TPC raw data optically to a computer farm where data analysis (e.g. track recognition) is performed.

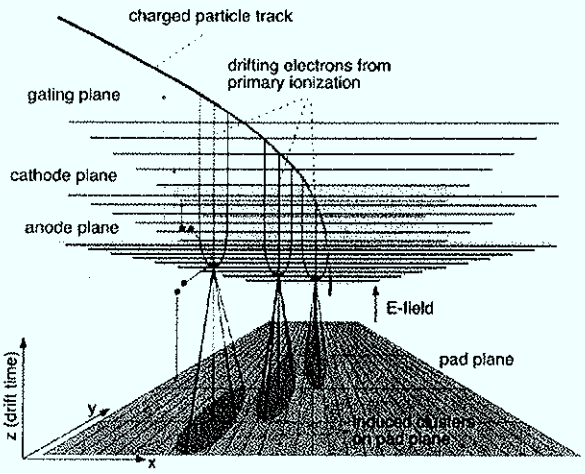


Figure 9 Track reconstruction [7]

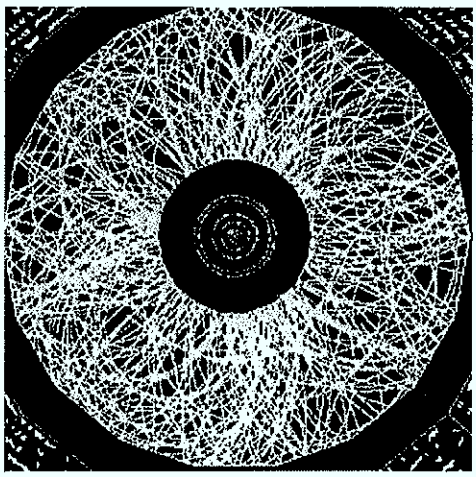


Figure 10 Tracks produced by Pb - Pb collisions [6]

1.1.5 Gas Electron Multiplier (GEM)

Modern lithography and etching technologies triggered the development of Micro Pattern Gaseous Detectors (MPGD). These are high granularity detectors with small distances between anode and cathode. GEM (Gas Electron Multiplier) and MICROMEGAS (MICRO MEsh GAseous Structures) are two examples of these new MPGD.

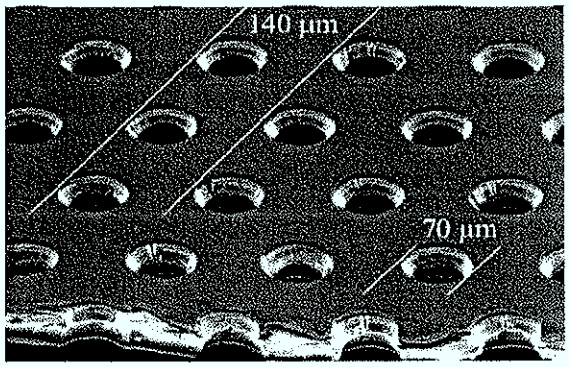


Figure 11 GEM foil, Electron microscope

The gas electron multiplier was first introduced by F. Sauli. A thin insulating polymer foil with metal on both sides constitutes the basic structure. An etching process forms holes through the metallized foil. A potential difference between the two sides is applied. Electrons drifting along the field lines towards the anode plane have to pass the GEM. The holes are places of high electric fields where the electron multiplying takes place by an avalanche process. The generated ions should be absorbed by the upper metal plane whereas the electron cloud drifts towards the anode. Hence only electrons induce a signal. GEM signals are fast and have no ion tail. The anode plane is a highly segmented printed circuit board with an arbitrary pad structure. [8]

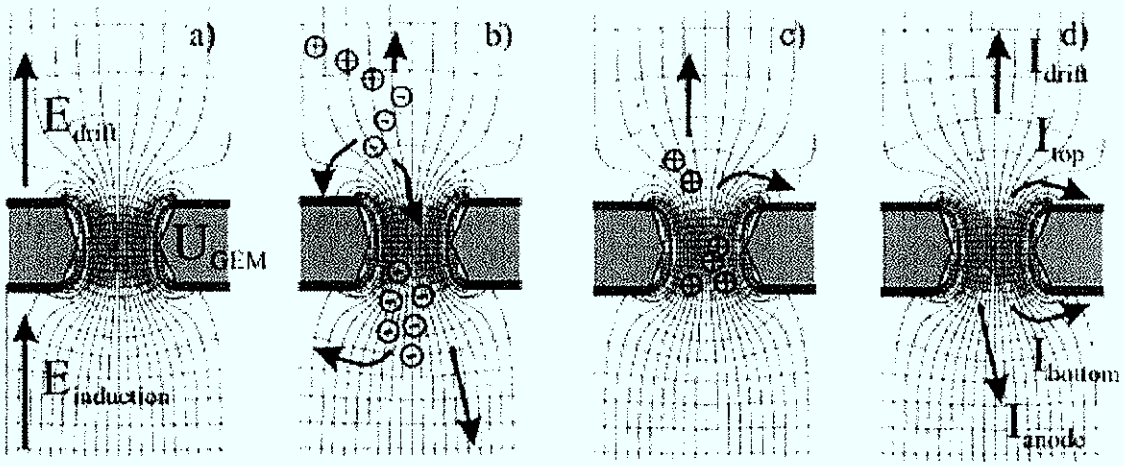


Figure 12 Electron multiplication process [3]

Not all generated ions are absorbed at the upper metal plane. Some drift back to the detector volume. This effect is called ion feedback. Also not all of the generated electrons reach the anode plane. Similar to the MWPC where M determines the gas amplification factor, a ratio (M) determining the effective gain can be defined.

$$M = G_{eff} = \frac{\text{Number or electrons reaching the anode}}{\text{Number or electrons reaching the GEM hole}} \tag{1.12}$$

The gain of a single GEM stage is a function of the applied potential difference. Higher gain can be obtained by a higher voltage difference. An increase in potential difference also enhances the probability of discharge sparks that may damage the detector. Cascading of GEM foils can be applied for cases where high gain is demanded. Each GEM is operated below the discharge limit.

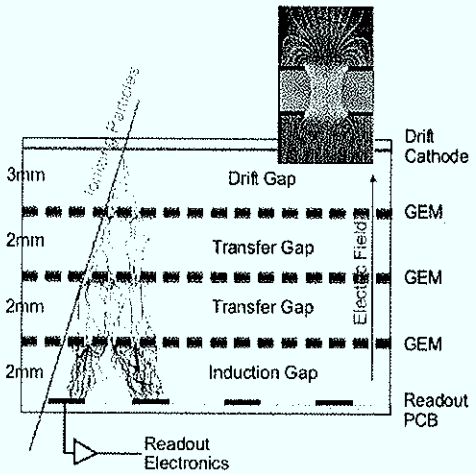


Figure 13 Triple GEM [9]

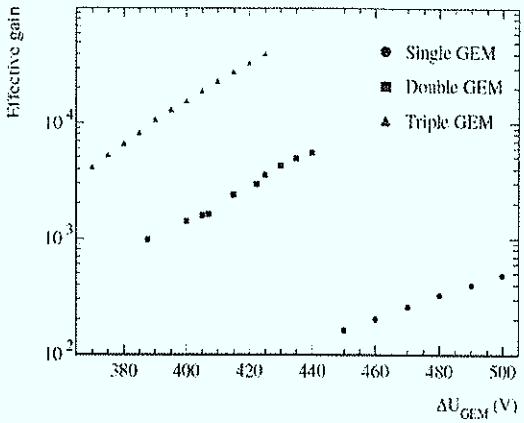


Figure 14 Gain for multiple GEM [9]

Signal Polarity:
The induced signal at the GEM anode plane has the opposite polarity to a signal at the pad plane of a MWPC. In the case of GEM an electron cloud drifting towards the readout plane induces the signal. In the other case positively charged ions drift towards the readout plane and electrons away.

Chapter 2

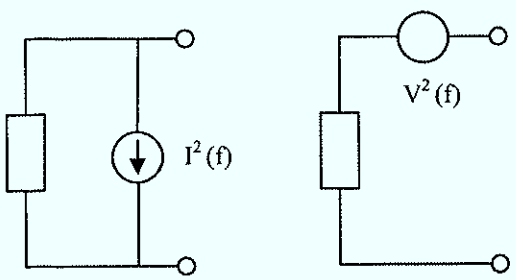
Noise Theory

Noise is present in every electronic circuit and sets the minimum signal level that can be processed. This chapter mainly deals with the intrinsic small current or voltage fluctuations that are generated within the electronic device itself. Any kind of noise from external sources is not subject of this chapter. Noise is of greatest significance when designing an amplifier for charge readout from a detector because it sets an ultimate limit to the minimum detectable charge. A trade-off between power consumption and the amplifiers bandwidth determines the minimum detectable portion of charge.

2.1 Important Noise Sources

2.1.1 Thermal Noise

Noise in a resistor is primarily the result of random thermal motion of electrons and is unaffected by the presence or absence of direct currents. Thermal noise is white in the frequency range of interest and can be characterized by a PSD (Power Spectrum Density). [10]



$$I^2(f) = \frac{4kT}{R} \quad (2.1)$$

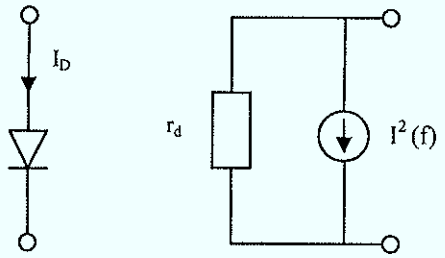
$$V^2(f) = 4kTR \quad (2.2)$$

Figure 15 Representation of thermal resistor noise

k	Boltzmann constant
T	Temperature in Kelvin
R	Resistance in Ohm
$I^2(f)$	Single sided PSD of thermal noise current in A^2/Hz
$V^2(f)$	Single sided PSD of thermal noise voltage in V^2/Hz

2.1.2 Shot Noise

Shot noise is associated with a direct current flow and is present in diodes and bipolar transistors. It results from the discrete movement of charge across a potential barrier. Thermal noise is present even without a current flowing through a resistor.
In the past shot noise did not play an important role in the noise characterization of MOSFETs. But nowadays the scaling down of the gate oxide thickness entails a gate tunneling current that introduces shot noise. Thermal noise is different from shot noise but is modeled in a similar way. Both show a white frequency spectrum. [11]



$$r_d = \frac{1}{g_m} = \frac{kT}{qI_D} \tag{2.3}$$

$$I^2(f) = 2qI_D \tag{2.4}$$

Figure 16 Diode small signal equivalent circuit [10]

q Electron charge

2.1.3 Flicker Noise

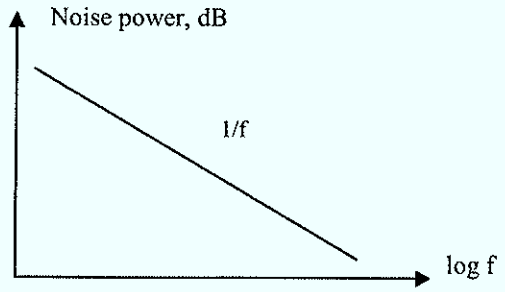


Figure 17 Flicker noise spectral density

Flicker noise is low frequency noise found in all active devices and in many passive components such as resistors. The origin of flicker noise in a MOSFET lies at the interface between the gate oxide and the silicon substrate where many "dangling" bonds appear, giving rise to extra energy states. Charge carriers moving close to the interface are trapped and released randomly which causes current fluctuations. There are several other theories that explain the mechanism of flicker noise. These certainly lie out of the scope of this theses and will therefore not be further considered. [12]
Different from shot and thermal noise the frequency spectrum is not white but pink (1/f behavior). Current or voltage fluctuations caused by flicker noise are concentrated at lower frequencies.

2.2 MOSFET

The input MOSFET has large impact on the noise performance, gain, bandwidth and power consumption of preamplifiers.

2.2.1 MOSFET in Saturation

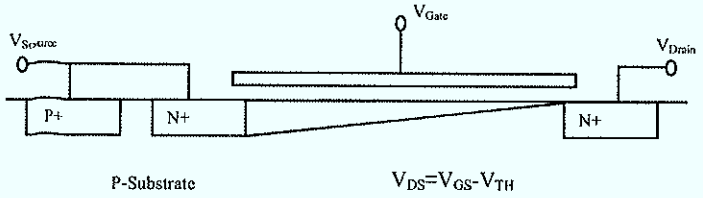


Figure 18 Pinched off channel of a saturated MOSFET

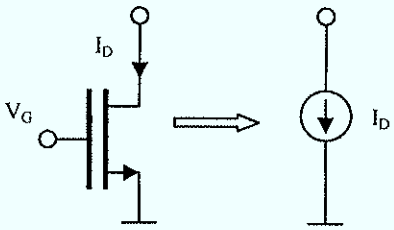


Figure 19 MOSFET as current source

If V_{DS} exceeds V_{GS}-V_{TH} the MOSFET leaves the linear operating region, the channel gets pinched off before it reaches the drain side and the transistor starts to operate in the saturated region. For $V_{GS} > V_{TH}$ the device operates in the strong inversion region and the following equations can be derived: [12]

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2 \tag{2.5}$$

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS},const} = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH}) \tag{2.6}$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS}-V_{TH}} \tag{2.7}$$

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})(1+\lambda V_{DS}) = \sqrt{\frac{2\mu_n C_{ox}(\frac{W}{L})I_D}{1+\lambda V_{DS}}} \tag{2.8}$$

I_D	Drain current
μ_n	Mobility of the charge carriers
C_{ox}	Gate oxide capacitance per unit area
V_{TH}	Threshold voltage
W	Width
L	Length
λ	Channel length modulation factor

2.2.1.1 MOSFET in Weak Inversion

Imagine a device that is operated at constant current. Judging from equation (2.7) it may be assumed that an increase in transistor width would permit to achieve an arbitrarily high g_m.

But if the current is kept constant, then V_{GS} will start to drop until it reaches V_{TH}. At this point the device enters the operating region of subthreshold conduction (weak inversion) and equation (2.7) is no longer valid. The relation between V_{GS} and I_D becomes exponential (similar to the bipolar transistor) and can be expressed by the following equations:

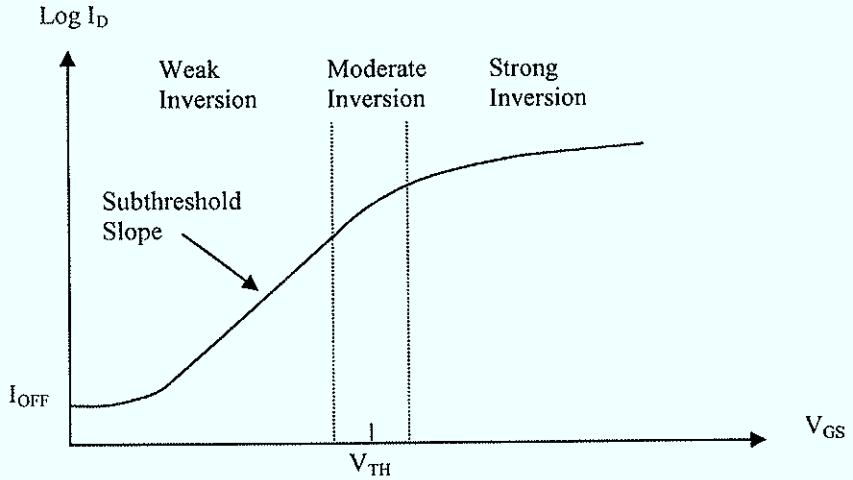


Figure 20 Drain current from weak to strong inversion

$$I_D = I_{D0}\frac{W}{L}e^{q\frac{V_{GS}-V_{TH}}{nkT}} \quad \textbf{(2.9)}$$

$$g_m = \frac{I_D}{nV_T} \quad \textbf{(2.10)}$$

V_T kT/q
n Inverse of the subthreshold factor [11]

2.2.2 MOSFET Noise

2.2.2.1 Poly Gate Noise

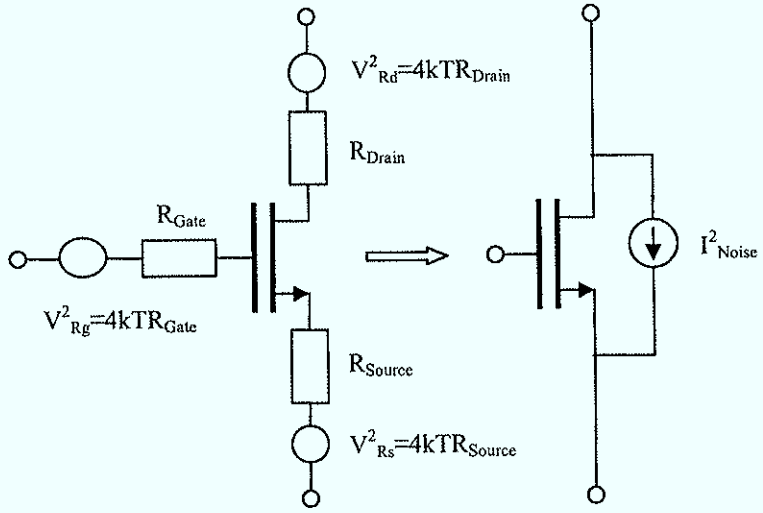


Figure 21 Ohmic noise sources

The most important ohmic noise source is the gate resistance. Input devices for low noise amplifiers are usually laid out with a high W/L ratio which results in negligible source and drain resistances but the gate resistance may not be negligible. Special layout techniques like fingering and metal contacts on both sides of the polysilicon gate help to decrease the gate resistance. If the contribution from drain and source resistance is neglected the following equation for the induced noise current can be derived: [12]

$$I_{Noise}^2 = 4kTR_{Gate}g_m^2 \tag{2.11}$$

2.2.2.2 Thermal Channel and Flicker Noise of a MOSFET

The thermal channel noise is the most significant noise source and can be represented as current source that modulates the drain current or as voltage source that modulates the gate to source voltage. [12]

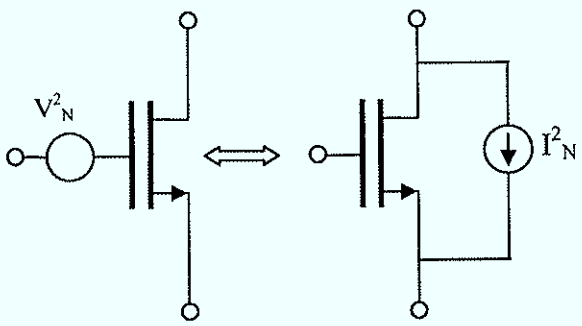


Figure 22 Noise voltage and current equivalent

$$I_{N,channel}^2 = 4kTg_m\lambda \tag{2.12}$$

$$V_{N,channel}^2 = \frac{4kT}{g_m}\lambda \tag{2.13}$$

$$I_{N,flicker}^2 = \frac{K_f g_m^2}{C_{ox}WLf} \tag{2.14}$$

$$V_{N,flicker}^2 = \frac{K_f}{C_{ox}WLf} \tag{2.15}$$

λ	1 for linear operation, 2/3 for strong inversion and 1/2 for weak inversion
K_f	Technology dependent parameter

Since thermal channel and flicker noise are uncorrelated the total noise V_N^2 or I_N^2 can be represented by the sum of the single noise contributions:

$$V_N^2 = \frac{4kT}{g_m}\lambda + \frac{Kf}{C_{ox}WLf} \tag{2.16}$$

2.3 Equivalent Noise Charge (ENC)

Figure 23 shows a typical system for charge measurement. It consists of a preamplifier that is followed by a shaping amplifier. A charge pulse generated by a detector provokes a voltage step at the output of the preamplifier that is proportional to the amplifier gain and inverse proportional to the sum of the capacitances at the input. The amplifier noise is modeled by a series voltage source v_{ns}^2 that is composed of a white and an inverse proportional to frequency part. A parallel current source i_{ns}^2 models current noise. [13]

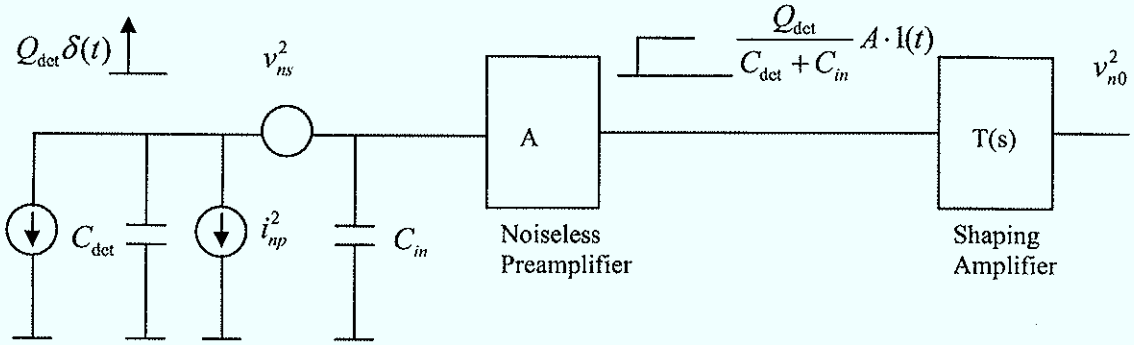


Figure 23 Preamplifier followed by a shaping amplifier

$$v_{ns}^2 = a + \frac{c}{|\omega|} \tag{2.17}$$

$$i_{np}^2 = b \tag{2.18}$$

$$C = C_{det} + C_{in} \tag{2.19}$$

For further calculations it proves more useful to convert the parallel current noise into an equivalent series voltage source. The total noise at the preamplifier output is described by $N(\omega)$.

$$N(\omega) = A^2 \cdot (a + \frac{b}{(\omega C)^2} + \frac{c}{|\omega|}) \tag{2.20}$$

The system's response to an infinitely short current pulse is given by the shaper step response (integrating behavior of the preamplifier):

$$v_o(t) = \frac{A}{C} \cdot L^{-1}\left(\frac{T(s)}{s}\right) \tag{2.21}$$

L^{-1} Inverse Laplace transform operator

In order to determine the maximum signal to noise ratio the maximum signal amplitude is calculated:

$$MAX[v_o(t)] = MAX\left[\frac{A}{C} \cdot L^{-1}\left(\frac{T(s)}{s}\right)\right] \tag{2.22}$$

The system's output noise is calculated by:

$$\overline{v_{n0}^2} = \int_{-\infty}^{\infty} N(\omega) \cdot |T(j\omega)|^2 \, df = \frac{1}{2\pi} \int_{-\infty}^{\infty} N(\omega) \cdot |T(j\omega)|^2 \, d\omega \tag{2.23}$$

$$SNR = \frac{Q_{\det} \cdot MAX\left[\frac{A}{C} \cdot L^{-1}\left(\frac{T(s)}{s}\right)\right]}{\overline{v_{no}^2}^{\frac{1}{2}}} \tag{2.24}$$

The noise performance of detector electronics is usually expressed in terms of ENC (Equivalent Noise Charge) that is defined by the amount of charge at the input of the amplifier that is needed to produce the amplifier's intrinsic output noise. To calculate ENC, SNR in equation (2.24) is set equal to 1 and the following expression is obtained:

$$Q_{\det} = ENC = \frac{\left\{\frac{1}{2\pi} \int_{-\infty}^{\infty} \left[C^2 \cdot \left(a + \frac{c}{|\omega|}\right) + \frac{b}{\omega^2}\right] \cdot |T(j\omega)|^2 \, d\omega\right\}^{\frac{1}{2}}}{MAX\left[L^{-1}\left(\frac{T(s)}{s}\right)\right]} \tag{2.25}$$

Equation (2.25) shows how the contribution of the serial noise sources to the overall ENC scales with the input capacitance.

2.3.1 Parallel Noise

Parseval's Theorem:

$$\int_{-\infty}^{\infty} |X(f)|^2 \, df = \int_{-\infty}^{\infty} |x(t)|^2 \, dt \tag{2.26}$$

$$v_o(s) = \frac{A}{C} \cdot \frac{T(s)}{s} \quad \rightarrow \quad T(s) = \frac{v_o(s) \cdot s \cdot C}{A} \tag{2.27}$$

$$\overline{v_{n0\,parallel}^2} = \frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{b}{(\omega C)^2} \cdot |T(j\omega)|^2 \, d\omega = \frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{b \cdot |(j\omega C)|^2}{(\omega C)^2} \cdot |v_o(j\omega)|^2 \, d\omega = \int_{-\infty}^{\infty} b \cdot v_o(t)^2 \, dt \tag{2.28}$$

The output noise due to the parallel input noise is proportional to the area of the pulse.

2.3.2 Series Noise

$$v_o'(t) = L^{-1}[s \cdot v_o(s)] \tag{2.29}$$

$$\overline{v_{n0serieswhite}^2} = \frac{1}{2\pi}\int_{-\infty}^{\infty} a \cdot |T(j\omega)|^2 \, d\omega = \frac{1}{2\pi}\int_{-\infty}^{\infty} a \cdot |(j\omega C)|^2 |v_o(j\omega)|^2 \, d\omega = \int_{-\infty}^{\infty} C^2 \cdot a \cdot v_o'(t)^2 \, dt \tag{2.30}$$

The output noise due to the series input noise is proportional to the integral of the first derivation of the pulse shape.

$$\overline{v_{n0series1/f}^2} = \frac{1}{2\pi}\int_{-\infty}^{\infty} \frac{c}{|\omega|} \cdot |T(j\omega)|^2 \, d\omega = \frac{C^2}{2\pi}\int_{-\infty}^{\infty} c \cdot |\omega| \cdot |v_o(j\omega)|^2 \, d\omega \tag{2.31}$$

2.3.3 Case Study Triangular Shaping

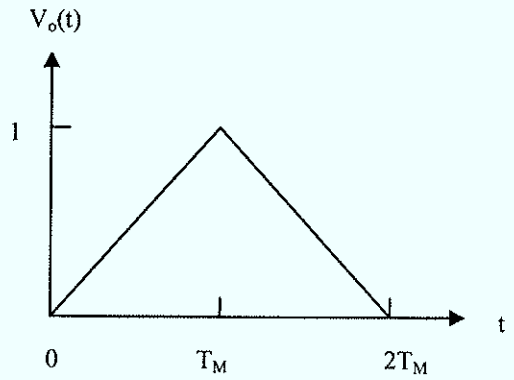


Figure 24 Triangular pulse shape

$$MAX[v_o(t)] = 1$$

$$ENC^2 = \frac{v_{no}^2}{MAX[v_o(t)]} \tag{2.32}$$

$$\overline{v_{n0serieswhite}^2} = ENC_{serieswhite}^2 = \int_{-\infty}^{\infty} C^2 \cdot a \cdot v_o'(t)^2 \, dt = C^2 \cdot a \cdot \frac{2}{T_M} = C^2 \cdot a \cdot \frac{A_1}{T_M} \tag{2.33}$$

$$\overline{v_{n0series1/f}^2} = ENC_{series1/f}^2 = \frac{C^2}{2\pi}\int_{-\infty}^{\infty} c \cdot |\omega| \cdot |v_o(j\omega)|^2 \, d\omega = C^2 \cdot c \cdot 0.88 = C^2 \cdot c \cdot A_2 \tag{2.34}$$

$$\overline{v_{n0parallel}^2} = ENC_{parallel}^2 = \int_{-\infty}^{\infty} b \cdot v_o(t)^2 \, dt = b \cdot \frac{2}{3} \cdot T_M = b \cdot A_3 \cdot T_M \tag{2.35}$$

$$ENC^2 = ENC_{serieswhite}^2 + ENC_{series1/f}^2 + ENC_{parallel}^2 \tag{2.36}$$

From the foregoing calculations a general equation can be derived where A_1, A_2 and A_3 are constant factors that depend only on the pulse shape geometry. Series noise can be

suppressed be choosing a longer shaping time but this increases the noise contribution from current noise. A very interesting result is that the series flicker noise contribution is independent of the shaping time. [14]

$$ENC^2 = C^2 \cdot a \cdot \frac{A_1}{T_M} + C^2 \cdot c \cdot A_2 + b \cdot A_3 \cdot T_M \qquad (2.37)$$

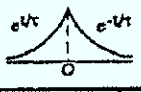
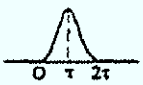
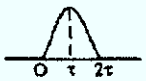
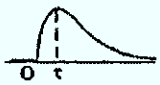
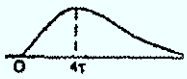
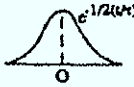
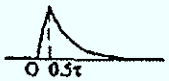
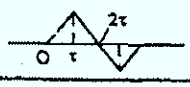
	Shaping	h (t) Function	A_2	$\sqrt{A_1 A_3}$	$\frac{A_2}{\sqrt{A_1 A_3}}$	A_1	A_3	$\sqrt{\frac{A_1}{A_3}}$
1	indefinite cusp		0.64 $\left(\frac{2}{\pi}\right)$	1	0.64	1	1	1
2	truncated cusp	 $k = \tau'/\tau$	k=1 0.77 k=2 0.70 k=3 0.67	1.04 1.01 1	0.74 0.69 0.67	2.16 1.31 1.31	0.51 0.78 0.91	2.06 1.30 1.10
3	triangular		0.88 $\left(\frac{4}{\pi^2} \ln 2\right)$	1.15 $\left(\frac{2}{\sqrt{3}}\right)$	0.76	2	0.67 $\left(\frac{2}{3}\right)$	1.73
4	trapezoidal		1.38	1.83	0.76	2	1.67	1.09
5	piecewise parabolic		1.15	1.43	0.80	2.67	0.77	1.86
6	sinusoidal lobe		1.22	1.57	0.78	2.47	1	1.57
7	RC-CR		1.18	1.85	0.64	1.85	1.85	1
8	semigaussian (n = 4)		1.04	1.35	0.77	0.51	3.58	0.38
9	gaussian		1	1.26	0.79	0.89	1.77	0.71
10	clipped approximate integrator		0.85	1.34	0.63	2.54	0.71	1.89
11	bipolar triangular		2	2.31	0.87	4	1.33	1.73

Figure 25 Important parameters for different pulse shapes [14]

2.3.4 ENC as a Function of Shaping Time

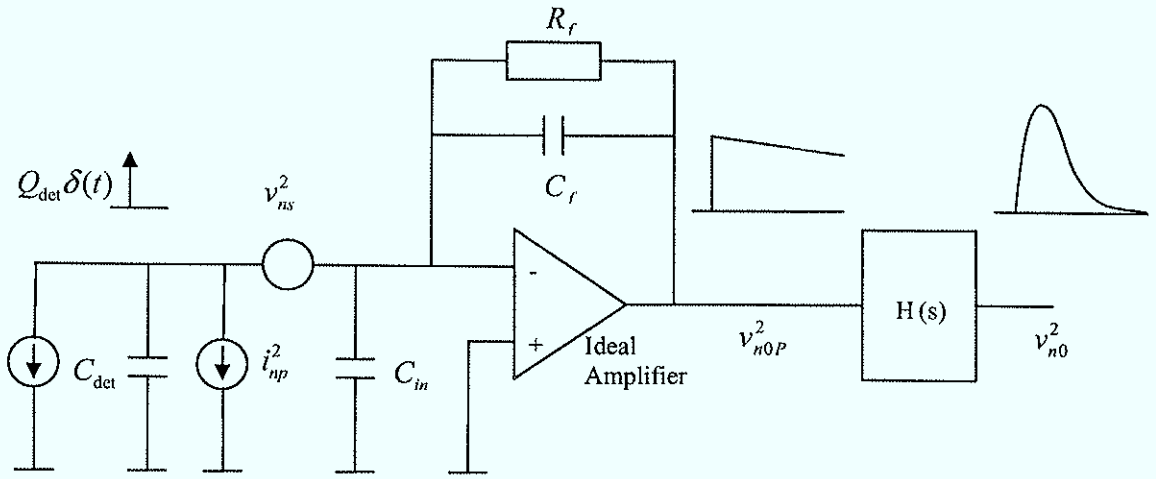


Figure 26 Charge sensitive amplifier followed by a shaping amplifier

The shaping filter after the CSA improves the signal to noise ratio by suppressing specific frequencies. Current noise is reduced by high pass filtering and white series noise by low pass filtering, suggesting the use of a band pass filter. The system peaking time changes by altering the pass band.

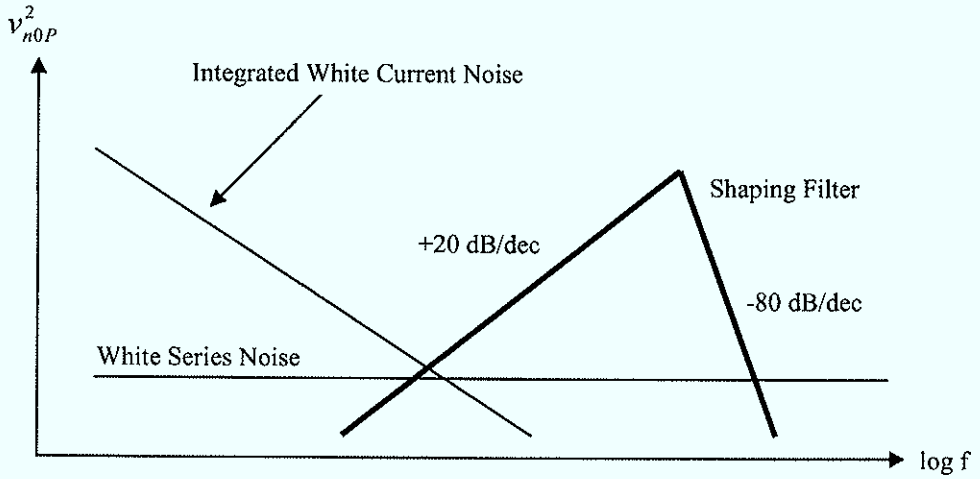


Figure 27 CR-RC^4 Shaper

Assuming that the only noise contributors to v_{nO}^2 are the CSA input transistor and the feedback resistor, equation (2.37) can be written as follows: [28]

$$ENC^2 = (C_{det} + C_{in})^2\left(\frac{A_1 2kTR_s}{T_M} + \frac{A_2 \pi K_f}{C_{ox} WL}\right) + T_M \frac{A_3 2kT}{R_f} \qquad (2.38)$$

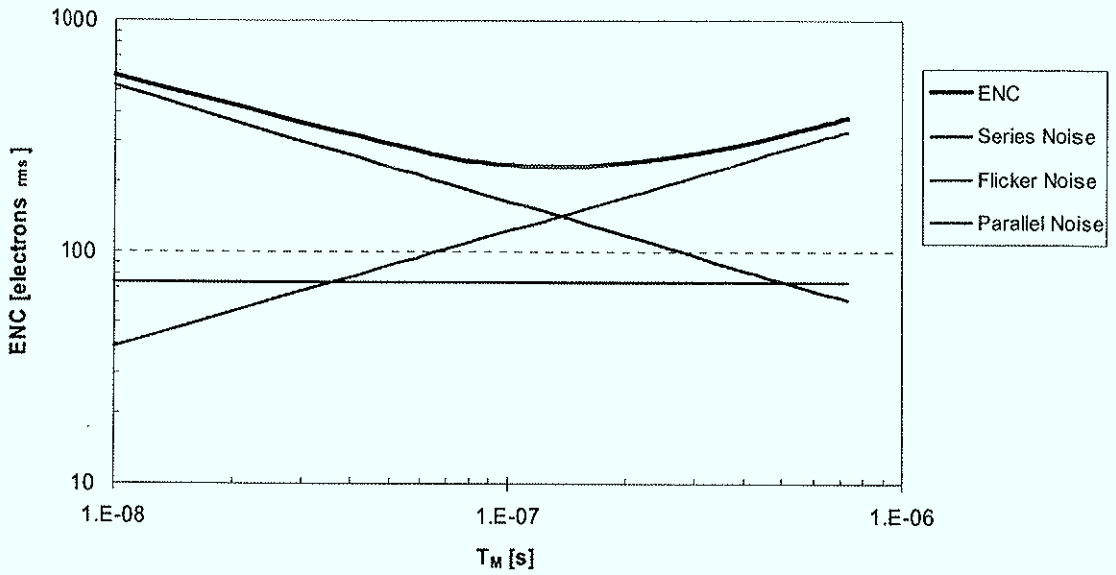


Figure 28 ENC vs. T_M

Parameters for the calculation of ENC:

C_{det}	C_{in}	g_m	R_f	K_f	T	A_1	A_2	A_3
12 pF	3 pF	30 mS	2 MΩ	6e-25	330 K	1.85	1.18	1.85

Table 1

$$R_s = \frac{1}{g_m}\lambda = \frac{1}{g_m}\frac{2}{3} \qquad \text{(Strong inversion)} \tag{2.39}$$

$$c = \frac{\pi K_f}{WLC_{OX}} \approx \frac{\pi K_f}{C_{in}} \tag{2.40}$$

Calculation of the minimum ENC:

$$ENC^{2'} = (C_{det} + C_{in})^2\left(\frac{A_1 2kTR_s}{-T_M^{\,2}}\right) + \frac{A_3 2kT}{R_f} = 0 \tag{2.41}$$

$$T_{M\,min} = (C_{det} + C_{in})\sqrt{\frac{A_1}{A_3}R_s R_f} = 173ns \tag{2.42}$$

$$\tau_C = \frac{1}{T_{M\,min}} \qquad \text{(Noise corner frequency)} \tag{2.43}$$

Signals generated by detectors in high energy physics show very large bandwidth. If the detector pulse is approximated by a delta Dirac impulse (white frequency spectrum), current noise and signal will have the same spectrum after the preamplifier. But why do longer peaking times lead to worse ENC if signal and current noise are affected by the shaper in the same way? This is due to the definition of the ENC that is the ratio of peak

amplitude to rms noise. Equation (2.28) shows that the noise floor due to current noise is proportional to the area of the pulse itself. Keeping the peak amplitude (conversion gain) constant but increasing the shaping time increases the pulse area. This worsens the ratio of peak amplitude and current noise and therefore the ENC.

2.4 Preamplifier Configurations

2.4.1 Pure Capacitive Feedback

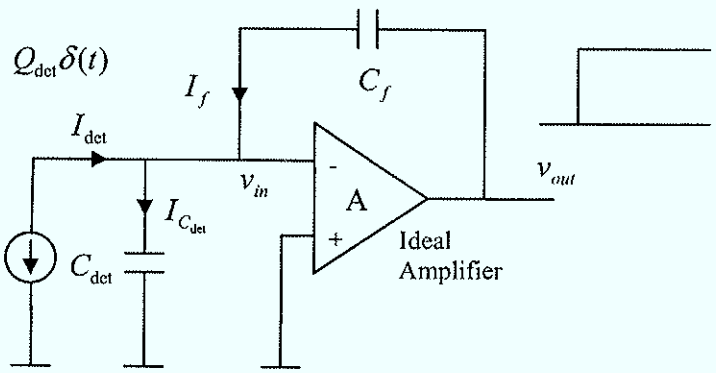


Figure 29 Charge sensitive amplifier

Charge released by the detector is integrated on the feedback capacitance. A finite gain and unlimited bandwidth amplifier will respond to a Dirac impulse with an instantaneous voltage step at the output. Due to the finite gain not all of the released charge will flow through the amplifiers virtual ground.

$$v_{out} = -v_{in}A \tag{2.44}$$

$$v_{out} - v_{in} = v_{C_f} = -v_{in}A - v_{in} = -v_{in}(A+1) \tag{2.45}$$

$$C_{in} = \frac{Q_{C_f}}{v_{in}} = \frac{C_f v_{in}(A+1)}{v_{in}} = C_f(A+1) \tag{2.46}$$

The amplifier input capacitance C_{in} appears in parallel to the detector capacitance. Making C_{in} big enough by choosing an appropriate gain will guarantee that nearly all of the released charge gets integrated on the feedback capacitance. But which portion of charge remains on the detector capacitance?

$$\frac{v_{in}C_{det}}{v_{C_f}C_f + v_{in}C_{det}} = \frac{v_{in}C_{det}}{v_{in}C_f(A+1) + v_{in}C_{det}} = \frac{C_{det}}{C_f(A+1) + C_{det}} = \frac{C_{det}}{C_{in} + C_{det}} \tag{2.47}$$

For a detector capacitance of 20 pF, a feedback capacitor of 500 fF and an amplifier gain of 1000 the portion of charge that remains on the detector capacitance is 3.8%.

In reality the amplifier has finite gain and limited bandwidth that has to be taken into account when analyzing the response of the CSA. In the ongoing analysis a first order model for the amplifier will be used. This constitutes a rather good approximation to reality because CSAs in use are usually built around single stage amplifiers that show only one dominant pole.

$$A(s) = \frac{A_{DC}}{1 + s\tau_P} \tag{2.48}$$

τ_P Pole time constant

$$I_{det} + I_f = I_{C_{det}} \tag{2.49}$$

$$V_{out}(s) = \frac{-I_{det}}{(\frac{C_{det} + C_f}{A_{DC}}) + C_f} \cdot \frac{1}{1 + s\tau_P \frac{C_f + C_{det}}{C_f + C_{det} + A_{DC}C_f}} \cdot \frac{1}{s} \tag{2.50}$$

Equation (2.50) shows how the different parameters modulate the amplifier gain and frequency characteristics. The dependence on the detector capacitance is of greatest importance because it is often not exactly known.

$$R_{in}(s) = \frac{I_{det}}{v_{in}} = \frac{\frac{1}{s} + \tau_P}{C_{det} + C_f + A_{DC}C_f + s\tau_P(C_{det} + C_f)} \tag{2.51}$$

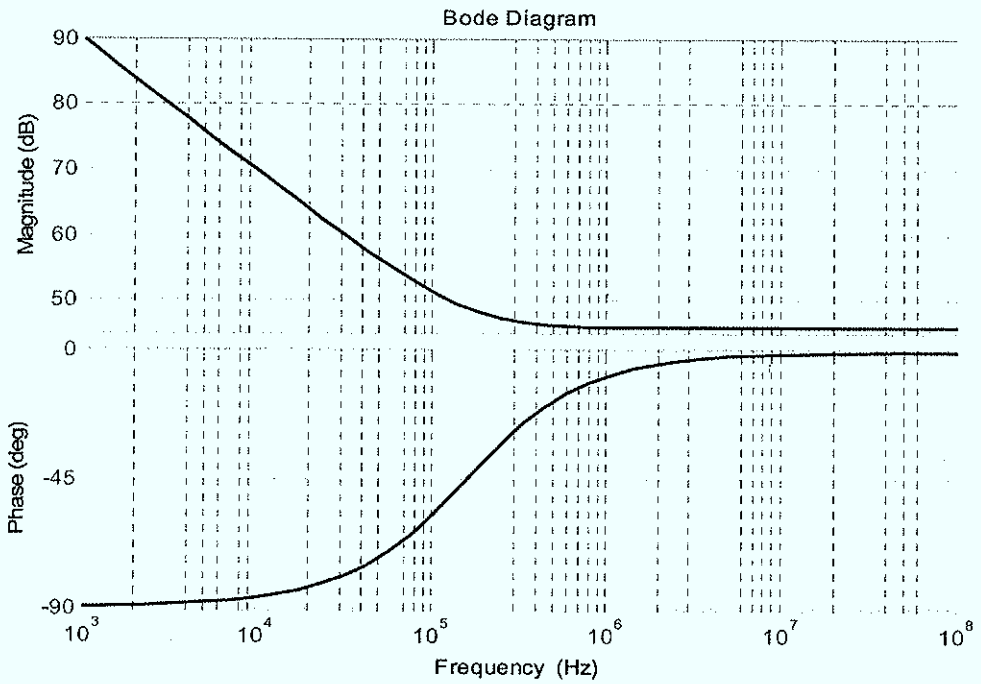


Figure 30 CSA input impedance

$$V_{out}(t) = \frac{-A_{DC} I_{in}}{C_{det} + C_f + A_{DC} C_f} \left(1 - e^{\frac{(C_{det} + C_f + A_{DC} C_f)t}{(C_{det} + C_f)\tau_P}} \right) \tag{2.52}$$

For A_{DC} >>:

$$V_{out}(s) \cong \frac{-I_{det}}{C_f} \cdot \frac{1}{1 + s\tau_P \frac{1}{1 + A_{DC} \frac{C_f}{C_{det}}}} \cdot \frac{1}{s} \tag{2.53}$$

2.4.2 Current Sensitive Configuration

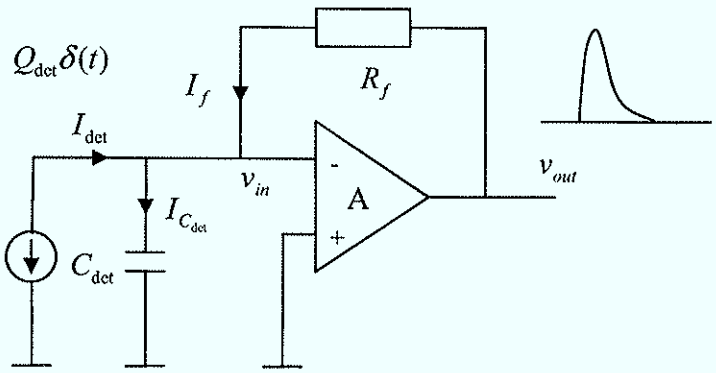


Figure 31 Current sensitive

An alternative to the CSA is the current sensitive configuration where the feedback capacitor is replaced by a pure resistance. The input impedance is given by the feedback impedance divided be the amplifier gain. In spite of capacitive feedback the input capacitance will not swamp the detector capacitance. By choosing an appropriate amplifier gain the input resistance can be made small enough so that it is effectively the current signal from the detector that is amplified. Ideally no charge remains on the detector capacitance. Depending on the application a resistance in the MΩ region is often mandatory to suppress current noise. In reality it proves difficult to apply highly resistive feedback over a high gain amplifier which results in stability problems.

$$R_{in} = \frac{R_f}{A+1} \tag{2.54}$$

$$R_{in}(s) = \frac{R \cdot (1 + s\tau_P)}{1 + A_{DC} + s(C_{det} R + \tau_P) + s^2 C_{det} R \tau_P} \tag{2.55}$$

$$V_{out}(s) = \frac{-I_{det} A_{DC} R}{1 + A_{DC} + s(C_{det} R + \tau_P) + s^2 C_{det} R \tau_P} \tag{2.56}$$

In order to avoid stability problems practical transimpedance amplifiers have also a small capacitance in parallel to the resistive feedback.

2.4.3 CSA with Discharge Resistor

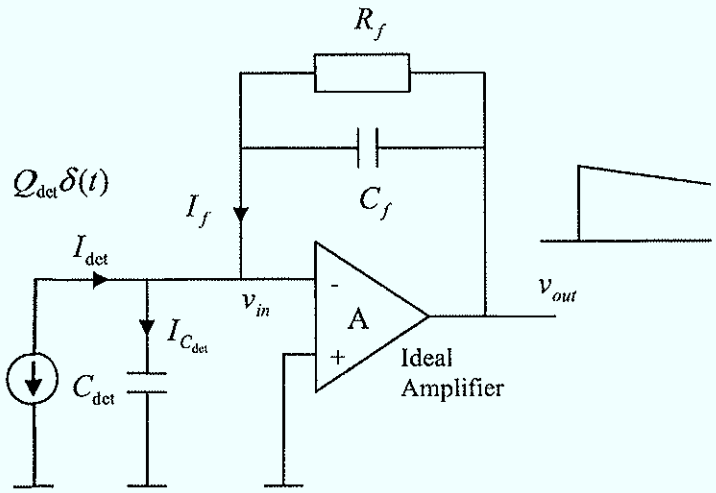


Figure 32 CSA with discharge resistor

The resistor serves as discharge device and sets output and input DC. Depending on the expected event rate the feedback time constant has to be chosen sufficiently small in order to avoid saturating the amplifier. In case of the charge sensitive configuration this resistance can be made very large so that its noise contribution is negligible. This has greatly contributed to the fact that the charge sensitive configuration is widely used in the field of detector readout.

$$R_{in} = \frac{Z_f}{A+1} \tag{2.57}$$

$$R_{in}(s) = \frac{R_f \cdot (1+s\tau_P)}{1+A_{DC}+s(C_{det}R_f + C_fR_f + A_{DC}C_fR_f + \tau_P)+s^2\tau_P(C_{det}R_f + C_fR_f)} \tag{2.58}$$

$$V_{out}(s) = \frac{I_{det}A_{DC}R_f}{1+A_{DC}+s(C_{det}R_f + C_fR_f + A_{DC}C_fR_f + \tau_P)+s^2\tau_P(C_{det}R_f + C_fR_f)} \tag{2.59}$$

If the detector signal is an indefinitely short Dirac delta current impulse the charge collection time will be determined by the preamplifier's rise time. The feedback resistance continuously discharges the feedback capacitance resulting in a loss of amplitude and pulse peaking before all of the detector charge got collected. This effect is called ballistic deficit and takes place if the charge collection time is not negligibly short in comparison to the peaking time of the output pulse. But if the detector does not release charge instantaneously the time profile of the detector current will affect the charge collection time. In detectors with a constant charge collection time, relatively large ballistic deficits can often be tolerated because a constant fraction of the amplitude for each pulse is lost. If the charge collection time varies, a variable amount of each pulse will be lost leading to a loss in terms

of charge resolution. This problem is obviously most severe for those detectors with large variations in charge collection time like proportional counters where the shape of the detector signals in a function of angular spread. [2] [1]

2.4.3.1 Charge Sensitive Mode

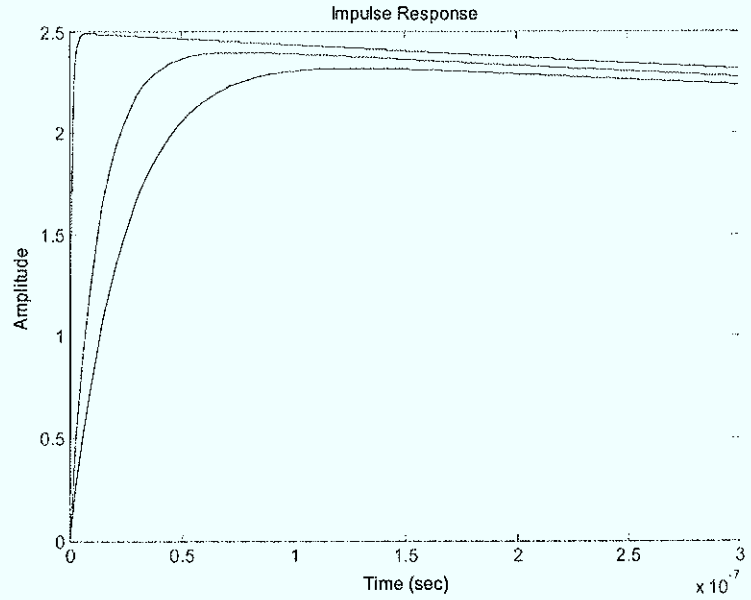


Figure 33 CSA impulse response, increasing C_{DET}

2.4.3.2 Transimpedance Mode

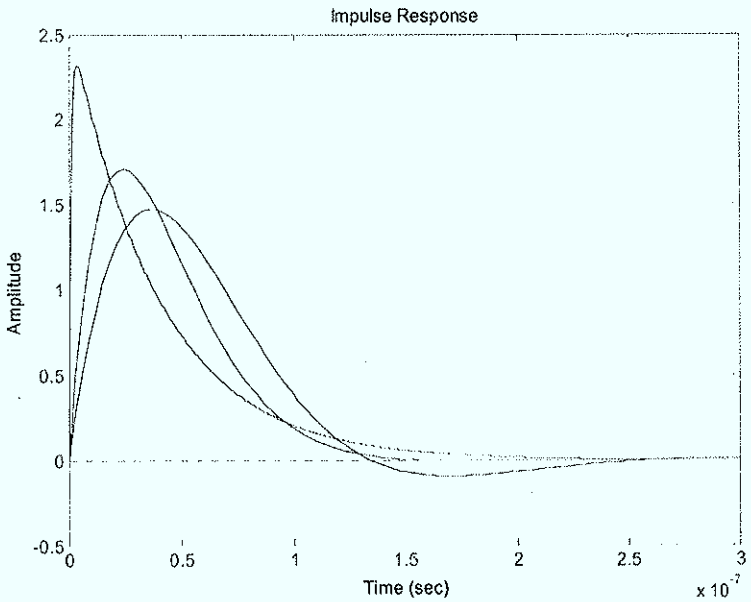


Figure 34 Transimpedance amplifier impulse response, increasing C_{DET}

The preamplifier discharge time constant is in the order of the shaping time.

Chapter 3

Designing in a 0.13 µm CMOS Process

3.1 IBM 0.13 µm CMOS

MOSIS offers access to the IBM 0.13 µm CMOS technology for prototype and low volume fabrication: [15]

- Twin-well CMOS technology on nonepitaxial p-doped substrate
- Low resistance cobalt-silicide n+ and p+ doped polysilicon and diffusion regions
- Supply voltages are 1.2 V core (1.5 V optional) and 2.5 V I/O.
- Broad range of FET devices to optimize power and performance
- High-value, low-tolerance capacitors
- Low tolerance resistors with low and high sheet resistivity
- Four to eight levels of global copper metal

The available technology of the CERN MPWR in December 2005 was the CMOS 8SFG that does not support many components of the analog CMOS 8RF technology.

Selection of available options: [16]

Thin Oxide + Thick Oxide + 3.3 V I/O's	1.2/2.5/3.3 V
Zero-V_{TH} NFET Thin Oxide	1.2 V
Thin Triple Well NFET	1.2 V
Zero-V_{TH} NFET Thick Oxide	2.5/3.3 V
Thick Triple Well NFET	2.5/3.3 V
Regular V_{TH} NFET + Low Power V_{TH} NFET + Low V_{TH} NFET	
Regular V_{TH} PFET + Low Power V_{TH} PFET + Low V_{TH} PFET	
PCDCAP Thin Oxide	Decoupling Capacitor
PCDCAP Thick Oxide	Decoupling Capacitor
VNCAP	Vertical natural Cap.
OP N+ Diffusion Resistor	
OP P+ Poly Resistor	

Table 2

No MIM (Metal Insulator Metal) capacitor was available. Therefore the VNCAP with a capacity density of 1.3 fF/µm^2 (M1-M6) was used as linear capacitor for the filtering stages.

3.2 Short Channel Effects

3.2.1 Hot Carrier Effect

At high lateral fields (see velocity saturation 4.4.3) the average velocity of carriers reaches a saturation level when the energy gained during the acceleration in the electric field equals the lost energy when hitting atoms in the silicon lattice. Impact ionization takes place if the acquired energy of charge carriers is high enough, thereby creating electron hole pairs. The created electrons are absorbed by the drain and the holes by the substrate (drain-substrate current). Due to the high energy of hot carriers they may be injected in the gate oxide where they can get trapped in the gate oxide itself or in the interface between Si and SiO_2. These trapped charges have influence on the threshold voltage (reliability). Gate leakage and substrate leakage current are observed as a consequence of hot carrier effects.
In velocity saturation the transconductance is found to be constant and no longer a function of the current.
The high lateral electric field causes carriers not to be in thermal equilibrium with the silicon lattice. The carriers have higher temperature (hot carriers) and cause therefore higher thermal noise (see 3.2.5). [17]

3.2.2 Mobility Degradation with Vertical Field

Higher gate voltages force the current to flow closer to the interface between oxide and silicon, resulting in more carrier scattering and hence lower mobility. The following equation is an empirical approach to model the lower mobility due to higher gate voltages. [12]

$$\mu_{eff} = \frac{\mu_0}{1+\theta(V_{GS}-V_{TH})} \tag{3.1}$$

θ Fitting parameter

Decreased mobility degrades the performance of MOS transistors by lowering the achievable transconductance and current capability.

3.2.3 Drain Induced Barrier Lowering (DIBL)

In short channel devices the drain potential has an impact on several parameters like threshold voltage and output resistance. Higher drain voltage increases the surface potential, therefore a conducting channel is easier formed. In this way DIBL decreases the threshold voltage.

3.2.4 Output Resistance

For constant output resistance the channel length modulation is modeled by λ that is inversely proportional to L. In reality the output resistance changes as a function of V_{DS}. For higher drain voltages the pinch off point in saturation moves towards the source, this increases the output resistance. As V_{DS} further increases DIBL lowers the threshold voltage and therefore the drain current increases. For even higher drain voltages impact ionization at the drain produces a large current flowing to the substrate and therefore reduces the output resistance.

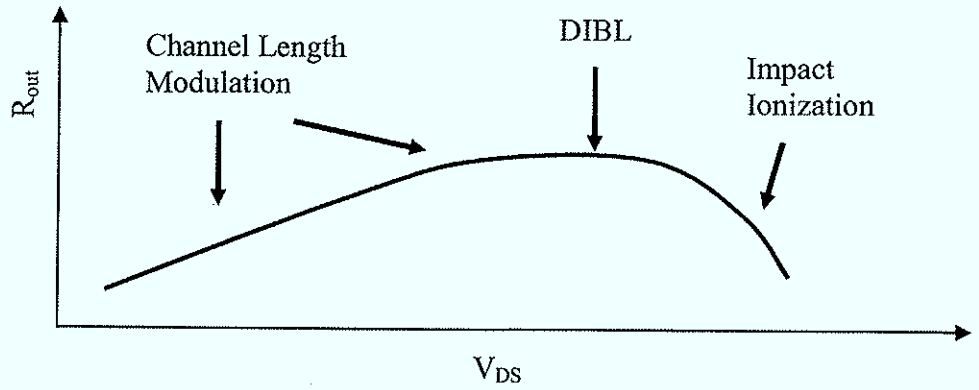


Figure 35 Output resistance vs. drain voltage for short channel devices [12]

3.2.5 Thermal Noise Excess Factor

$$V_{N,channel}^2 = \frac{4kT}{g_m}\Gamma = \frac{4kT}{g_m}\alpha_W n\gamma \qquad (3.2)$$

γ	Between 1/2 for weak inversion and 2/3 for strong inversion
n	Sub-threshold slope factor
Γ	Channel thermal noise coefficient [18]
α_W	Excess noise factor [19]

Effects like velocity saturation, carrier heating, mobility reduction due to the vertical field and channel length modulation are responsible for an increase in thermal channel noise in short channel devices. The effects mentioned above are functions of the biasing conditions. Low V_{DS} is recommended for minimizing the excess noise. [17]

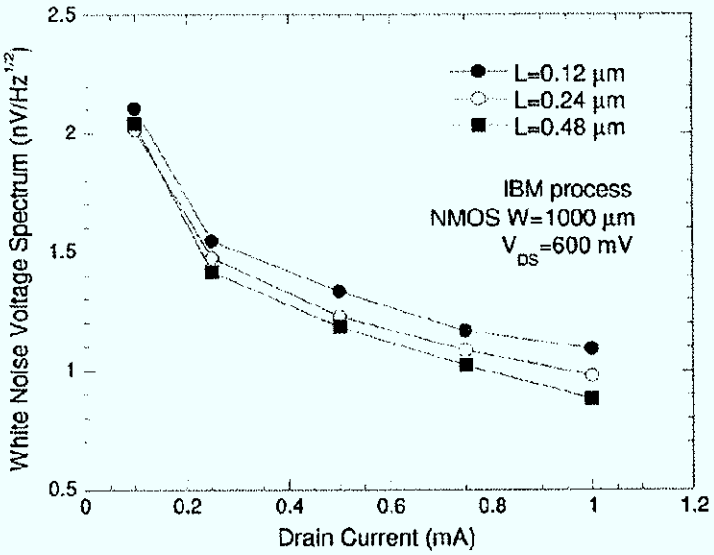


Figure 36 Voltage noise spectrum vs. drain current for three different NMOS transistors

The devices tested in Figure 36 were operated close to weak inversion where the geometry has only little effect on the transconductance as long as the device is kept in weak inversion. Therefore it was assumed that the additional noise component is due to short channel effects. It was observed that $\alpha_W = 1$, except for NMOS transistors with shorter channel length where $\alpha_W = 1.2$. [19]

3.2.6 Flicker Noise

$$V_{N,flicker}^2 = \frac{K_f}{C_{ox} W L f^{\alpha_f}} \tag{3.3}$$

There are different theories about the origin of flicker noise but all of them agree on the formula above where the voltage PSD referred to the gate is inverse proportional to the gate area and frequency. It is expected that PMOS transistors will lose their advantage in terms of flicker noise to NMOS devices in scaling CMOS. The factor α_f determines the noise slope. Its value is process and device dependent (see Figure 37). [17]

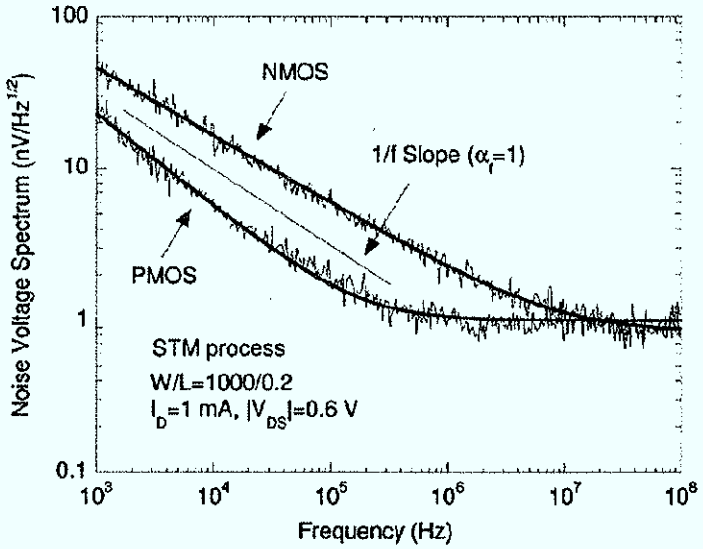


Figure 37 Gate referred noise voltage spectra for NMOS and PMOS devices with the same W/L in a STM 0.13 µm process [19]

The tested devices were operated in moderate inversion at I_D = 1 mA and V_{DS} = 0.6 V. PMOS transistors show steeper noise slopes. From Figure 37 one can see that the PMOS device retains its advantage in terms of flicker noise to the NMOS. Bearing in mind that the transconductance for weak inversion differs only by the sub-threshold factor that was found to be approximately equal in the given IBM process, a PMOS input exhibits better overall noise performance.

3.3 Radiation Effects

3.3.1 Total Ionizing Dose (TID)

Photons, neutral particles, heavy ions, protons and electrons interact in different ways with matter that can be classified by two different effects:

- Displacement
- Ionization

The MOS transistor is more sensitive to ionization than to displacement effects. An incoming particle generates electron hole pairs in conducting and insulating materials. Whereas in the conducting case recombination takes place immediately after the hole pair generation. Electron hole pairs in the gate oxide recombine with much lower probability, depending on the applied electric field. For positive gate bias the generated electrons move towards the gate electrode within some picoseconds whereas the ions drift (lower mobility) towards the Si-SiO_2 interface. Ions can get trapped in the gate oxide or at the Si-SiO_2 interface. This process results in trapped positive oxide charge and radiation induced interface traps. [20]

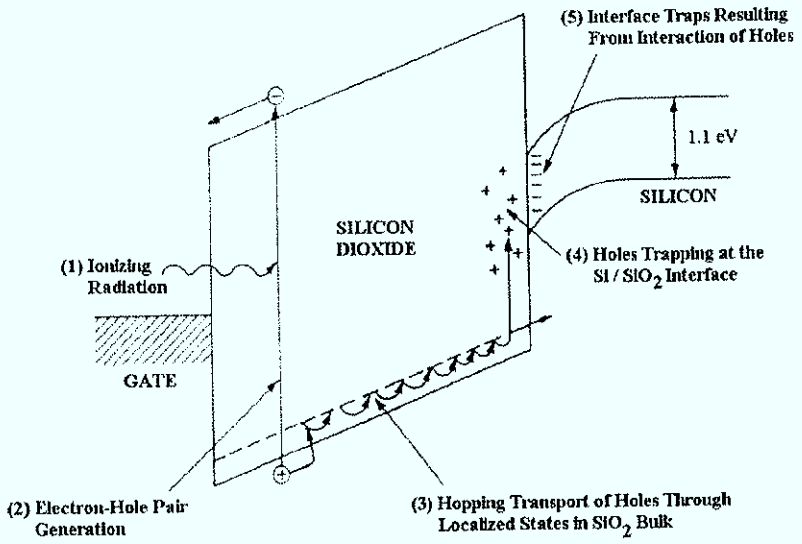


Figure 38 Trapped charge

The consequences of the afore mentioned effects are threshold-voltage shifts, mobility degradation, less transconductance, worsening of matching and increased noise. Since radiation induced trapped oxide charge is always positive the threshold voltage shift is always negative. [21] The bias conditions during radiation have large influence on the effective threshold shift. In submicron NMOS devices the shift tends to be positive. [22]

	Oxide Charge	Interface States	Total Shift
NMOS	-	+	+ or -
PMOS	-	-	-

Table 3

3.3.2 Leakage Currents

Beside the effects described above radiation can also cause parasitic leakage currents. Previously, local oxidation of silicon (LOCOS) was used for inter device isolation. Positive charge build-up in the field oxide, especially in bird's peak regions, moves the parasitic transistor operational point in direction depletion mode. Nowadays in advanced processes shallow trench isolation is used that is planar with the silicon surface and free from lateral encroachment. But this new isolation technique has not improved the intrinsic radiation hardness of commercially available technologies. [23]

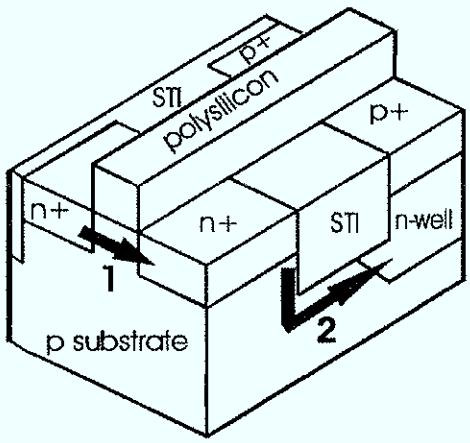


Figure 39 STI leakage current paths

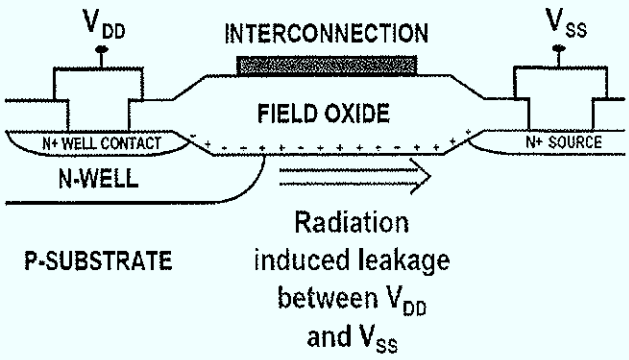


Figure 40 Radiation induced leakage between Vdd and Vss

There are several possible leakage current paths. The corner/sidewall path in a NMOS transistor is indicated as 1 in Figure 39. The inter-device path underneath the shallow trench isolation is indicated as 2 in Figure 39. Guard-rings can be used to overcome inter device leakage (as indicated in Figure 40). [22]

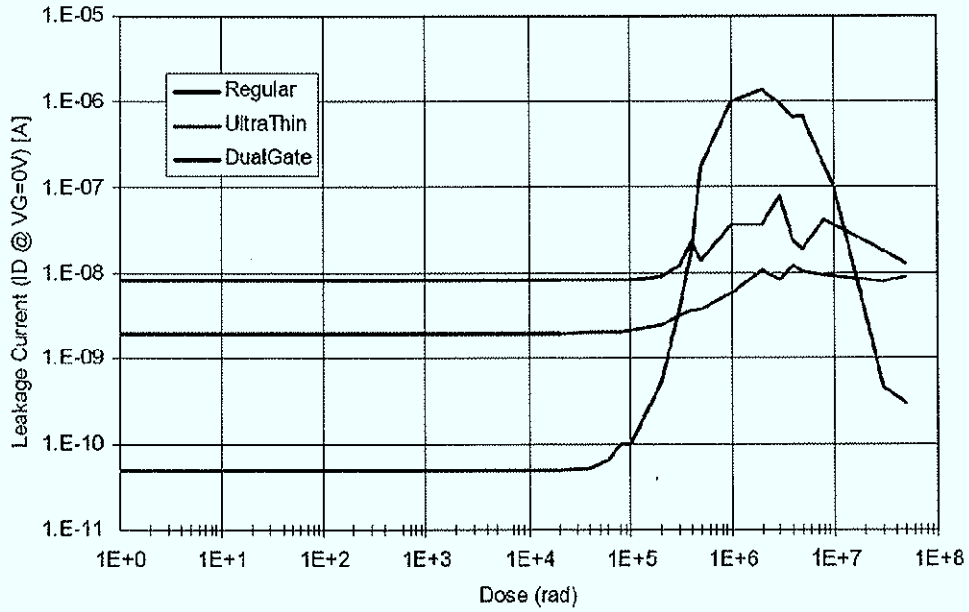


Figure 41 Leakage current measurements for wide linear transistors (W = 10 µm) [24]

3.3.3 Threshold Voltage Shift

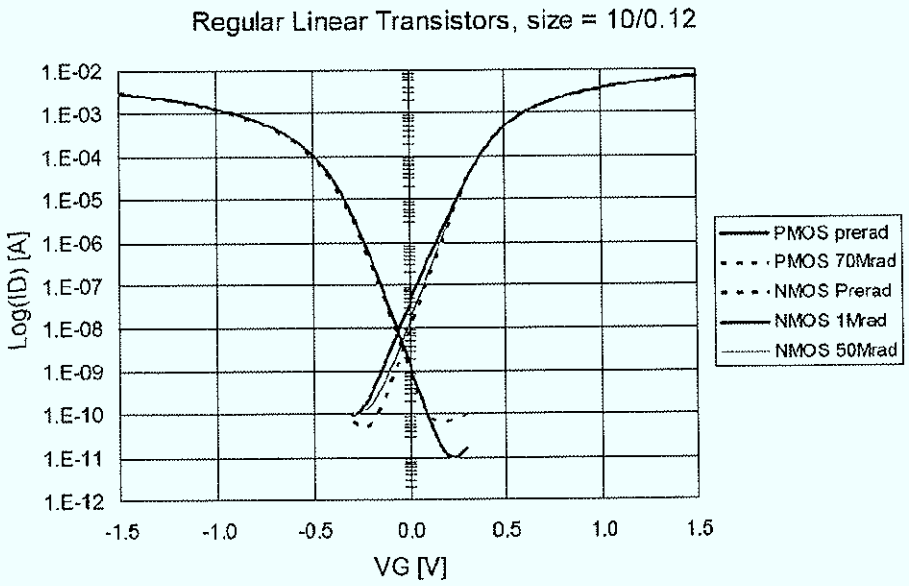


Figure 42 Drain current after radiation

Figure 42 depicts after radiation measurement results for wide linear transistors of the IBM 0.13 µm process. Especially the PMOS transistor shows good tolerance for the given total ionizing dose.

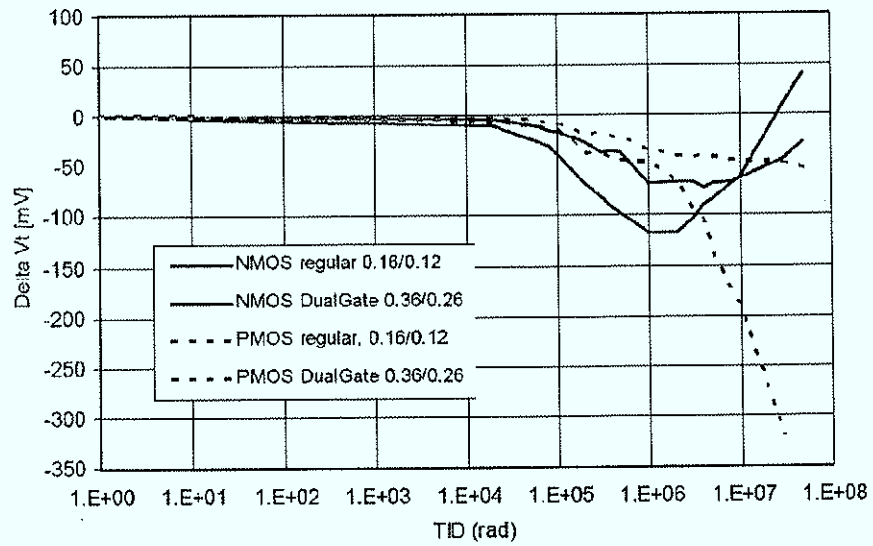


Figure 43 Threshold voltage shift vs. total ionizing dose for different components

Figure 43 depicts measurements for the threshold voltage shift of narrow linear transistors as a function of the total ionizing dose. As expected, devices with thinner gate oxide show less degradation. [24]

3.3.4 Additional Noise

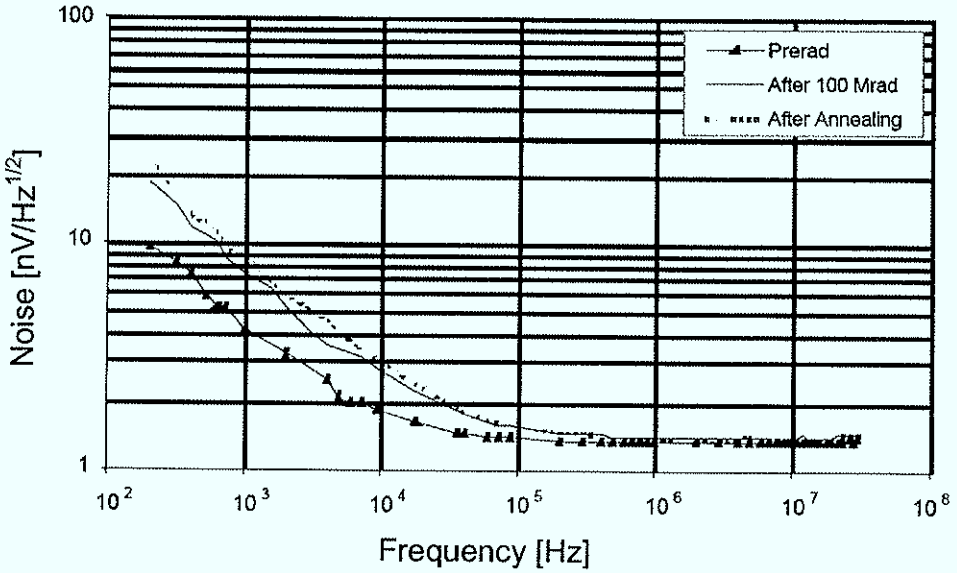


Figure 44 Noise spectrum for PMOS (2000/0.5 µm) before and after irradiation in a IBM 0.25 µm process

In [25] it was found that white noise after 100 Mrad increased by 15% for NMOS and 7% for PMOS. The white noise increase is only slightly higher than expected from the measured decreased transconductance. A correlation between interface traps and flicker noise was observed. The increase of flicker noise up to 100 Mrad is very little.

3.3.5 Layout Techniques

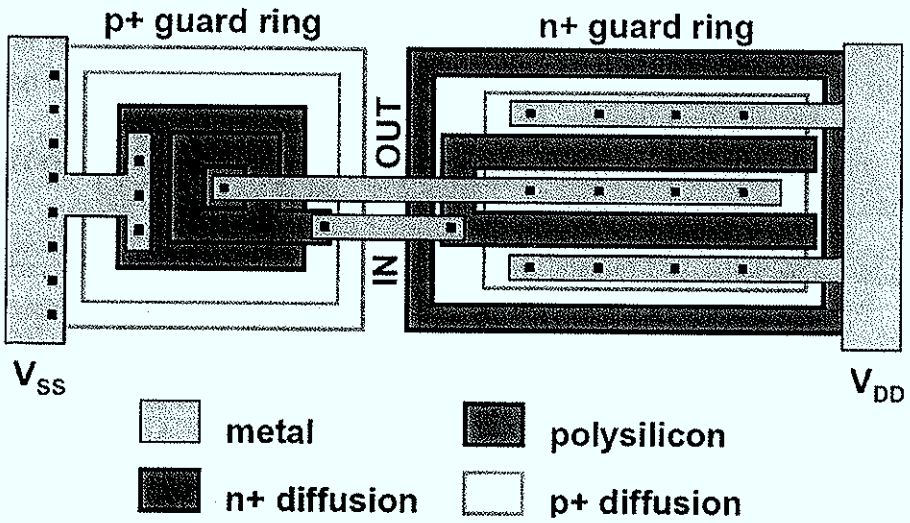


Figure 45 Radiation hard inverter, NMOS enclosed layout

There are several layout techniques to prevent radiation induced leakage. Increasing the length of parasitic transistors can be easily applied. Another approach that is much more effective in terms of radiation hardness is the use of enclosed transistor geometries. In Figure 45 the drain area is surrounded by gate and source. In that way the parasitic sidewall path is avoided. To reduce inter-device leakage guard rings are used. There is a trade-off between radiation hardness and silicon area. In analog design enclosed transistor geometries pose problems to proper modeling and the choice of W/L. [22]
The conventional linear self-aligned poly-gate transistor does not produce the densest possible layout. The waffle transistor uses a mesh of horizontal and vertical poly strips that divides the source/drain implant in rectangles. By alternately contacting these rectangles to source and drain, 4 drains are arranged around one source and 4 sources are arranged around one drain. This architecture yields usually better W/L per silicon area and avoids side leakage. Properly laid out octagonal transistors are less susceptible to ESD but more difficult to lay out and show disadvantages in terms of metallization resistance. [26]

3.4 Conclusions

SEU (single event upset) is a major concern in digital circuits. Single incoming charged particles can deposit enough energy to charge sensitive points and change logic states. In contrary analog circuitry is mainly sensitive to total ionization effects that change transistor parameters like noise, leakage and transconductance. Layout techniques exist to minimize most of these effects. Also radiation hardening by architecture is possible by estimating the threshold voltage shift and designing circuits that can tolerate shifts within certain boundaries. Enclosed transistors with thin gate oxide show good radiation tolerance. For thick gate oxide transistors the threshold shift is not negligible and has to be considered. Large wide linear transistors show promising results. The degradation of transistor parameters seems to be tolerable for a broad range of applications. Narrow linear transistors are more sensitive to radiation effects. [24]

Chapter 4

Prototype Circuit - Design and Layout

4.1 Architecture in Use

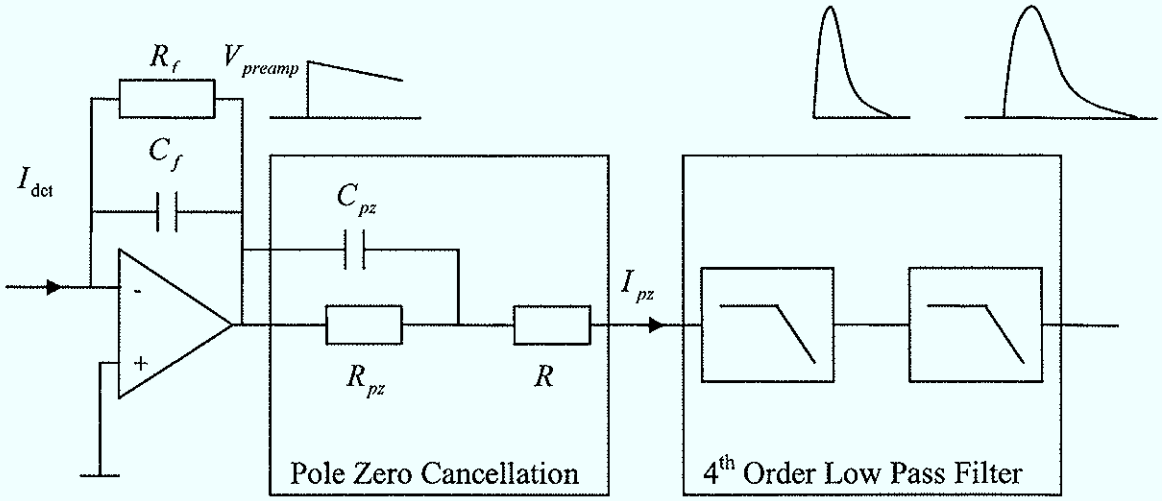


Figure 46 CSA followed by a 4th order shaping amplifier

4.1.1 Semi Gaussian Pulse Shaper

The transfer function of a CR-(RC)^n pulse shaper consisting of one RC differentiating stage and n integrating stages with equal time constants (τ_0) is given by:

$$H(s) = \frac{s\tau_0}{1+s\tau_0} \cdot \left(\frac{Gain}{1+s\tau_0} \right)^n \qquad (4.1)$$

The step response of $H(s)$ is described by a semi Gaussian pulse where n determines the order of the semi Gaussian pulse.

$$V_{out}(t) = \frac{Gain^n n^n}{n!} \cdot \left(\frac{t}{\tau_s} \right)^n e^{-\frac{nt}{\tau_s}} \qquad (4.2)$$

τ_s Peaking time of the semi Gaussian pulse ($\tau_s = n\tau_0$)

By taking the first derivative it can be proven that the pulse reaches its maximum amplitude at the peaking time. [27]

$$V_{out\max} = \frac{Gain^n n^n}{n! e^n} \tag{4.3}$$

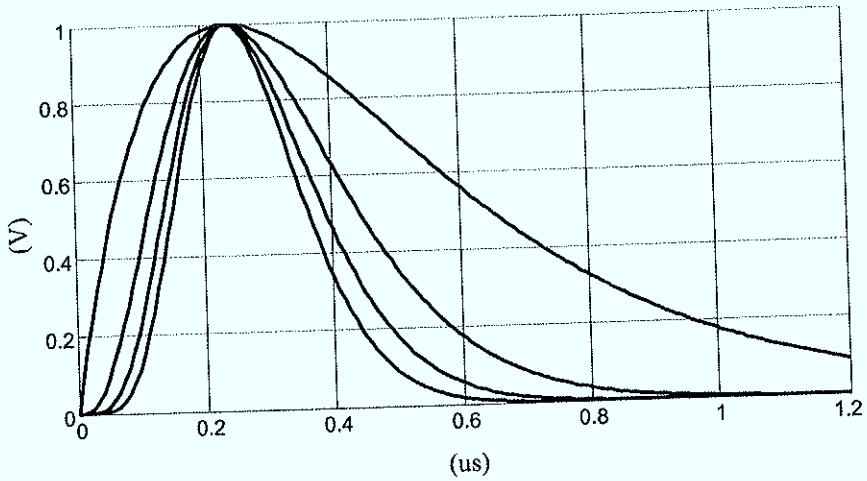


Figure 47 Normalized amplitude and peaking time (n=1, 3, 5 and 7)

Increasing n results in a more symmetrical pulse that becomes a Gaussian pulse for $n = \infty$.

4.1.2 Pole Zero Cancellation

Assuming an ideal preamplifier and low input impedance of the 4th order low pass filter the following equation for I_{PZ} can be derived:

$$V_{preamp} = \frac{-I_{det} R_f}{1 + sC_f R_f} \tag{4.4}$$

$$I_{PZ} = \frac{-I_{det} R_f}{1 + sC_f R_f} \cdot \frac{1 + sC_{pz} R_{pz}}{R + R_{pz} + sC_{pz} R_{pz} R} \tag{4.5}$$

If $C_{pz}R_{pz} = C_fR_f$, the zero introduced by the discharge resistor is eliminated and the transfer function for I_{PZ} reduces to a first order system whose impulse response cannot have undershoots.

$$I_{PZ} = \frac{-I_{det} R_f}{R + R_{pz}} \cdot \frac{1}{1 + sC_{pz} \dfrac{R_{pz} R}{R + R_{pz}}} \tag{4.6}$$

4th order real pole Shaper:

$$H(s) = \frac{Gain}{(1 + s\tau_{Shaper})^4} \tag{4.7}$$

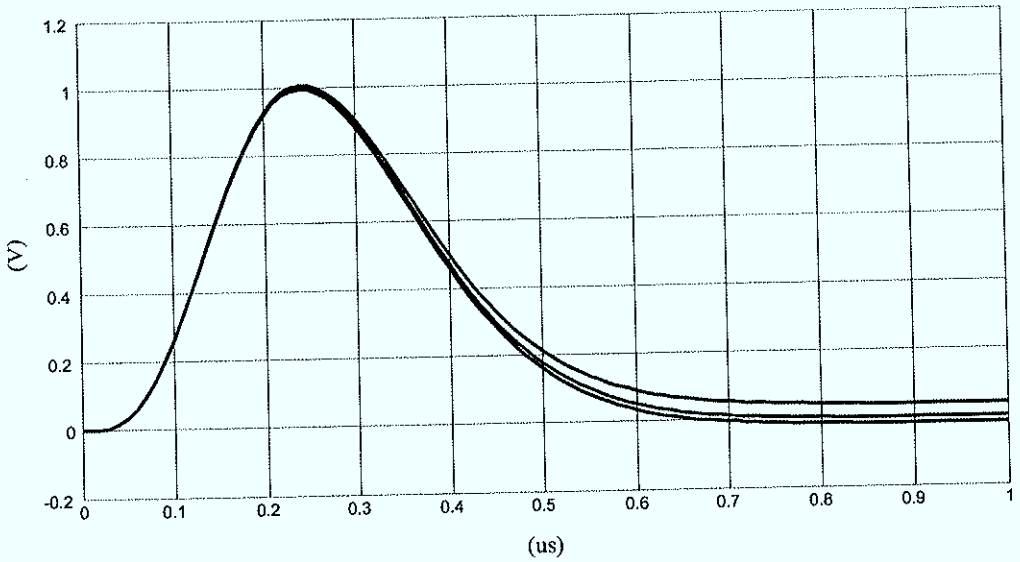


Figure 48 Imperfect pole zero cancellation

Circuit Implementation:

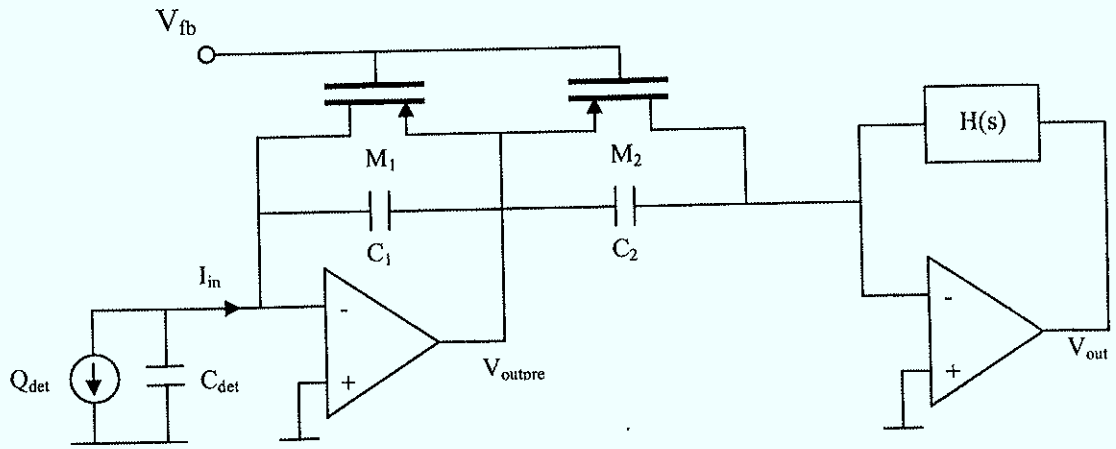


Figure 49 Non linear pole zero cancellation

Without detector leakage current or a current source at the input the feedback transistor operates in the linear region and its resistance is directly proportional to V_{GS1} and depends on V_{DS1}. The circuit implementation of Figure 49 forces $V_{GS1} = V_{GS2}$. Under the condition that preamplifier and shaping amplifier have the same DC operational point, V_{DS1} corresponds to V_{DS2} meaning if M_1 is identical to M_2 also the current through these devices is the same. In practical designs C_2 is chosen bigger than C_1 in order to reduce the noise contribution of the shaping amplifier. Therefore M_2 is realized using several parallel replicas of M_1 (depending on the ratio of C_1 and C_2) to guarantee in theory perfect pole zero cancellation under all operating conditions. In this way it is possible to cancel out the non linear pole that will no longer remain an inconvenience because at high counting rates V_{GS} will be bigger and the feedback capacitor will be discharged faster. The discharge

resistance should be independent of process variations. Therefore V_{FB} is generated by a circuit that uses a scaled replica of the preamplifier and M_1 to track process variations. [29]

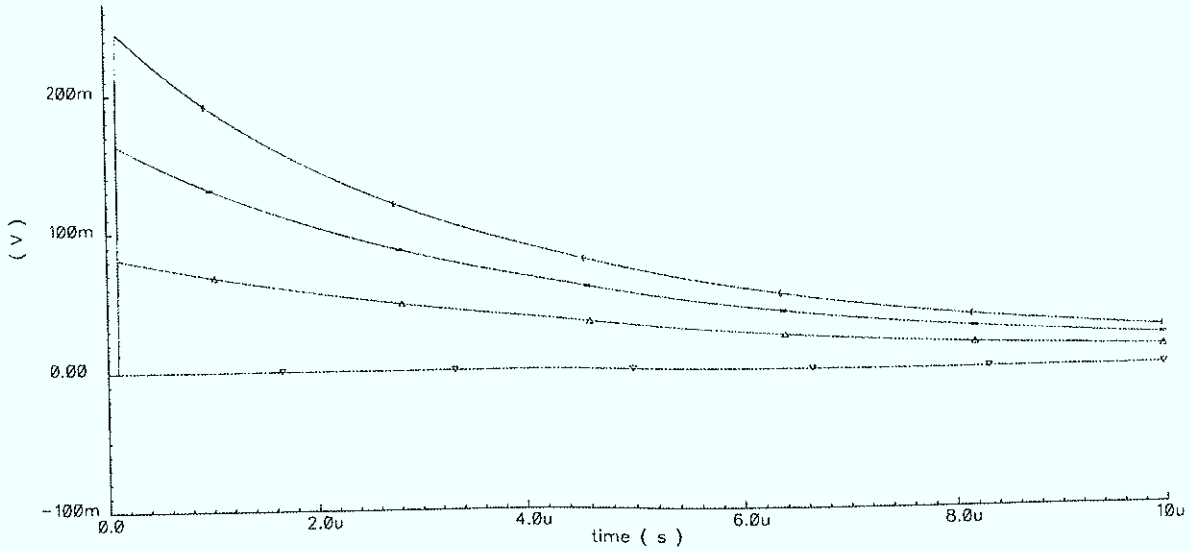


Figure 50 Discharge of the feedback capacitor for different charge pulses

Figure 50 shows V_{outpre} for different charge pulses from 0 to 200 fC and demonstrates the faster discharge for bigger signals.

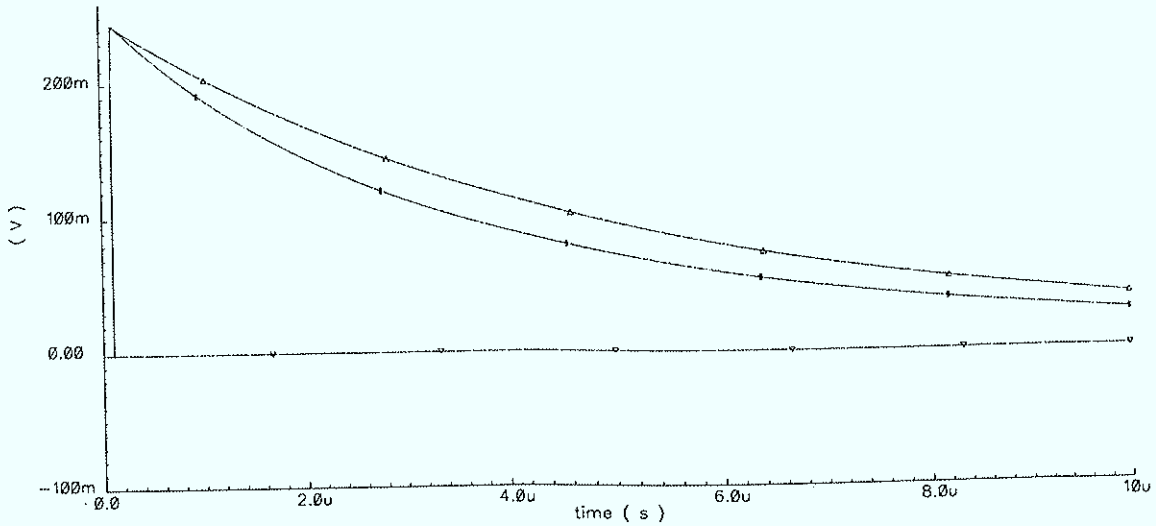


Figure 51 A 60 fC and a 200 fC charge pulse scaled to same amplitude

M_1 can be operated in the saturation region by forcing a current through it allowing different DC operating points at input and output of the preamplifier. The effective feedback resistance is determined by the resistance seen at the source of the feedback element.

$$R_{fbeff} = \frac{1}{g_{m1}} \tag{4.8}$$

Since M_1 is operated in the saturation region its g_m will be a function of the current. The current forced through M_1 contributes parallel noise. Therefore this approach is rather suitable for designs with short peaking time.

4.1.3 Complex Conjugated Poles

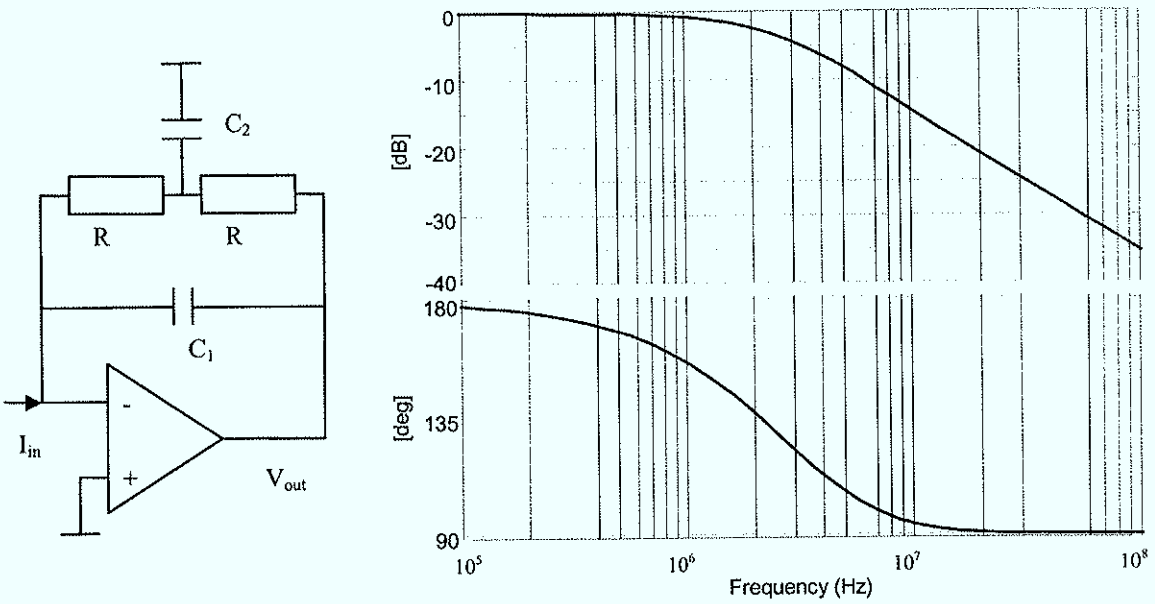


Figure 52 2nd order t-bridge low pass filter

$$V_{out}(s) = \frac{-I_{in}2R(1+sC_2R/2)}{1+s(2RC_1)+s^2(R^2C_1C_2)} \tag{4.9}$$

$$H(s) = \frac{K\omega_p^2(1+\frac{s}{\omega_z})}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2} = \frac{K(1+\frac{s}{\omega_z})}{\frac{s^2}{\omega_p^2}+\frac{s}{Q_p\omega_p}+1} \tag{4.10}$$

$$K = 2R \tag{4.11}$$

$$\omega_p = \frac{1}{\sqrt{R^2C_1C_2}} = \frac{1}{R\sqrt{C_1C_2}} \tag{4.12}$$

$$Q_p = \frac{1}{\omega_p 2RC_1} = \frac{1}{2}\sqrt{\frac{C_2}{C_1}} \tag{4.13}$$

$$\omega_z = \frac{2}{C_2R} \tag{4.14}$$

As equation (4.9) demonstrates, the t-bridge low pass filter has a zero in the transfer function that has to be considered when calculating the impulse response of the shaping amplifier. It is a 2nd order low pass filter but performs only 20 dB attenuation per decade above the corner frequency.

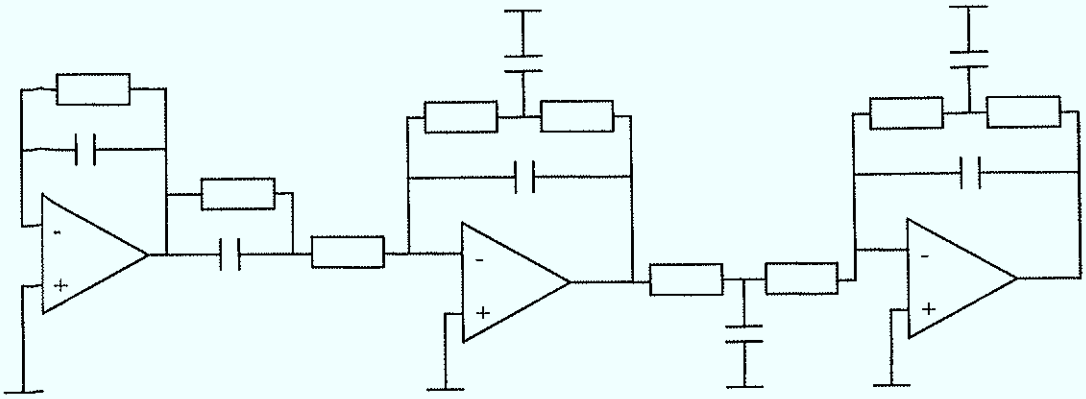


Figure 53 CSA followed by a CR-RC-$(RC_{Complex})^2$

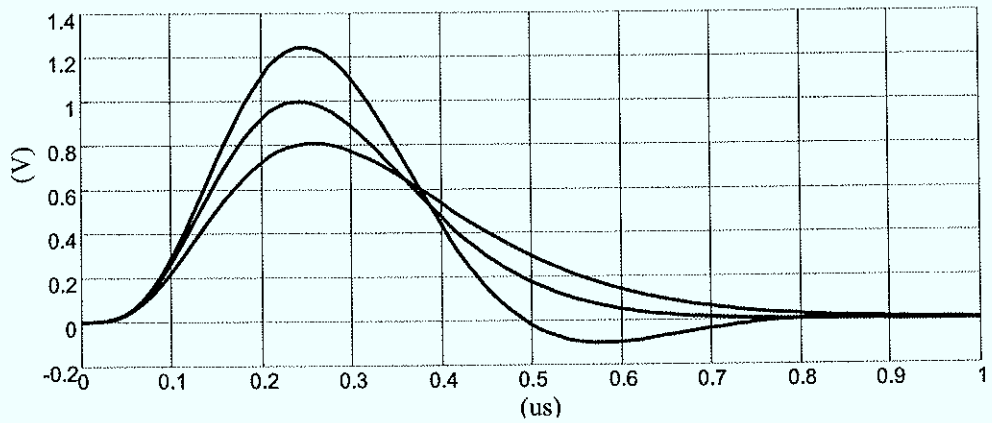


Figure 54 Impulse response for C_2 = 0.3, 1.3, 2.3 C_1

Figure 54 shows an increase in gain and a tendency for undershoot for larger C_2. This effect allows an approximation of higher order semi Gaussian pulses (faster return to the baseline) with lower order filter stages. In Figure 55 the black dashed impulse response (C_2/C_1 = 1.7) approximates a 4th order semi Gaussian pulse, magenta 3rd and 4th order pulses.

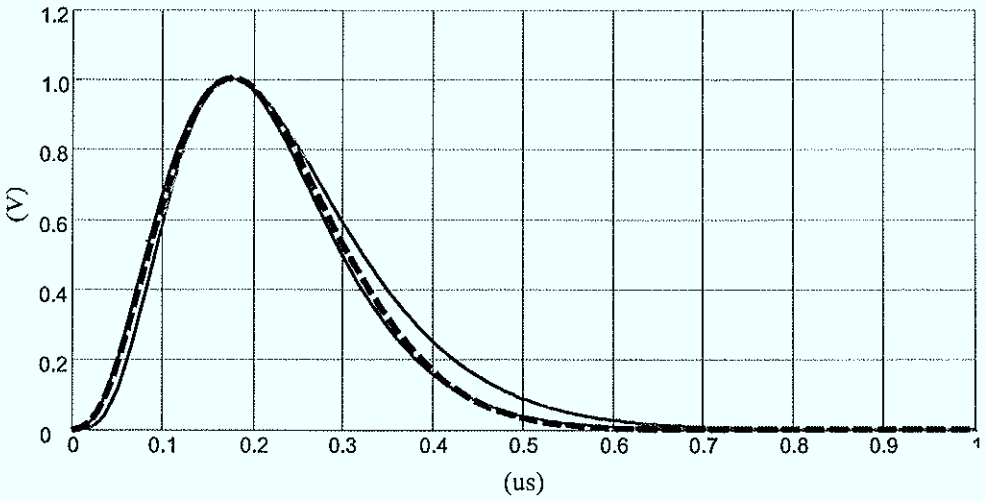


Figure 55 CR-RC-$(RC_{Complex})^2$ shaper approximates a 4th order semi Gaussian pulse

4.2 CMOS - Folded Cascode Amplifier

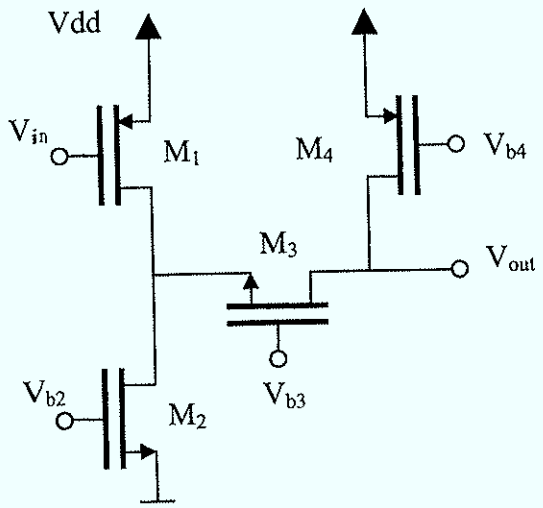


Figure 56 PMOS-NMOS folded cascode

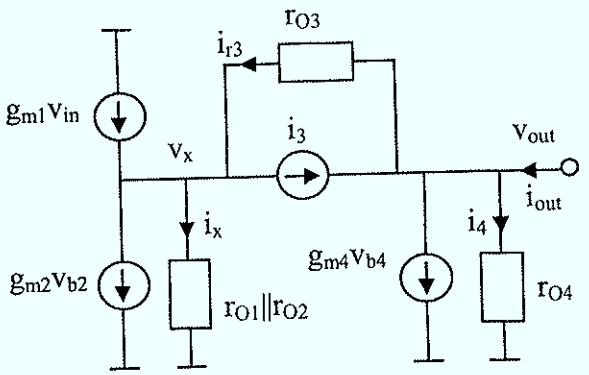


Figure 57 Small signal equivalent circuit

The idea behind the folded cascode structure is to convert the input voltage to a current and apply it to a common-gate stage (Figure 56). If V_{in} becomes more negative I_{DS1} will increase, forcing I_{DS3} to decrease and hence V_{out} to rise. A variation in I_{DS1} provokes V_{out} to change according to $\Delta I_{DS1} R_{out}$.

4.2.1 DC-Gain

Figure 57 depicts the small signal equivalent circuit from which the following equations were derived by using Mathematica.

Calculation of the output resistance:

By setting $r_{O4} = \infty$ the output resistance for the cascode branch is calculated:

$$v_x = i_x (r_{O1} \parallel r_{O2}) \tag{4.15}$$

$$v_x (g_{m3} + g_{mb3}) = i_3 \tag{4.16}$$

$$(v_{out} - v_x)/r_{O3} = i_{r3} = i_{out} + i_3 = i_x + i_3 \tag{4.17}$$

$$R_{outcas} = r_{O3} + [1 + r_{O3}(g_{m3} + g_{mb3})](r_{O1} \parallel r_{O2}) \tag{4.18}$$

R_{out} is given by the parallel combination of r_{O4} and R_{outcas}:

$$R_{out} = \{r_{O3} + [1 + r_{O3}(g_{m3} + g_{mb3})](r_{O1} \parallel r_{O2})\} \parallel r_{O4} \tag{4.19}$$

Under the assumption that any current change generated by the input transistor flows through the cascode branch the following equation holds true and A_{DC} can be derived by inspection:

$$A_{DC} \approx g_{m1} R_{out} \quad (4.20)$$

$$R = r_{O1} \parallel r_{O2} \quad (4.21)$$

$$A_{DC} = g_{m1} \cdot \{r_{O3} + [1 + r_{O3}(g_{m3} + g_{mb3})]R\} \parallel r_{O4} \quad (4.22)$$

But a part of the current change which is generated by the input transistor gets shunted by r_{O1} and r_{O2}. The expression for A_{DC} slightly changes to:

$$A_{DC} = g_{m1} r_{O4} R \frac{1 + (g_{m3} + g_{mb3}) r_{O3}}{R + r_{O3} + (g_{m3} + g_{mb3}) r_{O3} R + r_{O4}} \quad (4.23)$$

For $r_{O4} = \infty$:

$$A_{DC} = g_{m1} R[1 + (g_{m3} + g_{mb3}) r_{O3}] \quad (4.24)$$

The voltage gain from gate to drain of the input device is reduced by cascoding (suppression of the Miller effect):

$$\frac{vx}{vin} = -\frac{g_{m1} R(r_{O3} + r_{O4})}{R + r_{O3} + r_{O4} + (g_{m3} + g_{mb3}) R r_{O3}} \quad (4.25)$$

For $r_{O4} = r_{O3}$ and $Rg_{m3} >> 2$

$$\frac{vx}{vin} = -2\frac{g_{m1}}{g_{m3} + g_{mb3}} \quad (4.26)$$

For $i_{out} = 0$ the impedance seen at node X can be expressed as:

$$\frac{v_x}{i_{in}} = \frac{R(r_{O3} + r_{O4})}{R + r_{O3} + (g_{m3} + g_{mb3}) r_{O3} R + r_{O4}} \quad (4.27)$$

For $r_{O4} >>$, the impedance at node X is defined only by R meaning that the common gate stage cannot provide a low input impedance because the current through it is defined by an ideal current source.

$$\frac{v_x}{i_{in}} = R \quad (4.28)$$

But for $r_{O4} = 0$ and $R >>$, the resistance at X is given by the g_m of the cascode device:

$$\frac{v_x}{i_{in}} = \frac{1}{1 + \frac{1}{R} + (g_{m3} + g_{mb3})} \approx \frac{1}{g_{m3} + g_{mb3}} \quad (4.29)$$

For $r_{O4} = r_{O3} = R$:

$$\frac{v_x}{i_{in}} = \frac{2 r_{O4}}{3 + (g_{m3} + g_{mb3}) r_{O4}} \approx \frac{2}{g_{m3} + g_{mb3}} \quad (4.30)$$

4.2.2 Folded Cascode Frequency Response

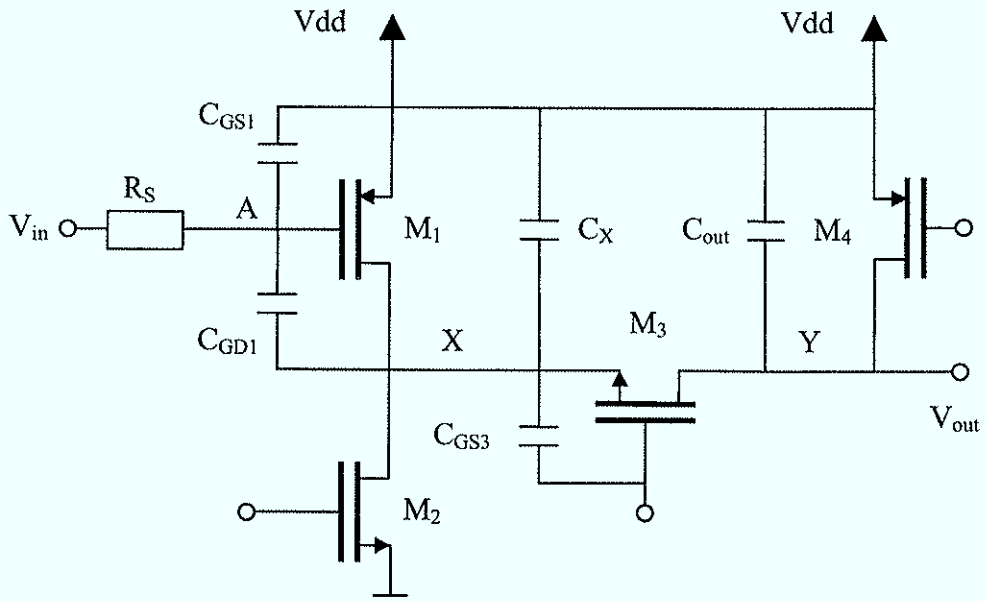


Figure 58 High frequency model of the folded cascode amplifier

C_{GD1} connecting node A and X appears at node A multiplied by the voltage gain between A and X. At high frequencies C_{out} shunts R_{out} establishing low impedance at the drain of M3 so that its source impedance can be approximated by $1/(g_{m3}+g_{mb3})$:

$$\omega_{p,A} = \frac{1}{R_S\left[C_{GS1} + (1+\frac{g_{m1}}{g_{m3}+g_{mb3}})C_{GD1}\right]} \quad (4.31)$$

$$\omega_{p,X} = \frac{g_{m3}+g_{mb3}}{\left[(1+\frac{g_{m1}}{g_{m3}+g_{mb3}})C_{GD1} + C_X + C_{GS3}\right]} \quad (4.32)$$

$$\omega_{p,Y} = \frac{1}{R_{out}C_{out}} \quad (4.33)$$

4.2.3 Noise Calculation

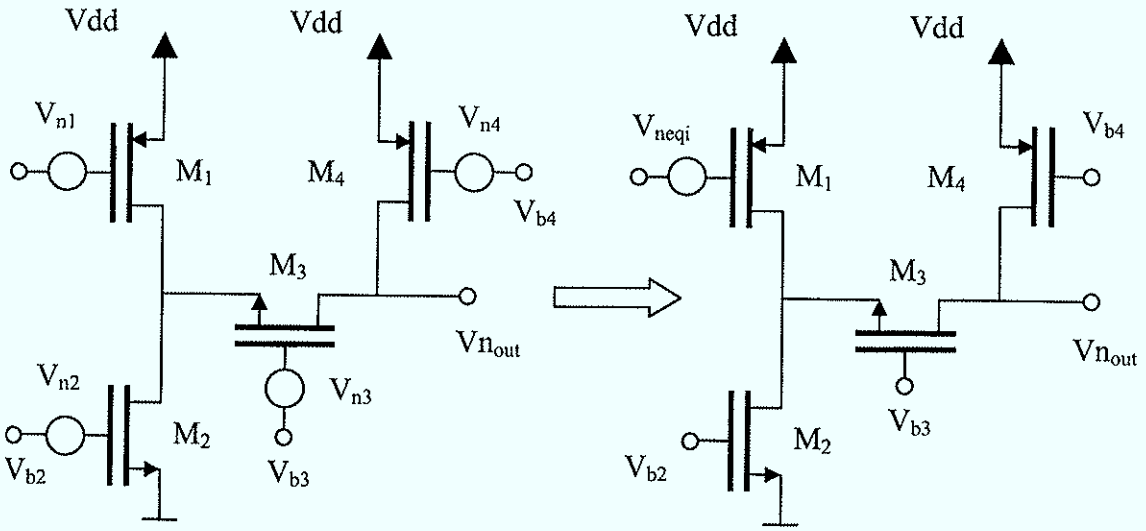


Figure 59 Input referred noise

$$R = r_{O1} \| r_{O2} \tag{4.34}$$

$$R_{out} = \frac{(R + r_{O3} + g_{m3} r_{O3} R) r_{O4}}{R + r_{O3} + g_{m3} r_{O3} R + r_{O4}} \tag{4.35}$$

$$\frac{v_{out}}{vx} = \frac{r_{O4}(1 + g_{m3} r_{O3})}{r_{O3} + r_{O4}} \tag{4.36}$$

Assuming uncorrelated noise sources:

$$Vn_{out}^2 = Vn_1^2 (\frac{V_{out}}{V_1})^2 + Vn_2^2 (\frac{V_{out}}{V_2})^2 + Vn_3^2 (\frac{V_{out}}{V_3})^2 + Vn_4^2 (\frac{V_{out}}{V_4})^2 \tag{4.37}$$

$$Vn_{ineqi}^2 = Vn_{out}^2 (\frac{V_1}{V_{out}})^2 = \frac{Vn_{out}^2}{(g_{m1} R_{out})^2} \tag{4.38}$$

Assuming that all transistors operate in saturation and strong inversion:

$$Vn_{ineqi}^2 = 4kT \frac{2}{3} \left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2} + \frac{g_{m4}}{g_{m1}^2} + \frac{1}{g_{m3}} (\frac{r_{O4}(1 + g_{m3} r_{O3})}{r_{O3} + r_{O4}})^2 \frac{1}{(g_{m1} R_{out})^2} \right) \tag{4.39}$$

In order to reduce the input-referred noise voltage the transconductance of the input device has to be maximized because signals at its gate have to be amplified and for transistors that serve as current sources the transconductance has to be minimized. The output noise of a properly designed low noise amplifier will be dominated by the input device. Including flicker noise and neglecting noise contributions from M_3 and M_4 the following expression can be obtained:

$$Vn_{ineqi}^2 = 4kT\frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g_{m1}^2}\right) + \frac{K_{fpmos}}{C_{ox}WLf} + \frac{K_{fnmos}}{C_{ox}WLf}\frac{g_{m2}^2}{g_{m1}^2} \tag{4.40}$$

4.2.4 Trade-Off Noise Performance vs. Output Swing

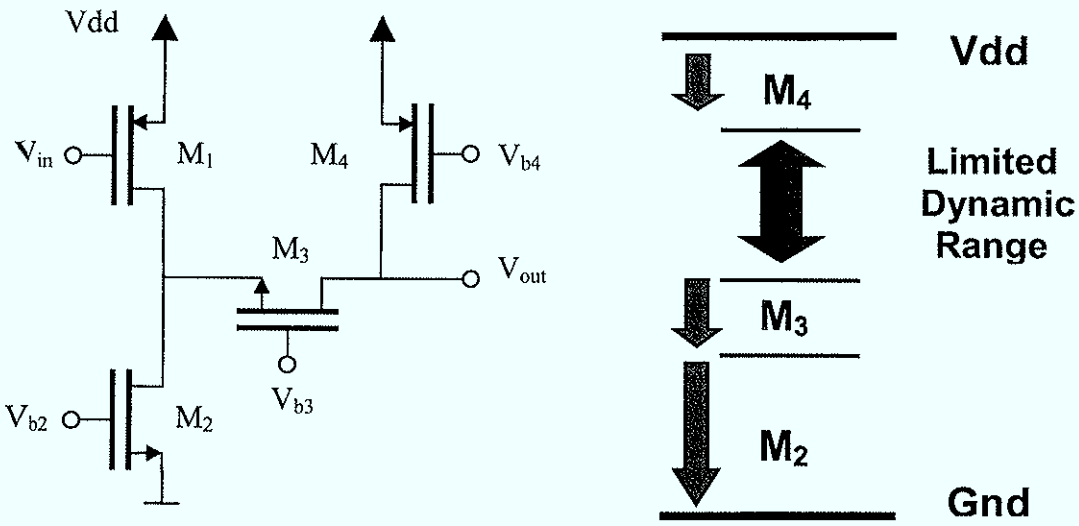


Figure 60 PMOS - NMOS cascode

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_{TH}} \tag{4.41}$$

For a given current the transconductance can be reduced by increasing the transistor's V_{GS}-V_{TH}. Higher V_{GS} affects the amplifier's maximum allowable output voltage swing because it will push the minimum V_{DS} where a transistor keeps operating in saturation region to higher values ($V_{DS} > V_{GS} - V_{TH}$). Minimizing the transconductance of M_2 while keeping the biasing current for the input device constant directly influences the allowable output voltage swing. Furthermore the current through the input device is decreased by the current necessary to bias the cascode branch.
The output dynamic range is limited to Vdd - $3V_{DSsat}$. This is of greatest significance particularly in low voltage low noise designs. The strong limitation in possible output swing will make the use of this amplifier topology prohibitive.

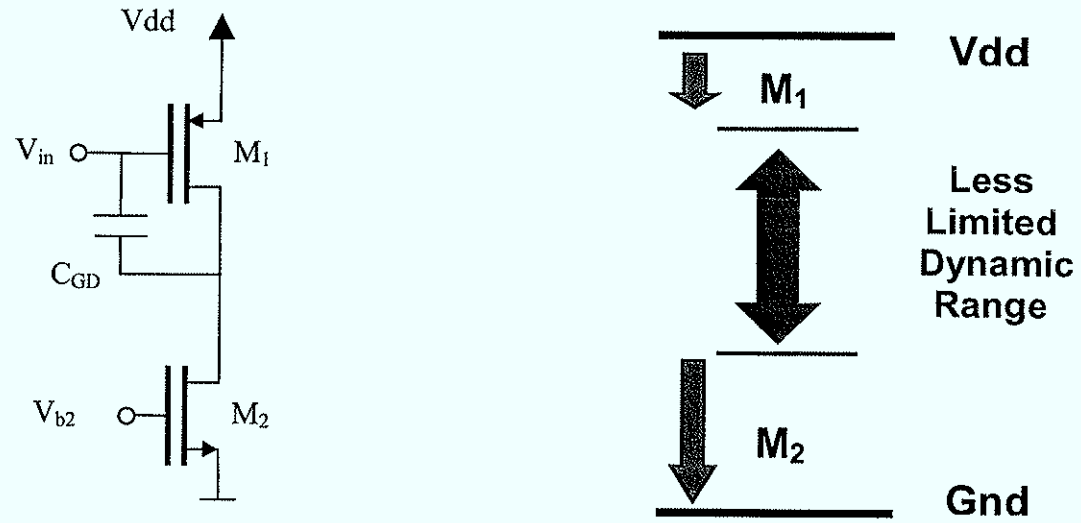


Figure 61 PMOS-NMOS common source

The removal of the cascode branch increases the possible dynamic range. However the advantages of the folded cascoded amplifier are lost. Cascoding suppresses the miller effect and increases the output resistance that is especially important for short channel devices that usually perform a much lower output resistance. Another possibility is given by the conventional non folded cascode amplifier but obviously this approach leads to a further decrease in possible output swing.

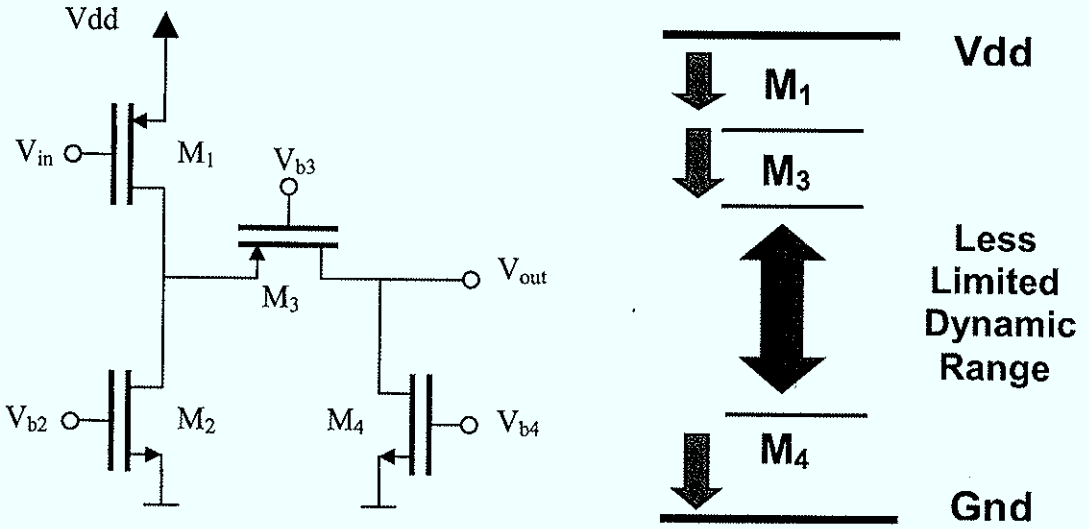


Figure 62 PMOS-PMOS cascode

Replacing the PMOS-NMOS cascode by a PMOS-PMOS cascode the noise contribution of the current source in the input branch can be minimized without degrading the output voltage swing. V_{b3} sets V_{DS} for M_1 that will be chosen small in order to reduce short channel effects like excess noise leaving Vdd - V_{DS1} as voltage room for M_2. This topology

is rarely used because the output DC level differs from the input DC level and makes it not easily possible to apply simple resistive feedback. Therefore a level shifter is necessary. The current through the cascode branch adds to the current through the input device what makes this topology more power efficient than the classical PMOS-NMOS cascode amplifier.

4.3 Rail to Rail Preamplifier

The classical single ended folded cascade amplifier is widely used in the field of low noise analog electronics for the readout of detectors. But especially at low supply voltages like 1.5 Volt in the 0.13 µm CMOS technology heavy restrictions in terms of allowable voltage swings arise. In order to be able to have more gain in the first stage that is essential for low noise designs a rail to rail preamplifier was developed to fully exploit the available voltage room. This additional voltage swing increases the circuit's pulse rate capability (see 5.1).

4.3.1 Moderate Gain Amplifier

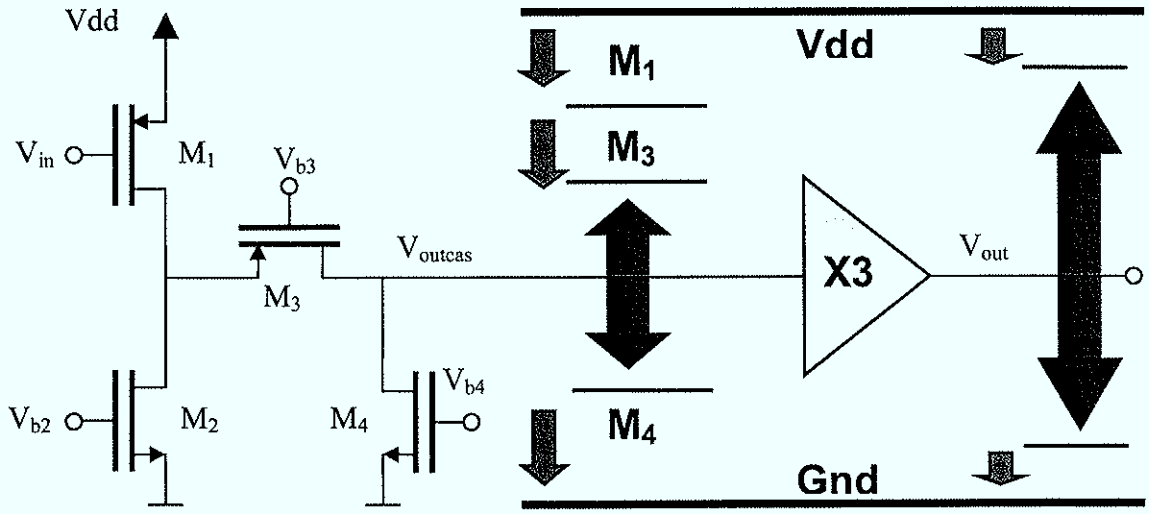


Figure 63 Moderate gain amplifier

A source follower after the cascode is often used to protect the high impedance point and to decrease the output impedance to be able to drive heavy loads. Replacing the source follower by a positive gain amplifier with rail to rail output introduces additional gain but also extends the possible output voltage range. Cascading of amplifier stages leads to multiple pole systems that are usually difficult to stabilize for high gain bandwidths. Therefore it was avoided to introduce unnecessarily much gain by choosing a moderate gain amplifier whose only function is to map the limited output range of the cascode to V_{out}. Figure 64 shows a possible circuit implementation where the moderate gain amplifier consists of two inverting amplifier stages. Resistive feedback is applied for the purpose of exactly defining the moderate gain. The input stage is designed for low noise and high gain without paying too much attention to swing-ability because the additional gain stage will limit voltage excursions around the operational point of V_{outcas} by its gain. The output stage

is optimized for output swing and speed. Although the amplifier of Figure 64 is built by the cascade 4 of amplifying stages (common source, common gate and two common source stages) the overall amplifier shows only one dominant pole at the high impedance point of the folded cascode.
In a low noise design it is absolutely necessary that most of the gain is concentrated in the input stage. Noise resulting from the following stages will be negligible because it is divided by the gain of the first stage when referred to the main input. But what applies to the intrinsic amplifier noise will certainly apply to noise generated by the power supply, as well. The conclusion is that the amplifier of Figure 64 exhibits negligibly more noise than the conventional folded cascode. Simulations verify the negligible noise contribution in the frequency range of interest.

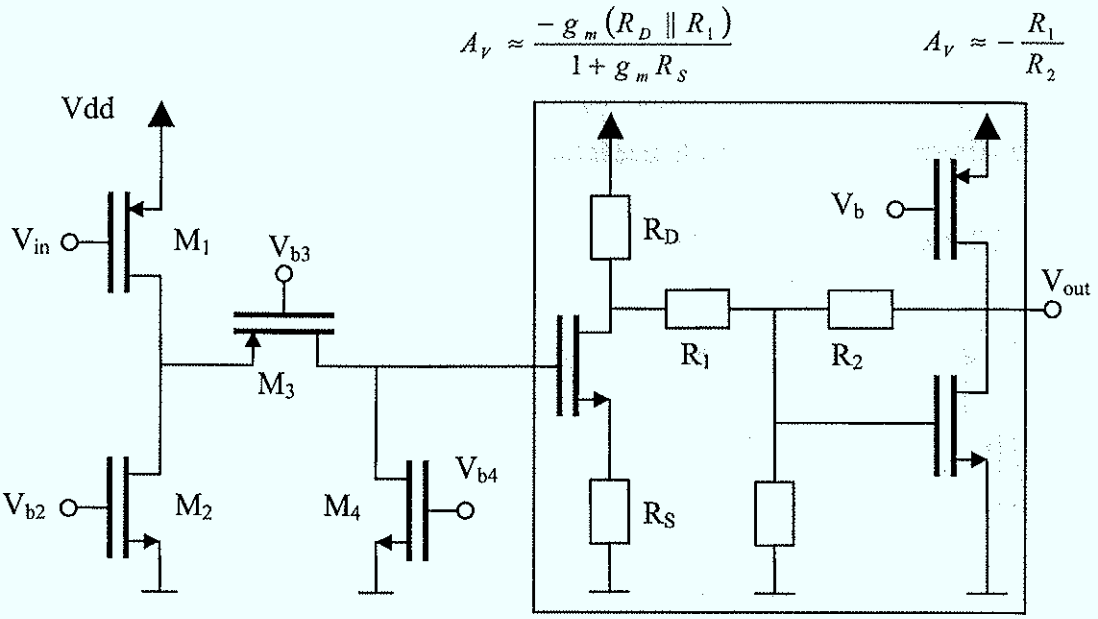


Figure 64 Circuit implementation of the moderate gain amplifier

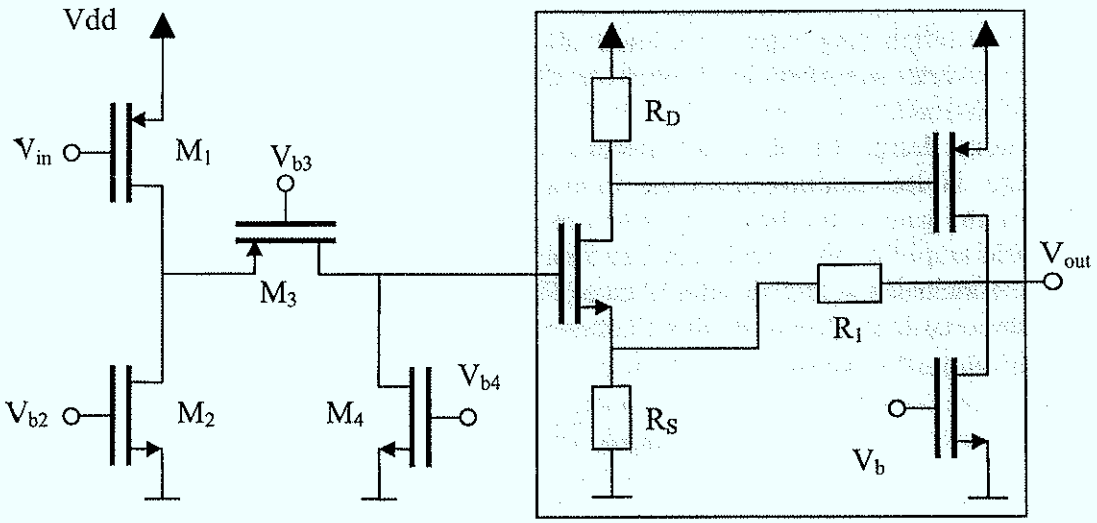


Figure 65 Alternative circuit implementation

4.3.2 Three Stage Amplifier

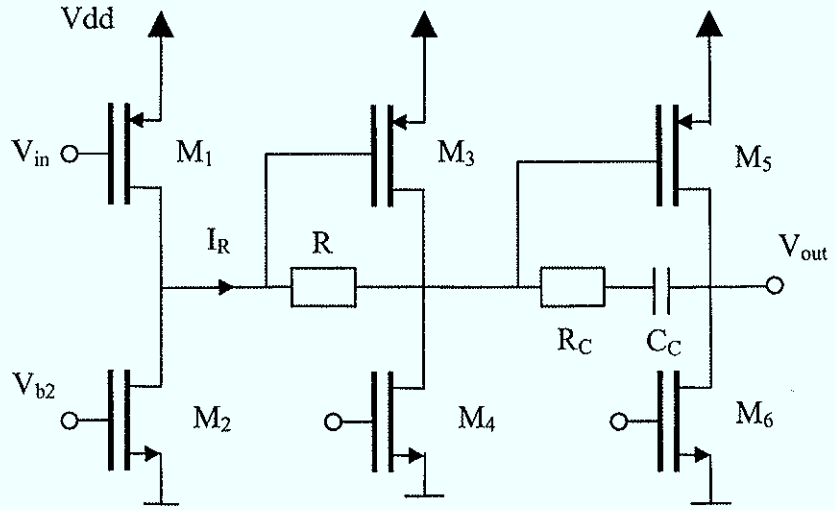


Figure 66 Three stage amplifier

Figure 66 depicts an inverting amplifier that is built of three common source stages in cascade. The transconductor establishes low impedance at the output of the input stage like the common source branch in folded cascode amplifiers. I_R gets transformed to a voltage and is applied to the output stage. The cascade of three inverting stages is an inverting amplifier.

Simulations show that the main noise sources are M_1, M_2 and M_3. Through maximization of g_{m3} the noise contribution of M_3 can be minimized to a negligible level. The architecture allows Vdd - V_{dsat1} as voltage room for M_2. Therefore V_{b2} can be chosen very high in order to minimize g_{m2}.

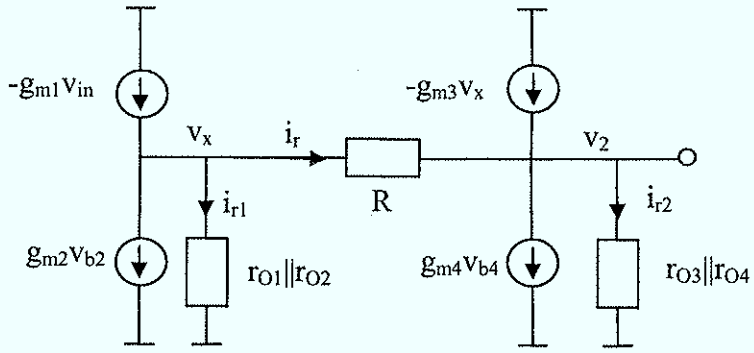


Figure 67 Small signal equivalent circuit of the first two stages

$$-g_{m1}v_{in} = \frac{v_x}{r_{O1} \parallel r_{O2}} + \frac{v_x - v_2}{R} = \frac{v_x}{R_1} + \frac{v_x - v_2}{R} \tag{4.42}$$

$$-g_{m3}v_x = \frac{v_2 - v_x}{R} + \frac{v_2}{r_{O3} \parallel r_{O4}} = \frac{v_2 - v_x}{R} + \frac{v_2}{R_2} \tag{4.43}$$

The DC gain is given by:

$$\frac{v_2}{v_{in}} = g_{m1}\frac{R_1 R_2}{R + R_1 + R_2 + g_{m3}R_1R_2}(g_{m3}R - 1) \tag{4.44}$$

Channel thermal noise calculation:

$$\frac{v_2}{v_x} = \frac{R_2}{R + R_2}(g_{m3}R - 1) \tag{4.45}$$

$$Vn^2_{ineqi} = 4kT\frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m2}}{g^2_{m1}} + \frac{1}{g_{m3}g_{m1}}\frac{R + R_1 + R_2 + g_{m3}R_1R_2}{R_1(R + R_2)}\right) \tag{4.46}$$

The general guide line of minimizing the g_m of current sources and maximizing the g_m of transistors that have to amplify a signal is still valid. But what is the noise contribution of the inserted feedback resistor of the second stage?

$$\frac{v_2}{i_r} = \frac{R_2}{1 + g_{m3}R_2}(g_{m3}R - 1) \tag{4.47}$$

$$Vn^2_{ineqi,R} = \frac{4kT}{R}\frac{1}{g_{m1}}\frac{R + R_1 + R_2 + g_{m3}R_1R_2}{R_1(1 + g_{m3}R_2)} \tag{4.48}$$

The noise contribution is negligible for sufficiently large values of R.

The amplifier in Figure 66 contains more poles than a single stage amplifier what makes it more difficult to stabilize. The phase margin can be improved by lowering the open loop gain or moving poles to higher frequencies. Multiple pole amplifiers have usually less

bandwidth because additional poles force the open loop gain to fall already at lower frequencies.
The resistor in the feedback of the second stage serves as gain control. The compensation capacitor enables pole splitting. At high frequencies C_C establishes a highly conductive path between output and gate of M_5. In that way the output pole moves to higher frequencies. Due to Miller multiplication C_C appears multiplied at the gate of M_5, the pole moves closer to the origin. C_C forms a parasitic feed forward signal path that manifests itself in a zero in the right half plane that introduces additional phase shift while preventing the open loop gain to fall. By means of R_C the position of the zero can be adjusted. The value of R_C has to be chosen carefully in order to assure that the zero is located at high frequencies. [12]

$$\omega_Z \approx \frac{1}{C_C\left(g_{m5}^{-1} - R_C\right)} \tag{4.49}$$

In reality it proves difficult to guarantee an accurate ratio of g_{m5} and R_C. Other circuit techniques exist that avoid the feed forward path.

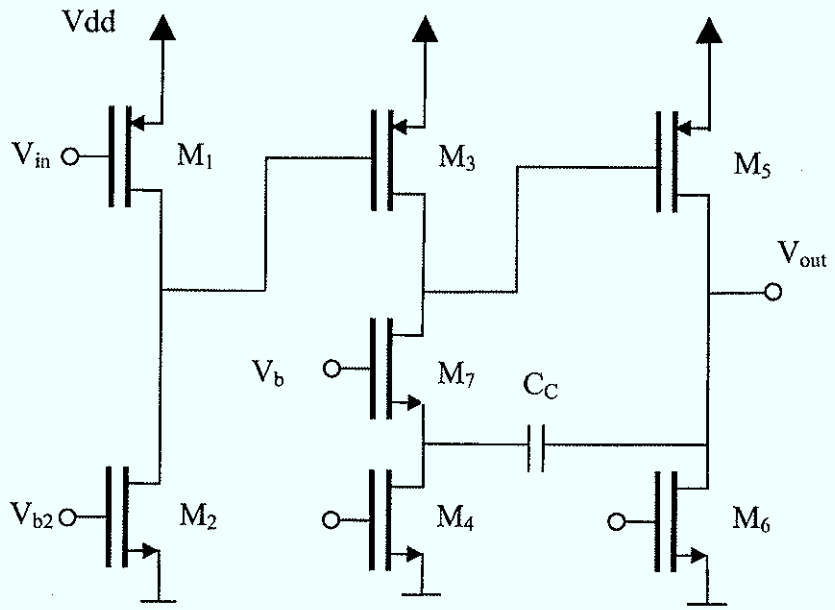


Figure 68 Eliminating the feed forward path [31]

The resistance seen at the source of M_7 is low ($1/g_{m7}$). The common gate stage performs current feed back.

4.3.3 Differential Preamplifier

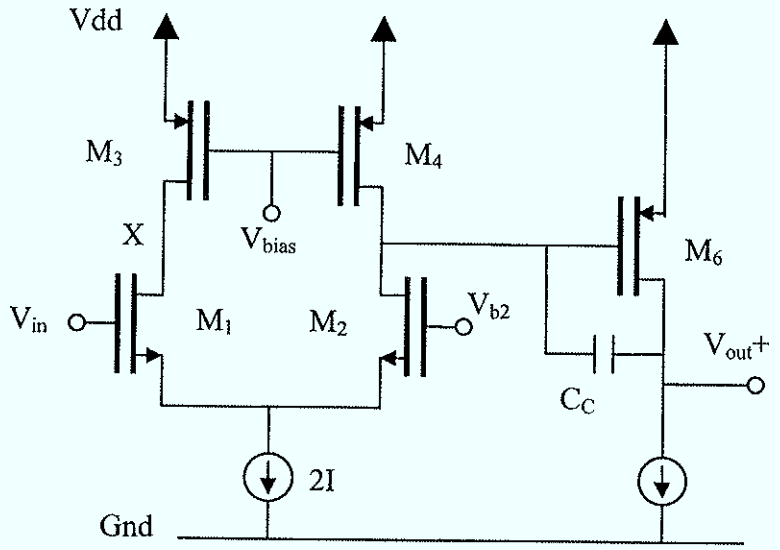


Figure 69 Differential preamplifier

Under the assumption that the noise contribution of M_6 is negligible and all transistors operate in saturation the following equation can be derived.

$$Vn_{ineqi}^2 = 2 \cdot 4kT \frac{2}{3}\left(\frac{1}{g_{m1}} + \frac{g_{m3}}{g_{m1}^2}\right) + \frac{2K_{fnmos}}{C_{ox}(WL)_1 f} + \frac{2K_{fpmos}}{C_{ox}(WL)_3 f}\frac{g_{m3}^2}{g_{m1}^2} \tag{4.50}$$

Since both input transistors carry AC current the squared equivalent input noise source is twice as large as it is the case for the single ended configuration, although twice the current is used. The increased PSRR of the differential configuration has to be paid by much larger power consumption when the same noise performance is desired. Furthermore the DC level of point X is poorly defined. The circuit of Figure 69 needs CMFB.

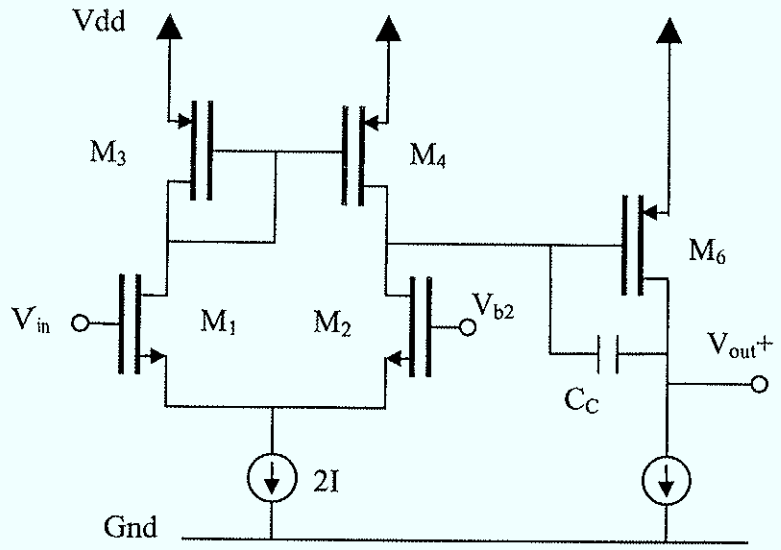


Figure 70 Differential two stage preamplifier with diode connected load

All DC levels can be derived by inspection. The current mirror distributes the current 2I equally among M_1, M_2, M_3 and M_4 which all carry AC current and thus contribute noise. It can be shown that best white thermal noise performance is achieved for equal contributions (g_{m1} equals g_{m3}). In this case the squared equivalent input noise source is four times as large as it is the case for the single ended configuration. Also the PSRR is poor because M_3 and M_4 see quite different loads. [30]

4.4 Matching the Detector Capacitance

Since parallel noise does not scale with the detector capacitance it will be neglected in the following discussion. A CMOS transistor, used as input-device, can be operated in three different operating regions (strong inversion, weak inversion and velocity saturation). It will be shown that depending on the operating region different approaches to match the detector capacitance apply.

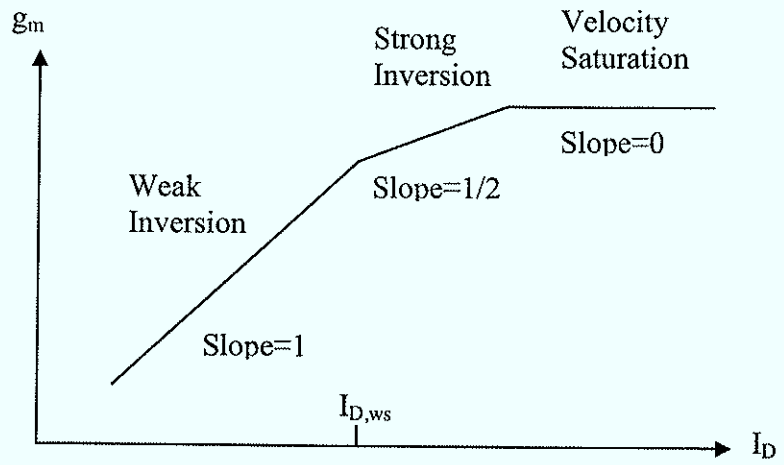


Figure 71 G_m as function of the drain current

The weak inversion region is the most efficient one in terms of g_m/I_D. Increasing the current increases g_m linearly until the device leaves the weak inversion region traverses the moderate inversion region and enters the strong inversion region where g_m increases only by the square root of I_D. Too large current pushes the operating point to velocity saturation and any further increase of I_D has no effect on g_m.

4.4.1 Strong Inversion

$$V_{N,channel}^2 = \frac{4kT}{g_m}\frac{2}{3} \tag{4.51}$$

$$C_G = WL \cdot C_{OX} \tag{4.52}$$

$$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = \frac{2I_D}{V_{GS}-V_{TH}} = \sqrt{2\mu_n \frac{I_D}{L^2}} \cdot \sqrt{WL \cdot C_{ox}} \tag{4.53}$$

$$V_{N,flicker}^2 = \frac{K_f}{C_{ox}WLf} \tag{4.54}$$

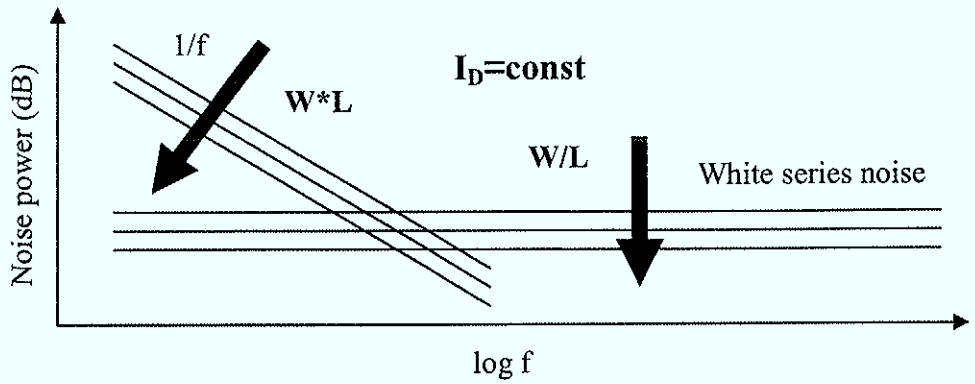


Figure 72 Serial noise sources

For a given drain current the equivalent noise sources of the input transistor show the behavior illustrated schematically in Figure 72. Increasing the gate area will reduce flicker noise whereas increasing the transconductance will decrease the thermal white noise. Larger gate area leads to larger parasitic capacitances at the CSA's input that add to the detector capacitance. For W = 0 the transconductance is zero and will increase by the square root of W but the added parasitic capacitance will influence the ENC linearly meaning that there must exist an optimum gate length that minimizes the ENC for a given detector capacitance.

$$ENC^2_{serieswhite} = (C_{det} + C_G)^2 \cdot a \cdot \frac{A_1}{T_M} = \frac{\alpha \cdot (C_{det} + C_G)^2}{gm} \tag{4.55}$$

$$\frac{d(ENC^2_{serieswhite})}{d(C_G)} = \frac{2\alpha \cdot (C_{det} + C_G) g_m - \alpha \cdot (C_{det} + C_G)^2 g_m'}{g_m^2} = 0 \tag{4.56}$$

$$2\sqrt{2\mu_n \frac{I_D}{L^2}} \cdot \sqrt{C_G} = \frac{(C_{det} + C_G)}{2\sqrt{C_G}} \sqrt{2\mu_n \frac{I_D}{L^2}} \tag{4.57}$$

$$C_{G,opt,StrongInversion} = \frac{C_{det}}{3} \tag{4.58}$$

$$ENC^2_{1/f} = (C_{det} + C_G)^2 \cdot \frac{A_2 \pi K_f}{C_{ox} WL} = (C_{det} + C_G)^2 \cdot \frac{A_2 \pi K_f}{C_G} \tag{4.59}$$

$$\frac{d(ENC^2_{1/f})}{d(C_G)} = A_2 \pi K_f \cdot \frac{2 \cdot (C_{det} + C_G) C_G - (C_{det} + C_G)^2}{C_G^2} = 0 \tag{4.60}$$

$$C_{G,opt,FlickerNoise} = C_{det} \tag{4.61}$$

The foregoing calculation [28] suggests an optimum C_G between C_{DET} and $C_{DET}/3$. Pulse shape, shaping time and available power influence the contribution of the series white noise to the total ENC. If series white noise dominates the ENC, C_G has to be chosen closer to $C_{DET}/3$ than in the case where flicker noise is dominant. Since $ENC_{1/f}$ is no function of the

shaping time it can only be further reduced by choosing an appropriate input device that has a lower K_f factor. 1/f noise sets the ultimate limit to the resolution of a CMOS charge detection circuit.

4.4.2 Weak Inversion

Due to CMOS scaling the weak inversion region is gaining more and more significance:

$$\frac{g_m}{I_D} = \frac{1}{nV_T} \tag{4.62}$$

Because of the bigger g_m/I_D the transconductance achieved for a given current in weak inversion (WI) is larger than in strong inversion (SI). The weak inversion region is preferred for high gain applications with less critical demands on speed because larger W has to be used in order to achieve the required low current density. The border between WI and SI is easily calculated by setting $(g_m/I_D)_{wi}$ equal to $(g_m/I_D)_{si}$:

$$\frac{g_m}{I_D} = \sqrt{2\mu_n C_{ox}\frac{W}{L \cdot I_D}} = \frac{1}{nV_T} \tag{4.63}$$

$$I_{D,sw} = \mu C_{OX}\frac{W}{L}2(nV_T)^2 \tag{4.64}$$

Shorter channel length and thinner gate oxide suggest that $I_{D,sw}$ will increase in scaled CMOS shifting the boarder towards velocity saturation and decreasing the SI region until it will vanish.
In WI operation g_m is not a function of W and hence not a function of the device dimensions. Reducing W will always improve the thermal noise contribution as long as the device stays in weak inversion leading to the fact that the optimal operation region is on the border between weak and strong inversion. [28]

$$C_{G,opt,WeakInversion} = 0 \tag{4.65}$$

4.4.3 Velocity Saturation

The carrier velocity $v = \mu E$ reaches a saturation value about 10^7 cm/s for sufficiently high fields. If the carrier velocity is constant over the whole channel the following equation for I_D can be derived:

$$I_D = v_{sat} \cdot Q_d = v_{sat} W C_{OX}(V_{GS} - V_{TH}) \tag{4.66}$$

$$g_m = C_{ox} \cdot W \cdot v_{sat} \tag{4.67}$$

v_{sat} Carrier saturation velocity

Q_d Inversion charge density (starting from $V_{GS} > V_{TH}$ an inversion layer is established and charge is mirrored via the gate capacitance to the inversion layer)

$$\frac{d(ENC^2_{serieswhite})}{d(C_G)} = \frac{2\alpha \cdot (C_{det} + C_G) g_m - \alpha \cdot (C_{det} + C_G)^2 g'_m}{g_m^2} = 0 \quad (4.68)$$

$$2 \cdot (C_{det} + C_G) \frac{C_G}{L} v_{sat} = (C_{det} + C_G)^2 \frac{v_{sat}}{L} \quad (4.69)$$

$$C_{G,opt,VelocitySaturation} = C_{det} \quad (4.70)$$

4.4.4 Optimal Operational Point for the Input Device

Starting from the optimal matching condition in strong inversion a general guideline for the optimum input device size can be derived that only depends on detector capacitance and available drain current: [28]

$$I_D = \frac{\mu C_{det}}{6L^2} (V_{GS} - V_{TH})^2 \quad (4.71)$$

$$(V_{GS} - V_{TH}) = \sqrt{\frac{6L^2 I_D}{\mu C_{det}}} \quad (4.72)$$

For strong inversion V_{GS}-V_{TH} has to be within certain boundaries:

$$\frac{v_{sat} L}{\mu} > (V_{GS} - V_{TH}) = \sqrt{\frac{6L^2 I_D}{\mu C_{det}}} > 2nV_T \quad (4.73)$$

$$\frac{6\mu}{v_{sat}^2} < \frac{C_{det}}{I_D} < \frac{3L^2}{2\mu (nV_T)^2} \quad (4.74)$$

The optimal operational point of the input device is dependent on technology parameters and the ratio between C_{det} and I_D. For a small ratio the point for optimum matching will shift to velocity saturation ($C_{G,opt} = C_{det}$). For larger ratios the point lies in the strong inversion region at $C_{G,opt} = C_{det}/3$. And for even larger ratios the optimum point lies at the border to weak inversion with the smallest possible C_G.

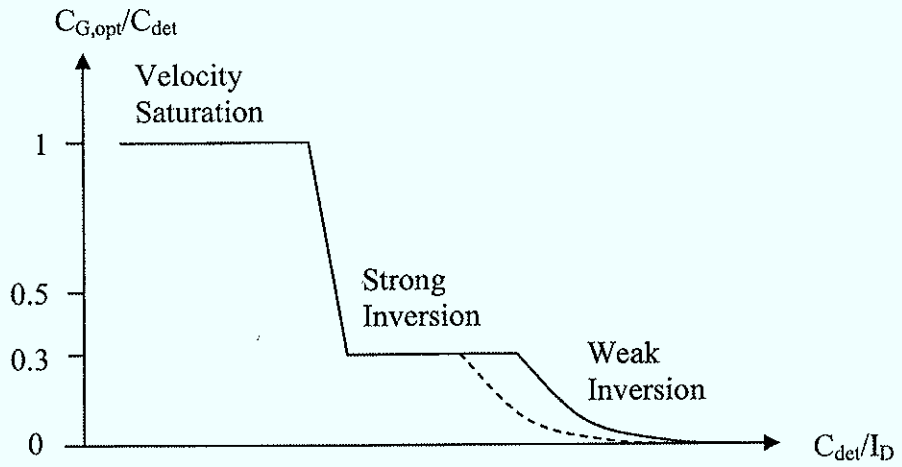


Figure 73 Optimal C_G

Figure 73 shows the optimal operational point for two different technologies (dashed-shorter minimum channel length) pointing out that the strong inversion region loses significance in scaled CMOS. The foregoing calculations are based on simple equations to enable hand calculations and give general guidelines for the design and the minimization of white series noise. Figure 73 does not take into account flicker noise that is minimized for $C_{G,opt} = C_{det}$. This implies that the optimum gate capacitance that minimizes the overall ENC is bigger than suggested for the case of strong and weak inversion. Careful simulations with modern simulation tools that use more complex models have to be carried out in order to achieve optimal noise performance.

4.4.5 Shaper Noise Contribution

Up to now it has always been assumed that the output noise is only produced by the preamplifier itself. A real system will also have noise contribution from the following shaping stages. Especially in the case where a big output dynamic range is demanded the output noise level has to be as low as possible. This will lead to a non negligible noise contribution of the shaping amplifier and therefore to an increase of the ENC predicted by the foregoing hand calculations.

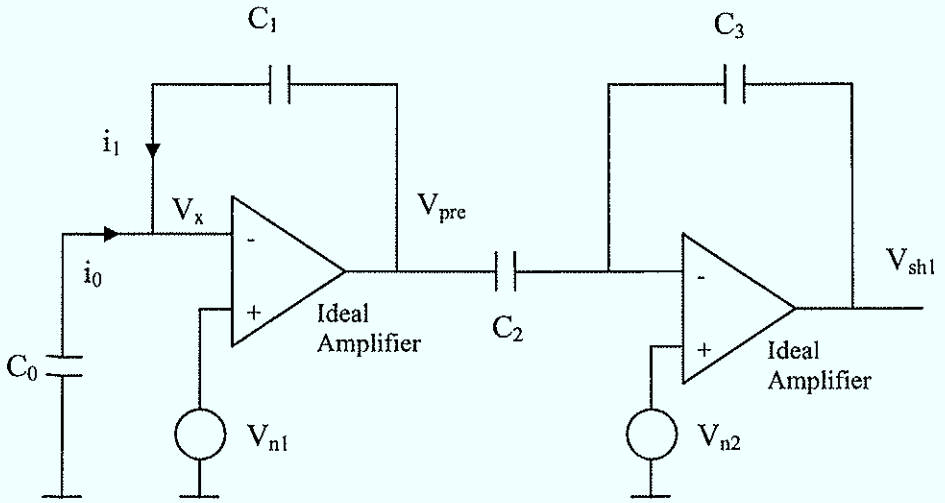


Figure 74 Shaper noise contribution – series noise sources

$$-i_0 = i_1 = V_x sC_0 = (V_{pre} - V_x)sC_1 \tag{4.75}$$

For an ideal amplifier V_x is equal to V_{n1}.

$$\frac{V_{pre}}{V_{n1}} = \frac{C_0}{C_1} + 1 = \frac{C_0 + C_1}{C_1} \tag{4.76}$$

$$V_{pre}^2 = \left(\frac{C_0 + C_1}{C_1}\right)^2 V_{n1}^2 \tag{4.77}$$

$$V_{sh1}^2 = \left(\frac{C_2}{C_3}\frac{C_0 + C_1}{C_1}\right)^2 V_{n1}^2 + \left(\frac{C_2 + C_3}{C_3}\right)^2 V_{n2}^2 \tag{4.78}$$

Dividing by the overall gain, the equivalent input noise source can be expressed as follows:

$$V_{in,eqi}^2 = V_{n1}^2 + \left(\frac{C_2 + C_3}{C_3}\frac{C_3}{C_2}\frac{C_1}{C_0 + C_1}\right)^2 V_{n2}^2 = V_{n1}^2 + \left[\left(1 + \frac{C_3}{C_2}\right)\frac{C_1}{C_0 + C_1}\right]^2 V_{n2}^2 \tag{4.79}$$

The relative contribution of V_{n2} to the output noise is low for large detector capacitances and for a small ratio between C_3 and C_2 that determines the gain from the first to the second stage outlining the trade off between optimum ENC and dynamic range.

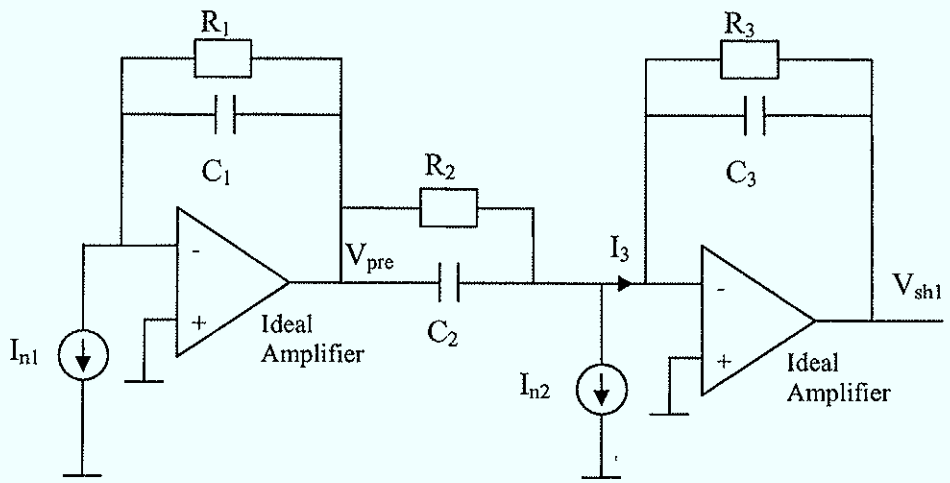


Figure 75 Shaper noise contribution – parallel noise sources

$$V_{sh1} = -I_3 Z_3 = -I_3 \left(\frac{1}{R_3} + sC_3 \right)^{-1} = -I_3 \frac{R_3}{1 + sC_3 R_3} \tag{4.80}$$

$$I_{n1}^2 = 4kT \frac{1}{R_1} \tag{4.81}$$

$$I_{n2}^2 = 4kT \frac{1}{R_2} + 4kT \frac{1}{R_3} \tag{4.82}$$

$$V_{n,sh1}^2 = \left(I_{n1}^2 \left(\frac{C_2}{C_1} \right)^2 + I_{n2}^2 \right) \cdot \left| \frac{R_3}{1 + sC_3 R_3} \right|^2 \tag{4.83}$$

$$\overline{V_{n,sh1}^2} = \int_0^\infty 4kT \left[\frac{1}{R_1} \left(\frac{C_2}{C_1} \right)^2 + \frac{1}{R_2} + \frac{1}{R_3} \right] \frac{R_3^2}{1 + 4\pi^2 C_3^2 R_3^2 f^2} df \tag{4.84}$$

$$\overline{V_{n,sh1}^2} = \int_0^\infty 4kT \left[\frac{1}{R_1} \left(\frac{C_2}{C_1} \right)^2 + \frac{1}{R_2} + \frac{1}{R_3} \right] \frac{1}{2\pi C_3 R_3} \frac{R_3^2}{1 + x^2} dx \tag{4.85}$$

$$\overline{V_{n,sh1}^2} = \frac{2kT}{\pi C_3} R_3 \left[\frac{1}{R_1} \left(\frac{C_2}{C_1} \right)^2 + \frac{1}{R_2} + \frac{1}{R_3} \right] \tan^{-1}(x) \Big|_{x=0}^{x=\infty} \tag{4.86}$$

$$\overline{V_{n,sh1}^2} = \frac{kT}{C_3} \left[\frac{R_3}{R_1} \left(\frac{C_2}{C_1} \right)^2 + \frac{R_3}{R_2} + 1 \right] \tag{4.87}$$

Considering only the shaping amplifier (neglecting R_1 and R_2), the minimum output noise is given by:

$$\overline{V_{n,sh1}^2} = \frac{kT}{C_3} \tag{4.88}$$

For R_1 = 1 MΩ, R_2 = 100 kΩ, C_2/C_1 = 10 and R_3 = 10 kΩ:

$$\overline{V_{n,shl}^2} = \frac{kT}{C_3}\left[\frac{10k}{1M}(10)^2 + \frac{10k}{100k} + 1\right] = \frac{kT}{C_3}[1 + 0.1 + 1] = 2.1 \cdot \frac{kT}{C_3} \tag{4.89}$$

I_3 is given by the input current multiplied by the ratio of C_2 and C_1. Since current noise is inverse proportional to the resistance, a sufficiently large R_3 will assure that the output noise is dominated by R_1.

The shaper output noise is dominated by the CSA noise for:

- Large C_2/C_1, current noise
- Large C_0/C_1, voltage noise
- Large C_2/C_3, voltage noise

4.5 PMOS or NMOS Input Device?

In weak inversion the transconductance is no longer dependent on device dimensions but on temperature and sub-threshold factor, see equation (4.62). PMOS and NMOS input devices operating in moderate inversion show comparable transconductance for the same current because the sub-threshold factors for the two different devices are nearly the same. In the technology used PMOS devices showed significantly less 1/f noise, meaning that a PMOS device that is much smaller performs the same 1/f noise like a NMOS device. A smaller device results in less input capacitance and degrades therefore not unnecessarily the series noise of the CSA, suggesting that considering only the facts mentioned above a PMOS device will exhibit a lower total ENC. Furthermore, PMOS devices are less affected by short channel excess noise.

4.5.1 Substrate Noise in Mixed Mode Circuits

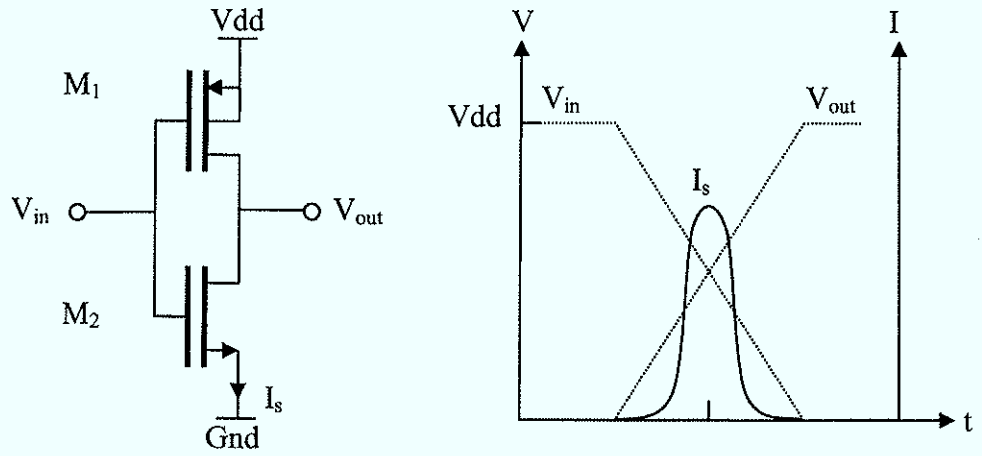


Figure 76 CMOS inverter, switching current

Ideally there is no static current flowing in CMOS logic. But during switching PMOS and NMOS transistors are both on for a short period of time establishing a conductive path from Vdd to Gnd. The resulting current is schematically sketched in Figure 76. [11]

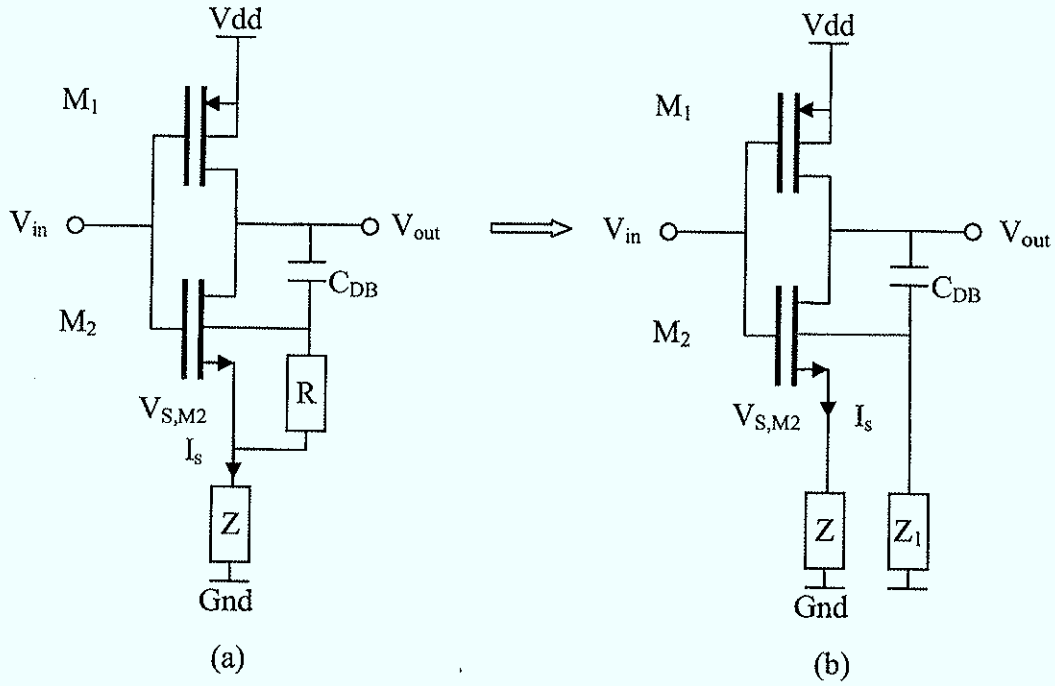


Figure 77 Separate substrate contact

In case (a) the substrate has a low ohmic connection to the source of M_2. In case (b) the substrate has its own connection to analog ground and perturbations generated at the source of M_2 are not directly injected to the substrate. This approach decreases perturbations from the digital section to the common substrate.

$$Z = R_{Wire} + sL_{Wire} \tag{4.90}$$

$$V_{S,M1} = I_s R_{Wire} + L_{Wire}\frac{dI_s}{dt} \tag{4.91}$$

As the foregoing calculation suggests, low bonding wire inductance and resistance will have a positive effect. Therefore the number of ground pins should be maximized.
Also capacitive coupling plays an important role. The output pin injects charge via C_{DB} to the substrate. The resulting perturbations of the substrate potential can be reduced by placement of more substrate contacts. This effect is also relevant for analog circuits where often large capacitors are used that have large parasitic capacitance to bulk. Limiting voltage swings, slower rise time, using capacitors with low parasitic capacitance, staggering of clock signals and output buffer timing, guard rings and substrate contacts help to minimize the impact on the substrate potential.
On chip decoupling before the wire bonds is very important to stabilize Vdd in case of fluctuations in current consumption. Unfortunately only small capacitors can be implemented on chip.

Types of Substrates:

An effective method for preventing latch-up is to reduce β of the parasitic bipolar transistors through layout techniques (guard rings and more distance). This approach suffers from the need for additional area that decreases the maximum number of gates that can be implemented for a given area. Nowadays there is a tendency towards low resistance substrates that have proven to be effective for the prevention of latch-up because lower resistances force currents causing latch-up to higher values.

Highly resistive substrate: [32]

High resistance of the substrate provides good isolation between distant points and creates a local substrate for wafers with non conductive backside.

Strategy to minimize interference from the digital circuitry:

- Remove channel stop implant to make substrate more resistive
- Guard rings - depletion region increases the length of the parasitic current path
- Distance
- Substrate contacts

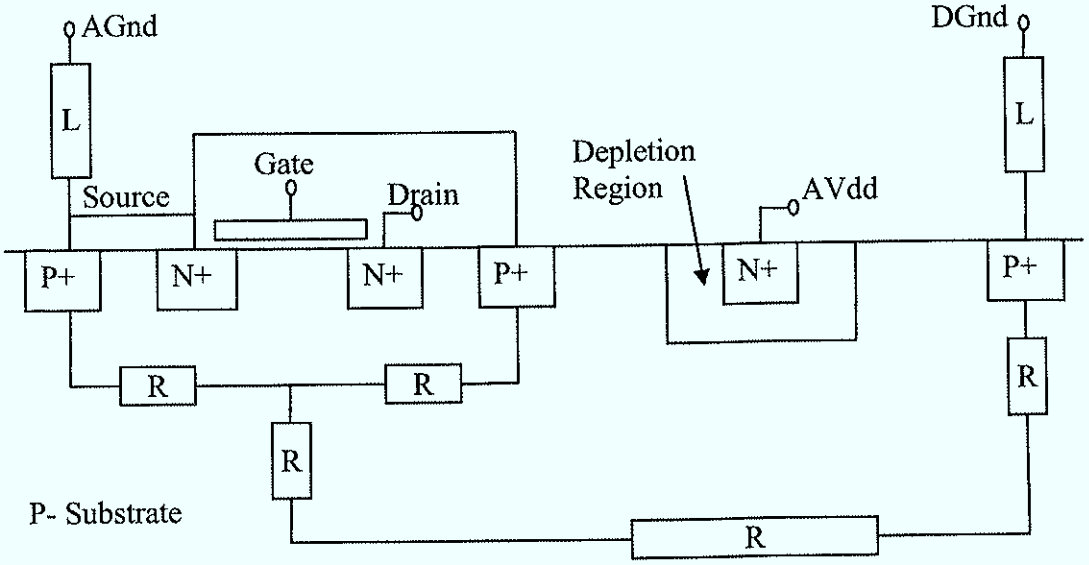


Figure 78 P- Substrate

Different supplies and guard rings are very effective to separate analog and digital circuitry on the same substrate.

Heavily doped substrate:

Because of the low resistance (~mΩ/cm) the bulk can be considered as a single node. The epitaxial layer has higher resistance (~Ω/cm).

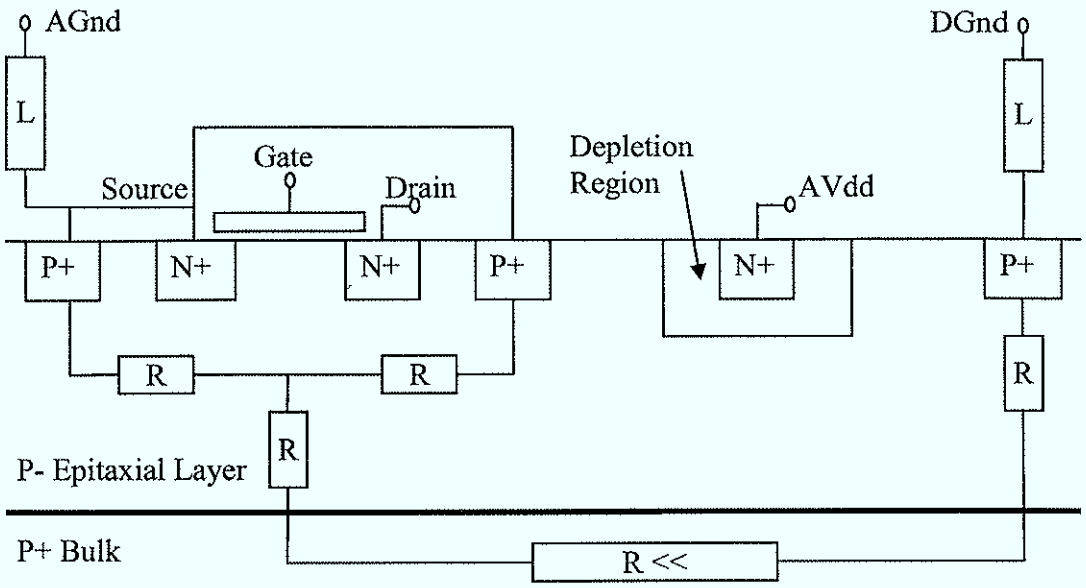


Figure 79 Heavily doped substrate

Strategy to minimize interference from the digital circuitry:

- Distance, guard rings and the removal of the channel stop implant do not prove very useful anymore
- Substrate contacts can make things worse (contact to quiet supplies only)
- Separate supply pins provide some benefit
- Minimize wire-bond inductance and resistance to ensure a low ohmic connection by maximizing the number of supply pins and choosing an appropriate package
- NMOS triple well transistor or PMOS will give some additional isolation. This approach proves very useful for low frequency applications. But at high frequencies substrate noise propagates over well capacitances to the sensitive area (do not use unnecessarily much bandwidth)
- Differential circuits and symmetrical layout for high PSRR and CMRR

The given 0.13 µm IBM process is a twin-well CMOS technology on nonepitaxial p- doped substrate. The p- doped substrate suggests that the process belongs to the group of high resistive substrates. But due to the very low substrate resistance it becomes similar to the heavily doped case.

PMOS – NMOS input:

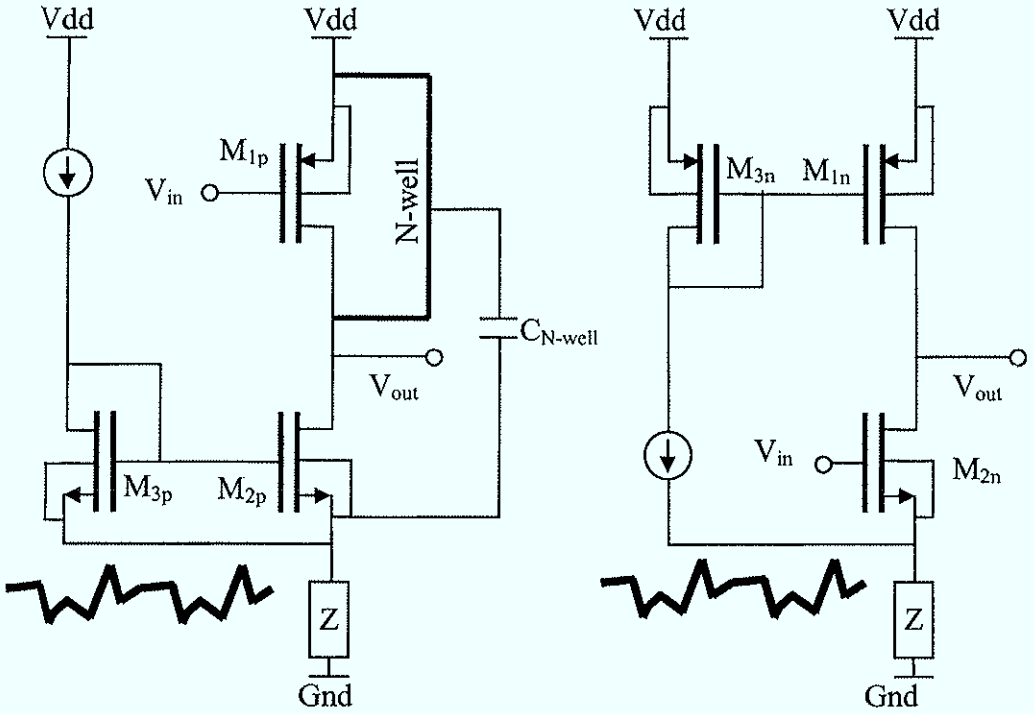


Figure 80 PMOS – NMOS input

In the case of the PMOS input device the N-well protects the most sensitive part of the circuit from substrate noise. Only capacitive coupling is possible and the N-well is tied to Vdd by low ohmic N-well contacts that will additionally attenuate disturbances originated from the capacitive coupling. Theoretically ground bounce does not influence the current mirror action because the low g_m devices M_{2p} and M_{3p} are equally affected. M_{2p} and M_{3p} should have similar layout (same L and same direction) and should be located close to each other (local bias network) in order to experience the same substrate noise and local process variations. Any imperfection will change the current and introduce in this manner a signal. This effect is attenuated by the low g_m of M_{2p} and M_{3p}. In a low noise design the input device performs the highest g_m. Since the current through M_{2n} is fixed by M_{1n} also $V_{GS,2n}$ is constant. Any voltage fluctuation seen at the source of M_{2n} will therefore directly introduce an artificial signal. If the gate potential changes also the voltage across C_{det} changes and the ground bounce gets additionally amplified by the ratio between C_{det} and C_f.

4.5.1.1 Detector Capacitance between Gate and Source of the Input Device

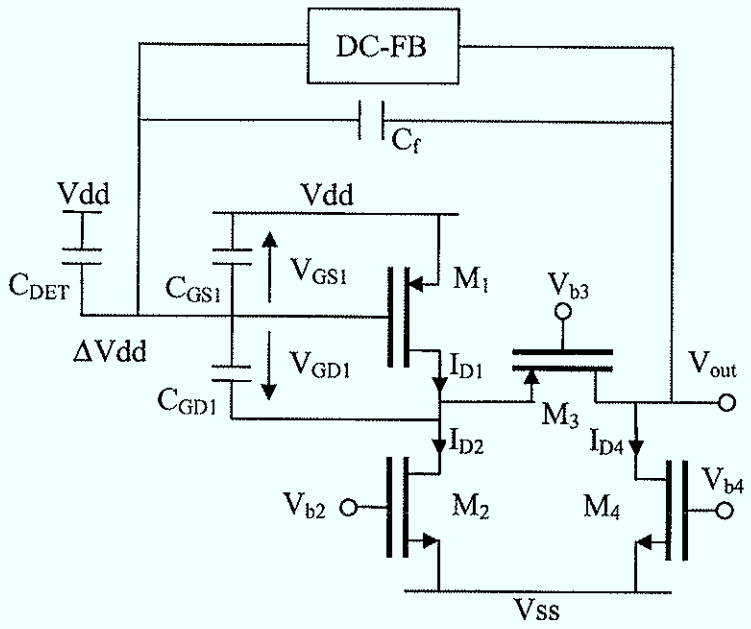


Figure 81 Detector capacitance between gate and source

PSRR+:
Assuming that Vdd changes by ΔVdd and Vss remains constant I_{D2} does not change (neglecting channel length modulation) because it is held constant by V_{GS} of M_2 that is not affected by ΔVdd. V_{GS} of M_1 remains also constant since the current through M_1 is fixed. ΔVdd translates directly to the input forcing V_{out} to change by ΔVdd. This means that any change of the positive power supply gets directly transferred to the output as long as the voltage across C_{GD1} stays also constant. Therefore V_{b3} should also change by ΔVdd because the drain potential of M_1 is fixed by $V_{b3}+|V_{GS3}|$.

PSRR-:
As long as the current of the two current sources is unaffected by a change in Vss I_{D1} does not change and V_{GS1} remains constant. Judging from the foregoing discussion it may be concluded that under ideal conditions ΔVss has no impact on V_{out}.

4.5.1.2 Detector Capacitance not between Gate and Source of the Input Device

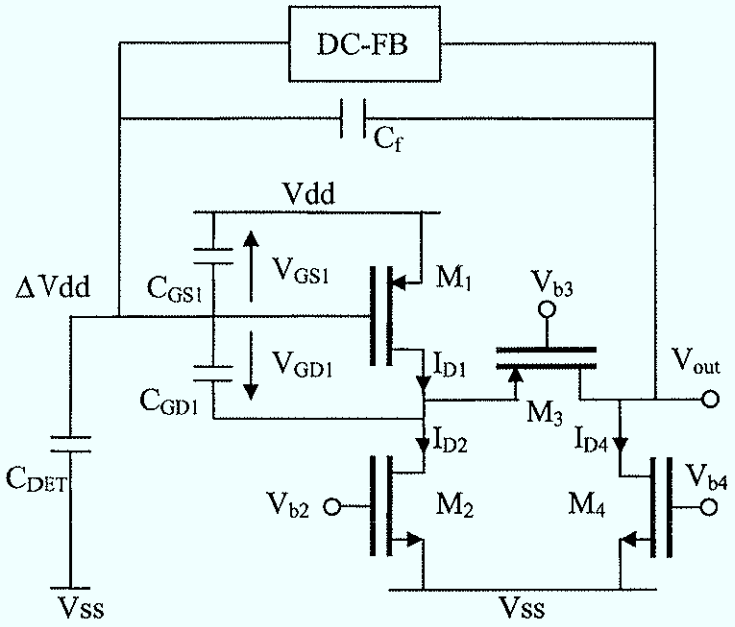


Figure 82 Detector capacitance not between gate and source

PSRR+:
Any change of the voltage across C_{DET} has a big impact on V_{out} because C_{DET} is the largest capacitance. Since I_{D1} is fixed any change in Vdd directly affects the voltage across C_{det}.

PSRR-:
For perfect biasing and neglecting channel length modulation the currents I_{D2} and I_{D4} do not change.

If C_{DET} is connected to Vss, noise from the power supply gets amplified by the ratio between C_{det} and C_f. Increasing C_{det} increases the noise originated from the power supply but also the intrinsic noise of the amplifier that scales with C_{det}.

For the former case where C_{DET} is between gate and source, better power supply rejection is obtained.

4.6 Prototype

The prototype circuit consists of a single ended charge sensitive amplifier that is followed by a fully differential 4th order shaping filter that produces a semi Gaussian pulse with predefined gain and peaking time. The circuit is designed in a 0.13 µm IBM technology. In order to reduce the complexity and gather some more experience with the new technology a non programmable architecture was chosen.

4.6.1 Chip Architecture

The available silicon area of the prototype run was 3 mm^2. Due to this limitation only 12 of the previously planned 16 channels were implemented. The prototype circuit is based on 5 different channel-architectures that differ in preamplifier architecture, peaking time and gain:

- 7 channels — PMOS folded cascode preamplifier, 100 ns shaping amplifier
- 1 channel — Thin oxide PMOS regulated folded cascode preamplifier, 100 ns shaping amplifier
- 2 channels — PMOS input rail to rail preamplifier, 100 ns shaping amplifier
- 1 channel — PMOS input rail to rail preamplifier, triple gain, 100 ns shaping amplifier
- 1 channel — PMOS folded cascode preamplifier, 50 ns shaping amplifier

40 dies were fabricated and the packaging was done by an external company.

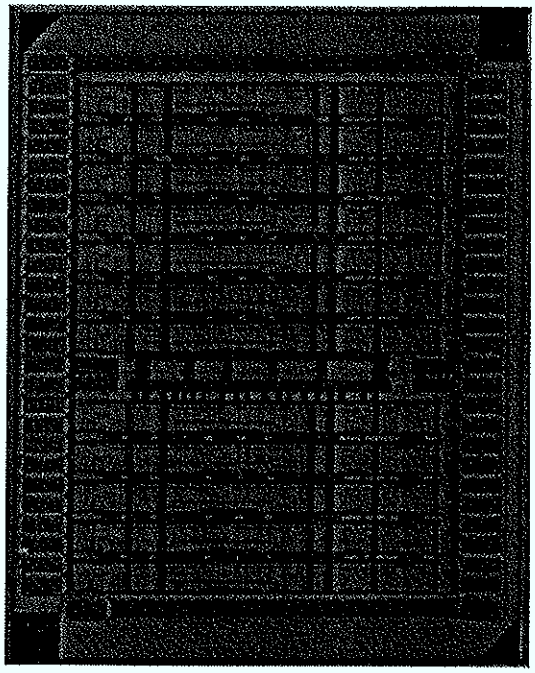


Figure 83 Silicon die photograph

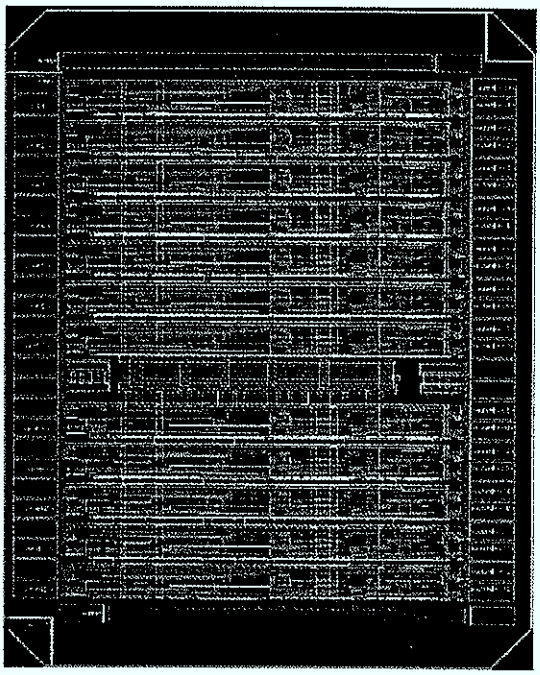


Figure 84 Chip layout

4.6.2 ESD Protection

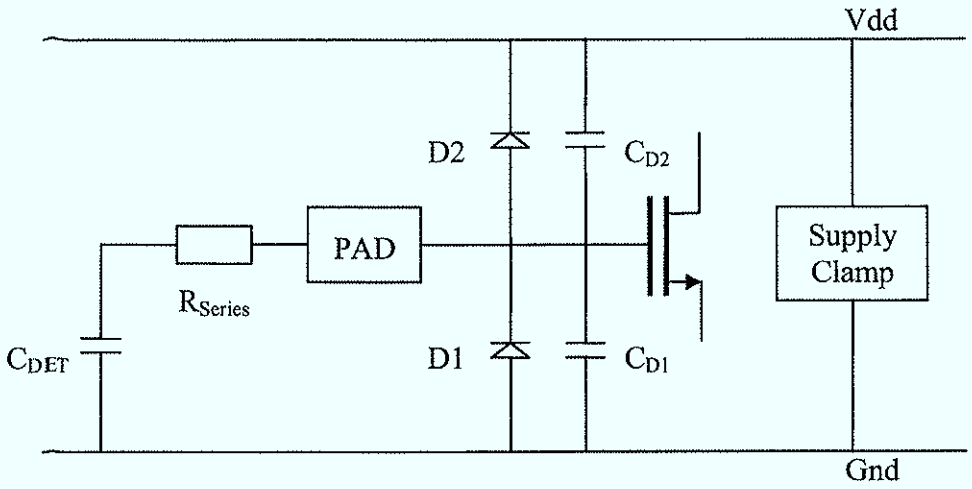


Figure 85 ESD protection

In order to protect the charge sensitive amplifier against sudden discharges of gaseous detectors and human handling additional circuitry has to be added. Reverse biased diodes clamp the potential of the sensitive input gate close to the supplies. In case of ESD the input potential can exceed the supply voltages and the protection diodes become conductive. During that process they usually have to absorb high currents that can even damage the ESD protection itself. Normally series resistance in the order of kΩ is used to limit current peaks. Unfortunately this is absolutely not compatible with high resolution detector electronics. ESD protection diodes have to be large enough to be able to absorb the maximum occurring energies. Therefore sufficient silicon area has to be used that incorporates also parasitic capacitance. The diodes used add approximately one pF input capacitance.

$$ENC^2 = (C_{\det} + C_{in} + C_{paraistic})^2 \left(\frac{A_1 2kT}{t_M} R_s + \frac{A_2 \pi K_f}{C_{ox} WL}\right) + \frac{A_3 2kT t_M}{R_f} \qquad (4.92)$$

The noise increase due to series resistance can be estimated by:

$$R_s = \frac{1}{g_m}\frac{2}{3} + R_{Sereis} \qquad \text{(Strong inversion)} \qquad (4.93)$$

A transconductance of 30 mS yields an equivalent noise resistance of 22 Ω. Only some Ω of series resistance would considerably contribute to the overall noise. Located in the substrate (heat sink) diffused resistors seem to be more appropriate as series resistor. In case of ESD the parasitic diode to substrate can become conductive and the circuit could be damaged due to thermal failure. Therefore no on- chip series resistance was realized.
Dielectric breakdown of the gate oxide takes place at roughly 10^7 V/cm [12], pointing out that thin oxide devices are more susceptible to field induced failures.

Beside series resistance and increase of input capacitance, the diode reverse current constitutes an additional noise source.

4.6.3 Channel Layout

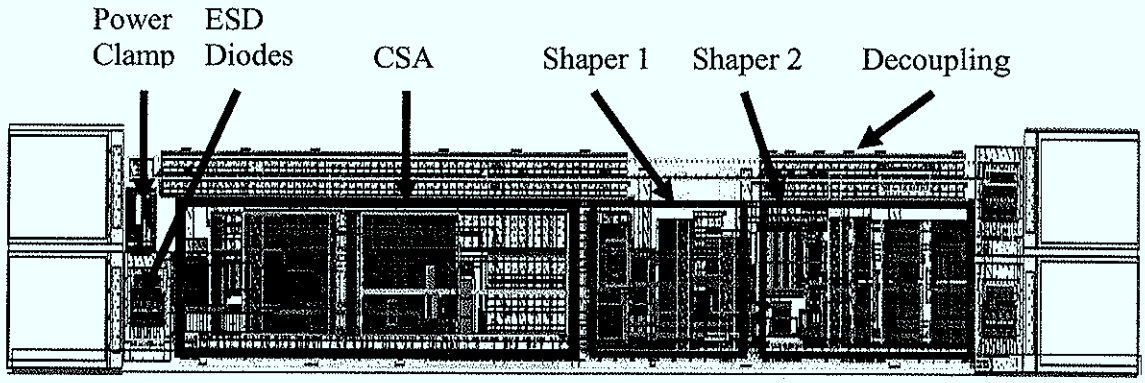


Figure 86 Single channel layout

4.7 Test Board

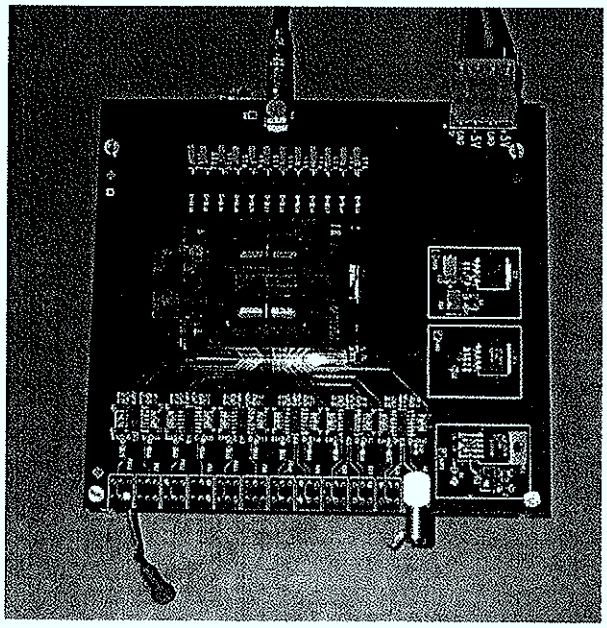


Figure 87 Test board photograph

Test Board Architecture:

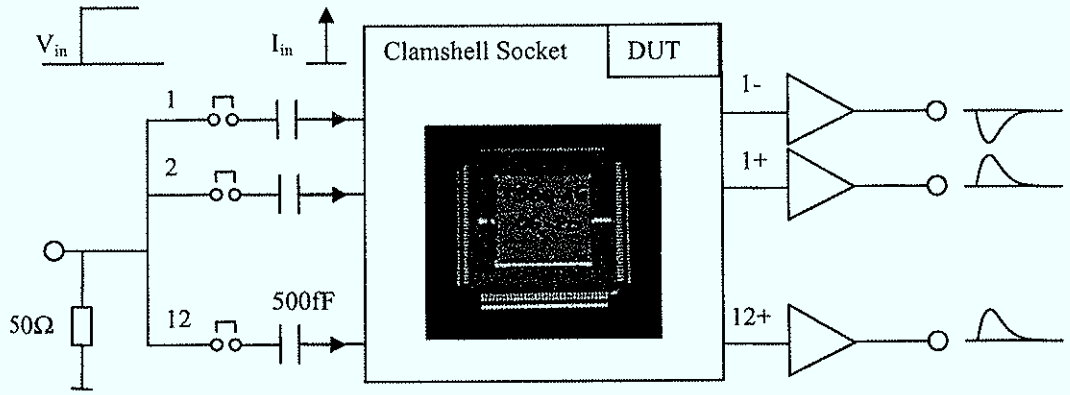


Figure 88 Test board architecture

Charge pulses are injected via small 500 fF capacitors that provoke impulse responses. A series of jumpers allows channel selection. In order to drive 50 Ω loads the prototype outputs are buffered by low noise unity gain amplifiers (Texas Instruments - OPA 4820). Due to the high on chip driving capability (30 pF) the output can be probed by means of an oscilloscope. The Tektronix TDS 540 was used to determine conversion gain and noise floor for the characterization of the amplifier. On the backside capacitors are soldered whether to Gnd or Vdd in order to emulate the detector.

4.8 Measurement Results

4.8.1 Conversion Gain

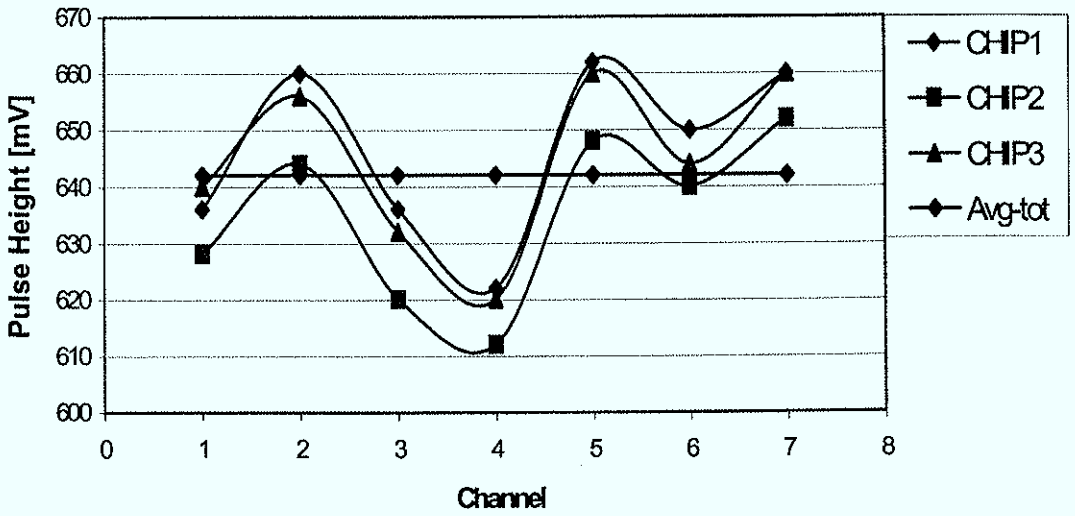


Figure 89 Standard channel – Gain (@ 10 pF)

Due to imperfections of the test board and variations of the small injection capacitor the injected charge is not exactly known. This systematic error was found to be larger than gain variations of the three measured chips. Assuming 500 fF capacitors, the injected charge is 74 fC. The average conversion gain is calculated to be 8.67 mV/fC.

4.8.2 Linearity

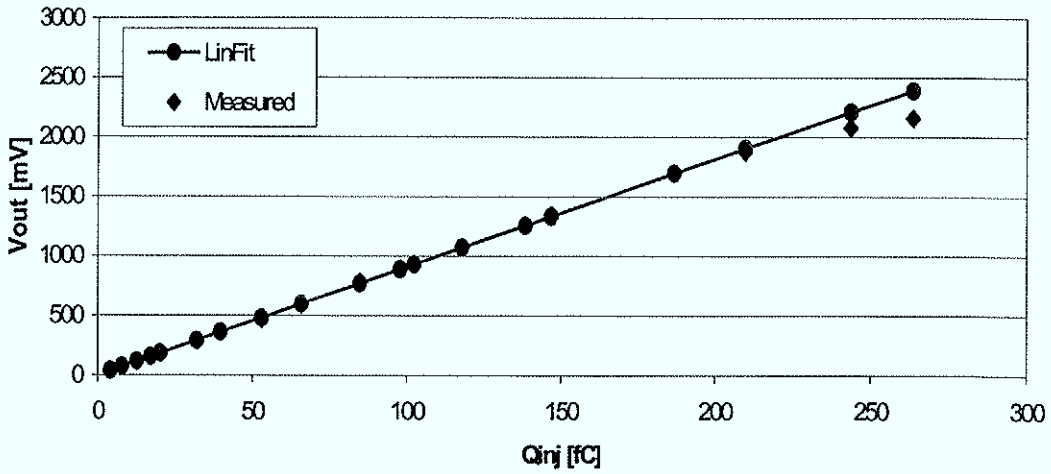


Figure 90 Linearity of standard channel (@10 pF)

The measured linearity is < 0.5 % up to 200 fC @ 10pF.

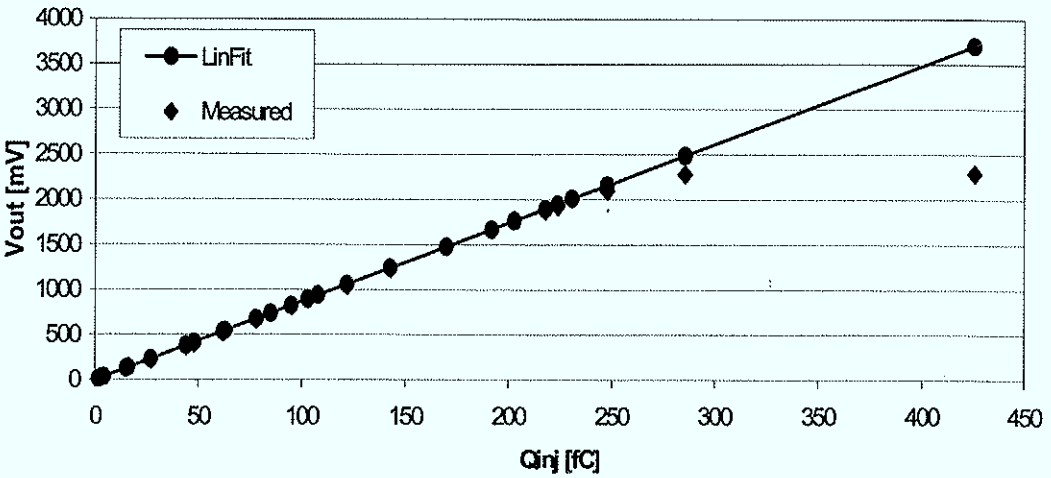


Figure 91 Linearity of rail to rail amplifier (@ 10 pF)

The measured linearity is < 1 % up to 200 fC @ 10pF. The standard channel shows better linearity.

4.8.3 ENC

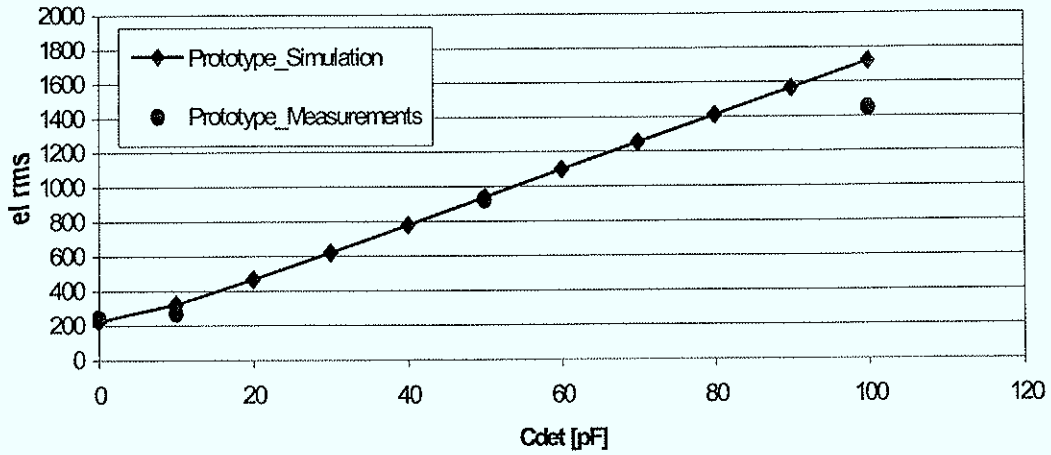


Figure 92 ENC vs. C_{det} – standard channel, 100 ns peaking time

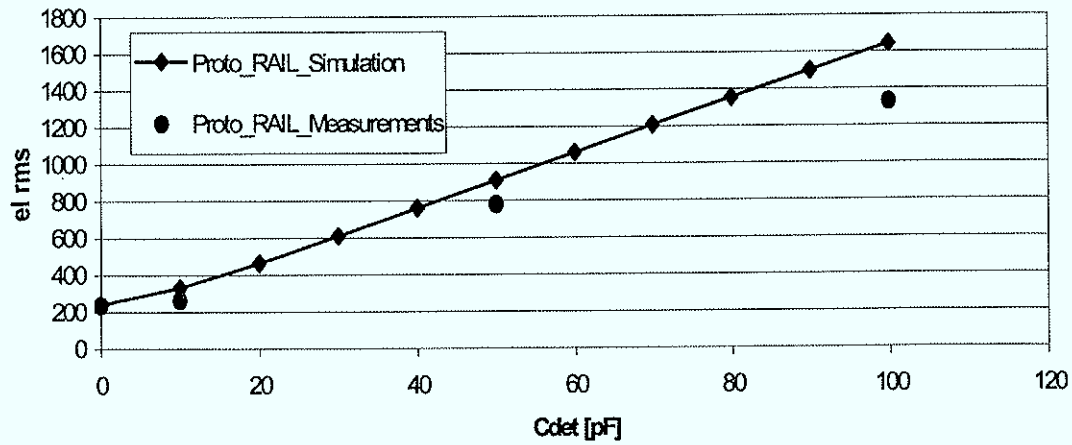


Figure 93 ENC vs. C_{det} – rail to rail preamplifier, 100 ns peaking time

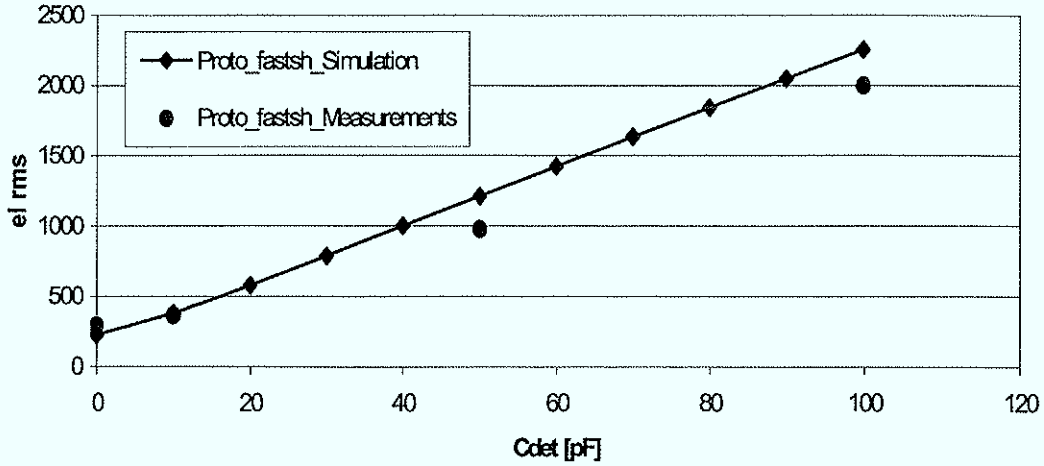


Figure 94 ENC vs. C_{det} – standard amplifier, 50 ns peaking time

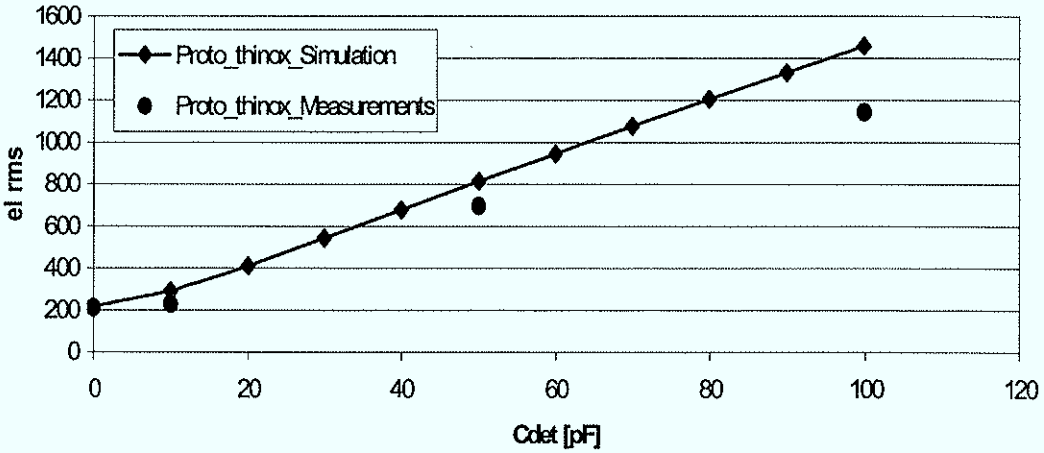


Figure 95 ENC vs. C_{det} – thin oxide input, 100 ns peaking time

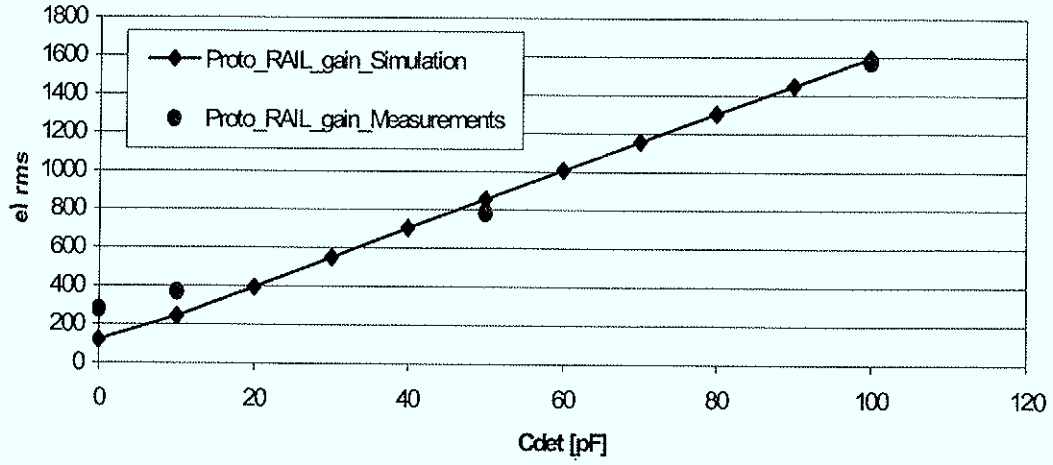


Figure 96 ENC vs. C_{det} – rail to rail preamplifier, triple gain in first stage, 100 ns peaking time

4.8.4 Pulse Shape

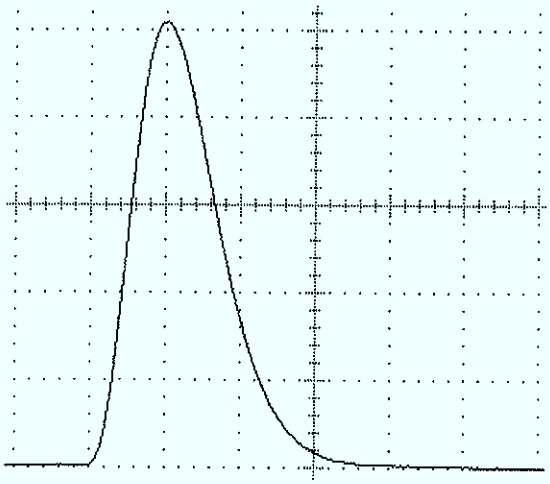


Figure 97 Impulse response, the horizontal scale is 100 ns/div and the vertical is 200 mV/div

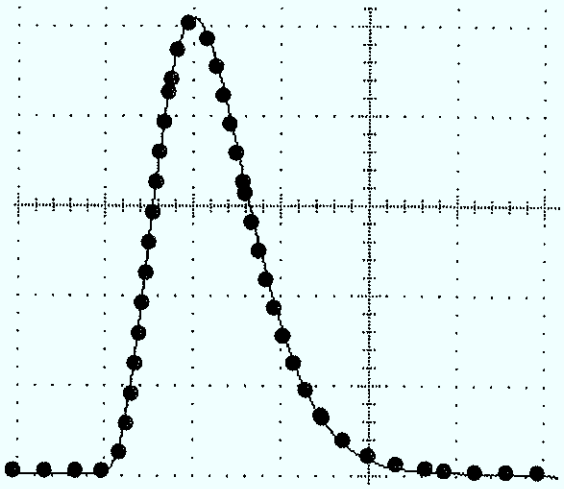


Figure 98 4th order semi Gaussian fit of the impulse response, the horizontal scale is 100 ns/div and the vertical is 200 mV/div

4.8.5 Requirement – Simulation –Test Results

Parameter	Requirement	Simulation	Test Result
Noise (ENC)	1000 e	322 e @10pF	270 e @10 pF
Conversion Gain	10 mV / fC	10mV / fC	8.7 mV / fC
Peaking Time	100 ns	About 100ns	About 100 ns
Nonlinearity	< 1 %	< 1 %	< 1 %
Power Consumption	< 20 mW / channel	10 mW/channel	10 mW/channel
Dynamic Range	> 10 bit	11.5 bit	11.5 bit
Area	< 3 mm2		

Table 4

Chapter 5

Programmability

5.1 Both Polarities

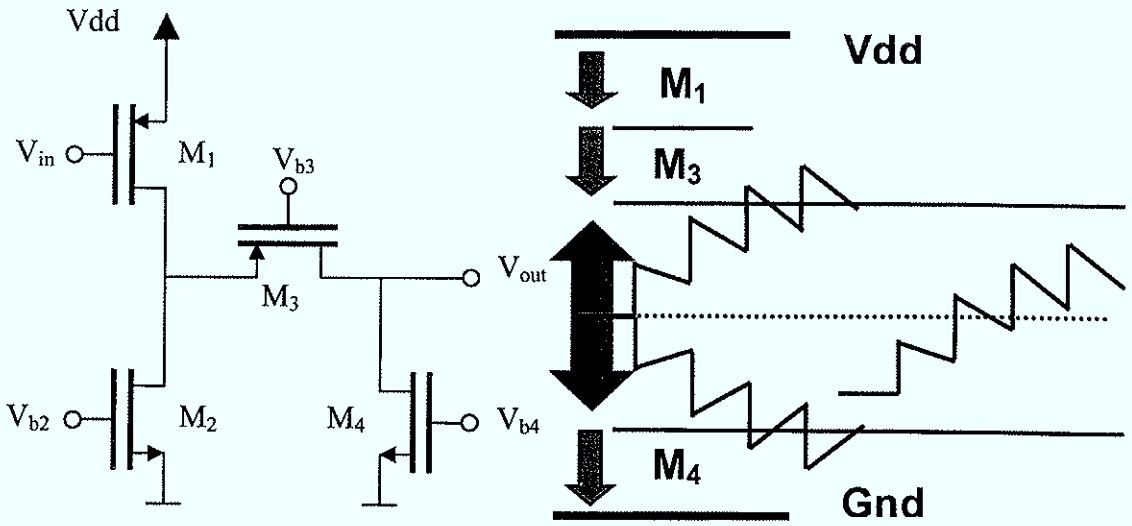


Figure 99 Operational point adjustment for expected polarity

Especially at low supply voltages the swing at the cascode output is strongly limited. Figure 99 suggests the placement of DC operating points depending on the expected signal polarity.
A very effective way of overcoming the pile up problem is the preamplifier working in transimpedance mode. But the fast discharge results in additional current noise contribution that is not acceptable for many applications.
A rail to rail preamplifier extends the voltage range, suggesting the use of a differential preamplifier or the folded cascode followed by a moderate gain amplifier. This approach can be combined with the transimpedance mode by taking advantage of the nonlinear resistance of a MOS transistor. At output voltages near to the boarders of the allowed output swing, the discharge resistance is sufficiently low so that these boarders are not exceeded, even for the highest expected pulse rate. The prototype was designed in a way that three consecutive maximum charge pulses can be handled by the preamplifier. Also consecutive maximum charge pulses separated by 2 µs in time do not saturate the input stage.

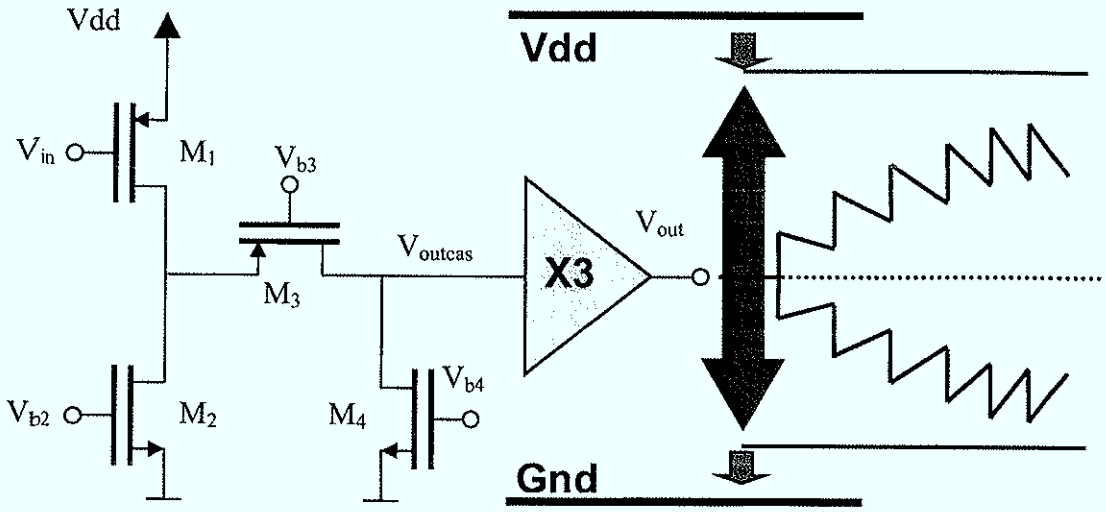


Figure 100 Rail to rail preamplifier

The operational point set to Vdd/2 gives enough voltage room for both signal polarities. The big advantage of this approach is that no switching of passive components in the preamplifier stage is necessary. But on the other hand the realization of the double sided decrease of the time constant calls for a PMOS/NMOS discharge network. This clearly increases complexity but makes the circuit suitable for a broad range of applications.

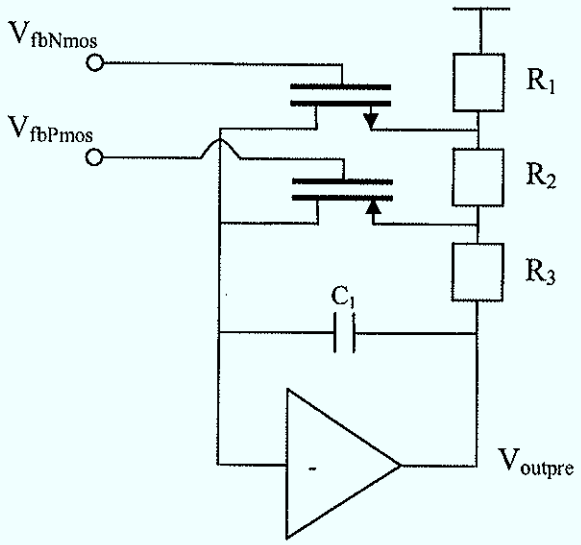


Figure 101 PMOS NMOS feedback

The voltage divider formed by R_1, R_2 and R_3 determines together with the virtual ground potential the output DC. For rising/falling V_{outpre} the NMOS/PMOS feedback is becoming more conductive. This architecture is also compatible with the principle of pole zero cancellation.

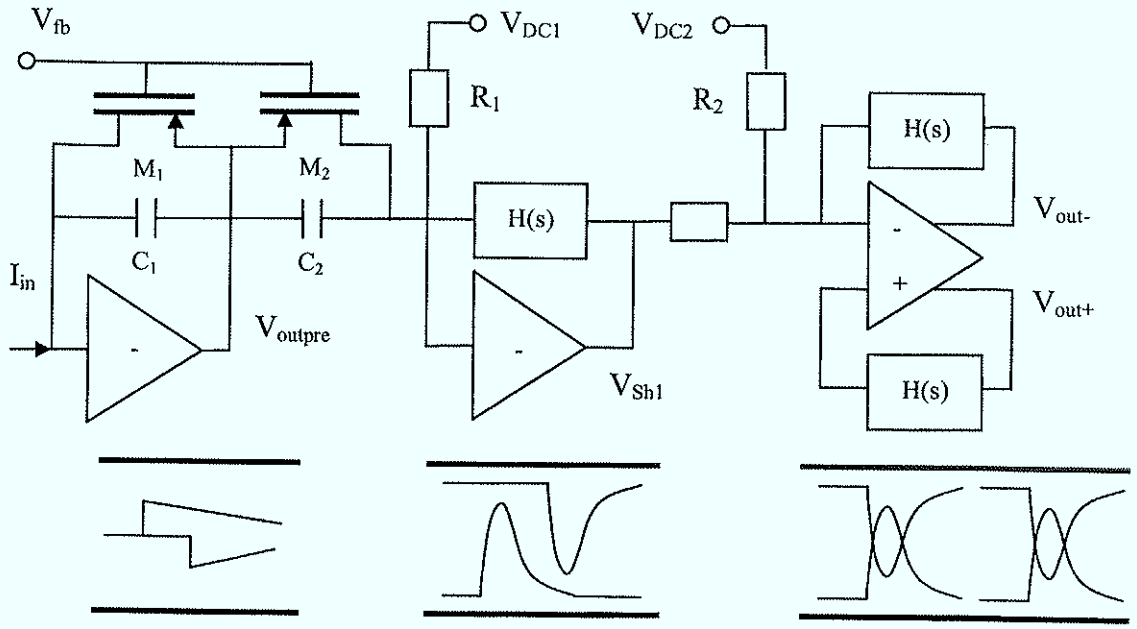


Figure 102 DC levels of shaping stages

The gain at shaper one is very important for the noise contribution of the following stages. Therefore it proves useful to maximize the voltage room by setting DC levels according to the expected signal. Different DC levels at shaper one cause different DC conditions at shaper two. R_1 and R_2 are in charge of shifting the output DC. Voltage references complicate the system level design but allow compensation for process variations of the baseline.

5.2 Current Division Principle

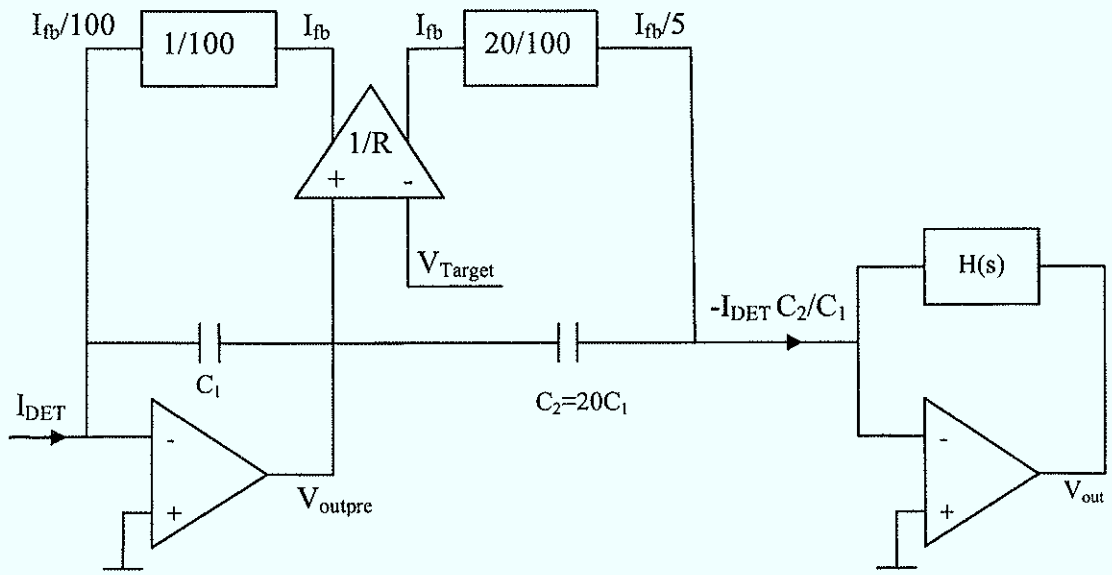


Figure 103 Output DC is set independently of input DC

The transconductor generates a current from the voltage difference between V_{Target} and V_{outpre}. A division network applies the scaled down current to the preamplifier input. In case of an ideally linear transconductor no current has to be supplied to the shaping amplifier and the pole could be cancelled with a passive RC network. But one could also take advantage of nonlinear discharge and implement on purpose a nonlinear transconductor, knowing that the introduced nonlinearity gets compensated by the principle of pole zero cancellation. A disadvantage of the proposed scheme is the current mirror at the preamplifier. To bias it, a steady current has to be applied that introduces current noise.
Leakage current compensation circuits are built in a similar way. A low frequency feedback detects constant deviations from the original operational point and corrects for it.

5.3 Conversion Gain – Shaping Time

There are several ways of changing the conversion gain. One possibility is given by the replacement of resistors with transistors in the shaping amplifier. The transistors' V_{GS} can be used to change gain and shaping time. Due to the better linearity of passive RC filters, only the switching of passive components to alter conversion gain and shaping time was investigated.

Motivation for changing the gain and shaping time:

- Compensate for process variations
- Change gain according to the maximum expected signal
- Match amplifier output to ADC input range
- Make the intrinsic amplifier noise larger than the system noise level

- ...

5.3.1 Preamplifier Gain Adjustment

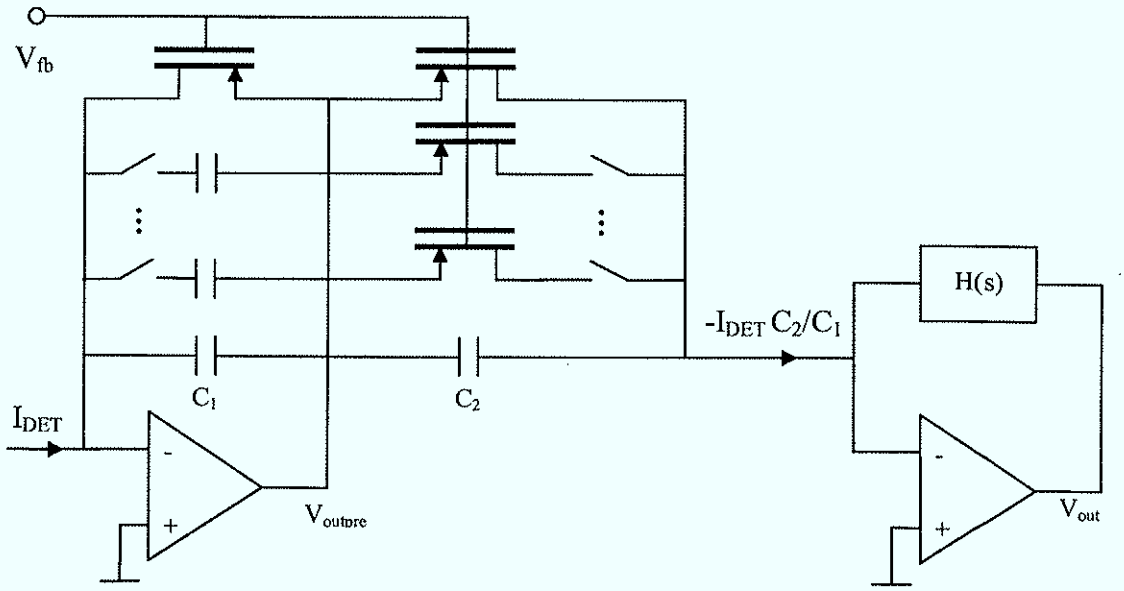


Figure 104 Gain adjustment in the first stage

The current gain from the first to the second stage is determined by the ratio of C_2 and C_1. Additional feedback capacitance extends the input charge range but also increases the discharge time constant. The preamplifier is the most critical part of the system. Changing C_f influences the phase margin of the closed loop what has to be taken into account. To compensate for different rise times also the size of the compensation capacitor has to be modified according to the new feedback configuration.
In order to preserve pole zero cancellation ($C_{pz}R_{pz} = C_fR_f$), also the time constant built by C_2 and its discharge resistor has to be modified in the same way like the preamplifier discharge time constant.

5.3.2 Shaper Gain and Peaking Time Adjustment

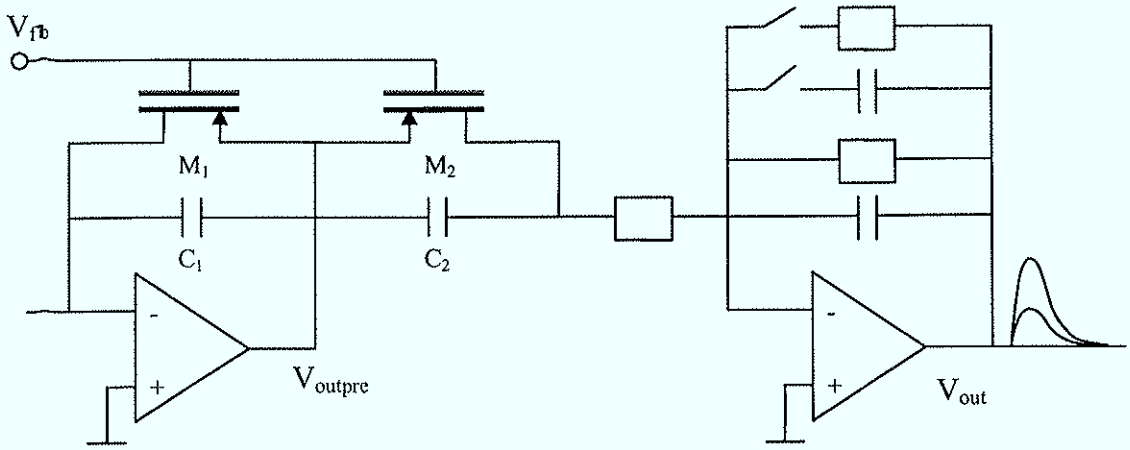


Figure 105 Gain adjustment in the 2nd stage

Figure 105 depicts a more attractive way of changing the overall gain because the pole zero cancellation network remains unmodified. The CSA should be able to handle signals of maximum pulse rate and charge. The 1st shaping stage is used for gain and peaking time adjusted. Special care has to be taken that all time constants are modified in the same way in order to preserve the pulse shape.
Also noise considerations play an important role. The gain should be large enough so that following shaping stages only contribute negligibly to the overall noise.

5.3.3 Programmable Preamplifier and Shaper

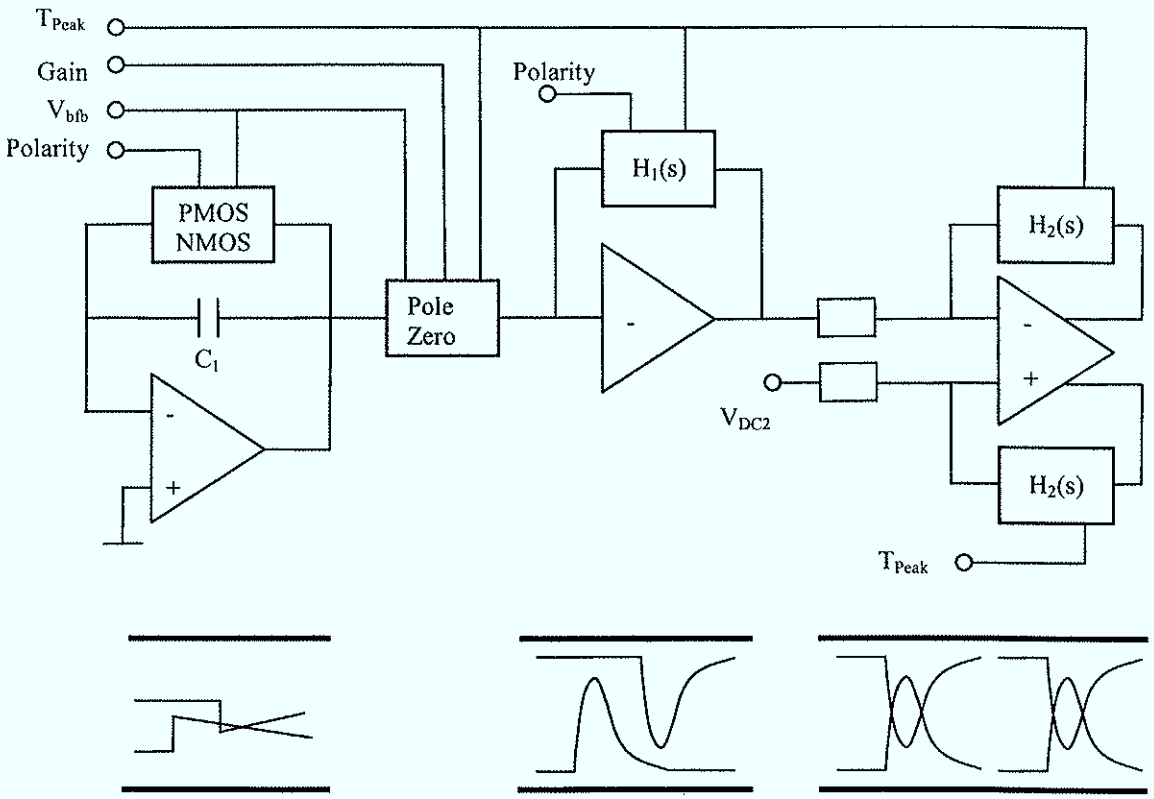


Figure 106 Programmable polarity, gain and peaking time amplifier

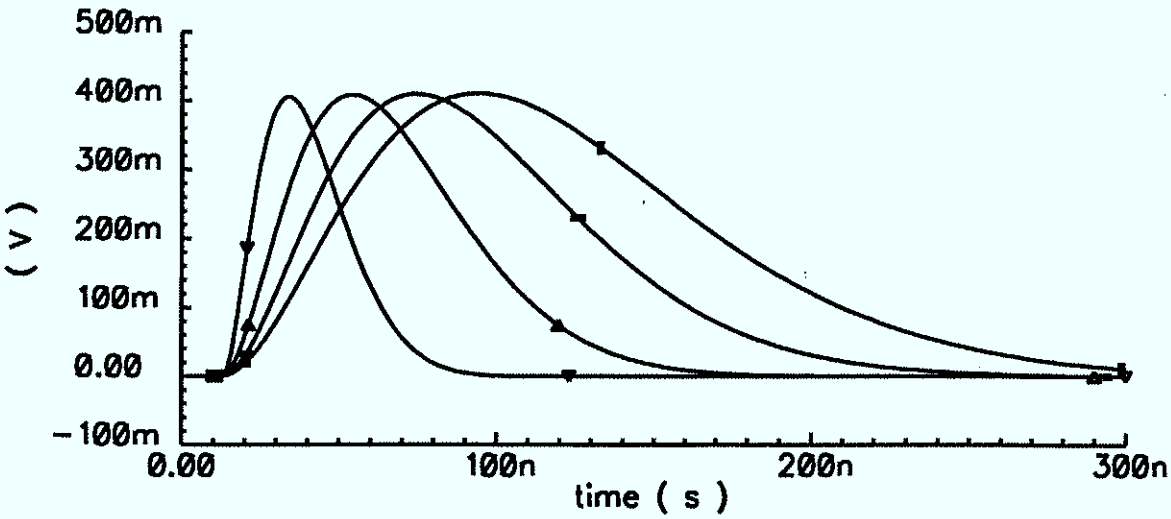


Figure 107 Programmable peaking time (20 – 100 ns)

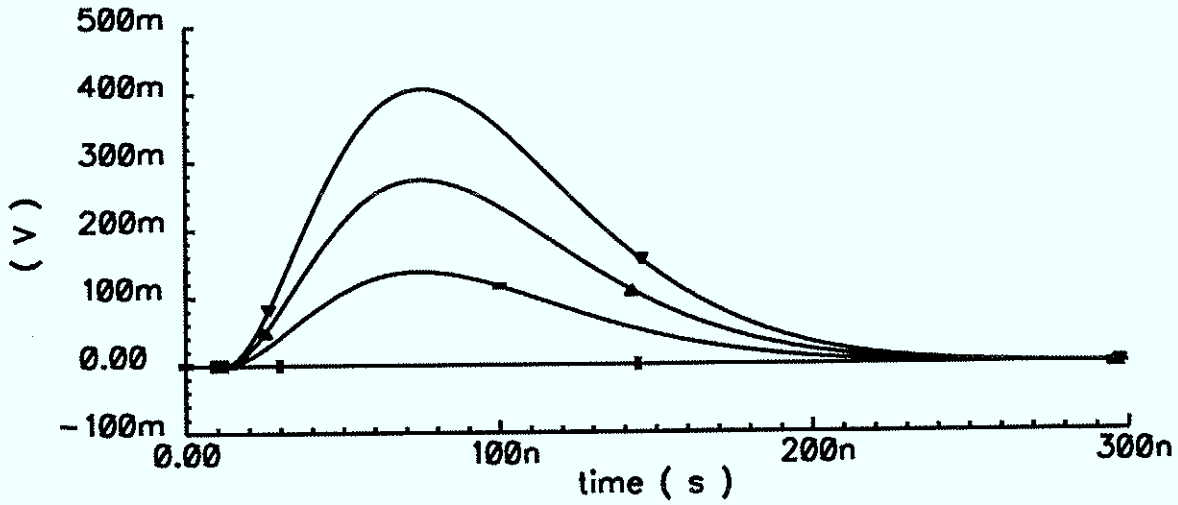


Figure 108 Programmable gain (10, 20 and 30 mV/fC)

5.3.4 Dynamic Range Increase with Redundant Structures

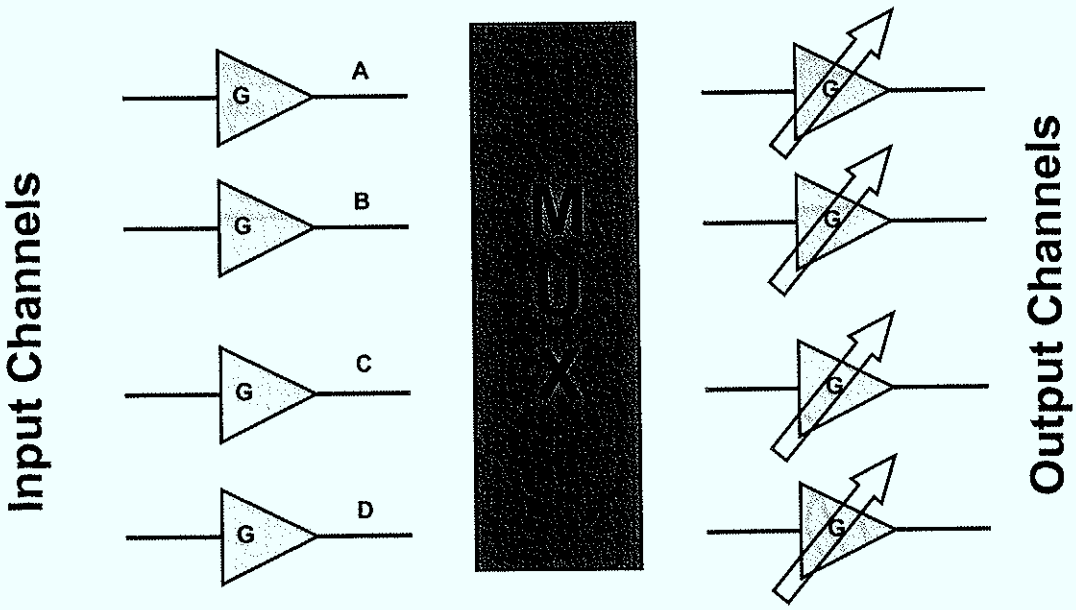


Figure 109 Multiplexer routs preamplifier outputs to programmable gain shaping amplifiers

Under normal operating conditions each preamplifier output is connected to shaping stages with uniform gains.

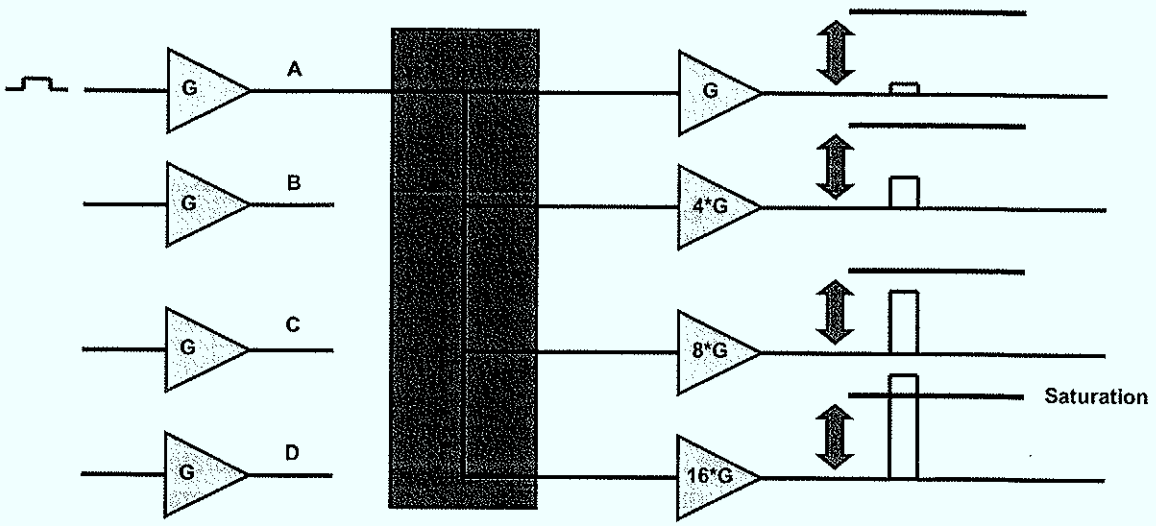


Figure 110 Trade off between maximum number of channels and dynamic range

An ADC of a certain resolution digitizes the signal after shaping. The resolution can be improved by using piecewise linear approximation. Each ADC samples only a portion of the complete charge range.

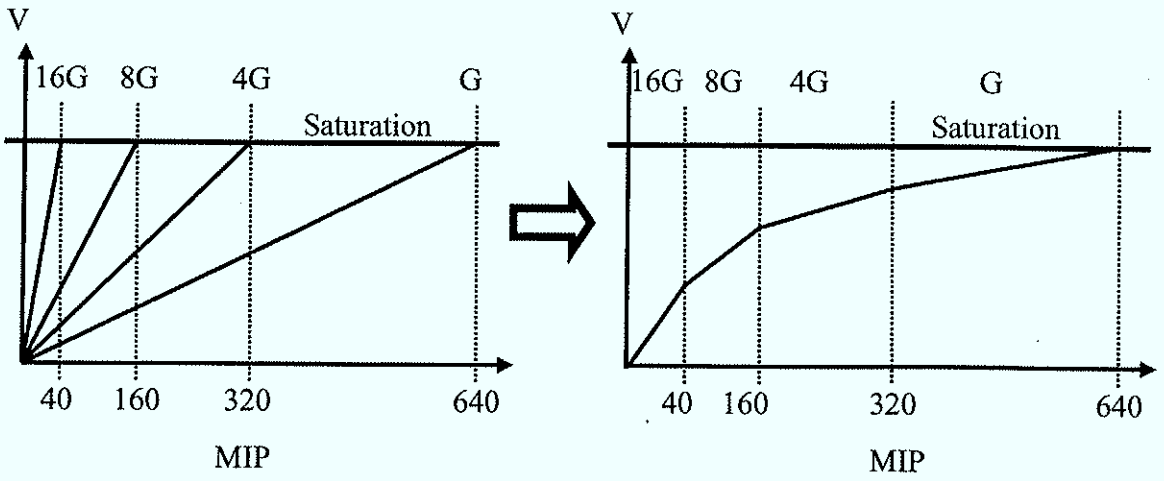


Figure 111 Piecewise linear approximation of a logarithmic amplifier

5.4 Charge Sampling Amplifier (QSA)

5.4.1 KTC Noise

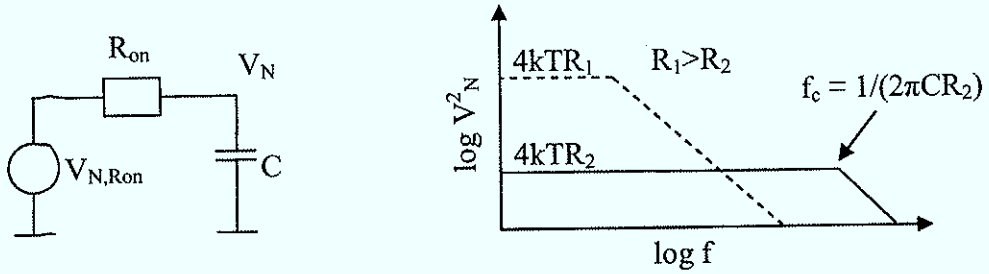


Figure 112 Sampling noise

A capacitor does not generate noise but it is a component that can accumulate it. Figure 112 shows a sample and hold circuit during the sampling phase. Noise generated by the on resistance of the sampling transistor appears low pass filtered at the sampling capacitor. When the switch opens, the noise voltage is frozen. A larger resistance induces more noise but lowers at the same time the cut off frequency. It can be shown that the integrated noise over all frequencies is independent of the resistance: [12]

$$\frac{V_{out}}{V_{N,Ron}}(s) = \frac{1}{RCs+1} \tag{5.1}$$

$$\overline{V_N^2} = \int_0^\infty \frac{4kTR_{on}}{4\pi^2 R_{on}^2 C^2 f^2 + 1} df \tag{5.2}$$

$$\int \frac{1}{x^2+1} dx = \tan^{-1}(x) \tag{5.3}$$

$$\overline{V_N^2} = \frac{kT}{C} \tag{5.4}$$

Only the size of the sampling capacitor determines the noise power:

Size of capacitor	T	Sampling noise
10 pF	300 K	20 10^{-6} V_{rms}
1 pF	300 K	64 10^{-6} V_{rms}
100 fF	300 K	203 10^{-6} V_{rms}
10 fF	300 K	643 10^{-6} V_{rms}

Table 5

KTC noise limits the performance of switched capacitor circuits. In general sufficiently large capacitors must be taken to fulfill the requirements on noise, thus degrading other circuit parameters like power and speed.

5.4.1.1 SC Integrator Noise

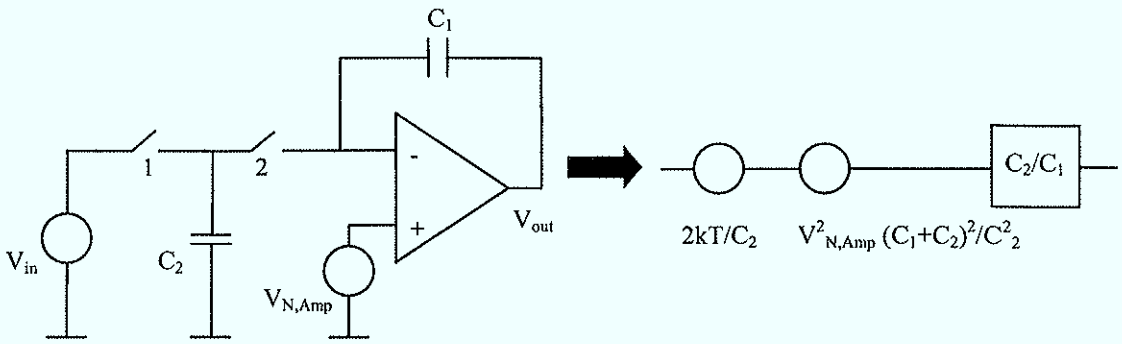


Figure 113 SC integrator

$$V_{out}(z) = V_{out}z^{-1} + V_{in}\frac{C_2}{C_1} \tag{5.5}$$

$$\frac{Vout}{Vin}(z) = \frac{C_2}{C_1}\frac{1}{1-z^{-1}} \tag{5.6}$$

Noise constraints force a minimum size for the sampling capacitor.

5.4.2 Principe of Operation

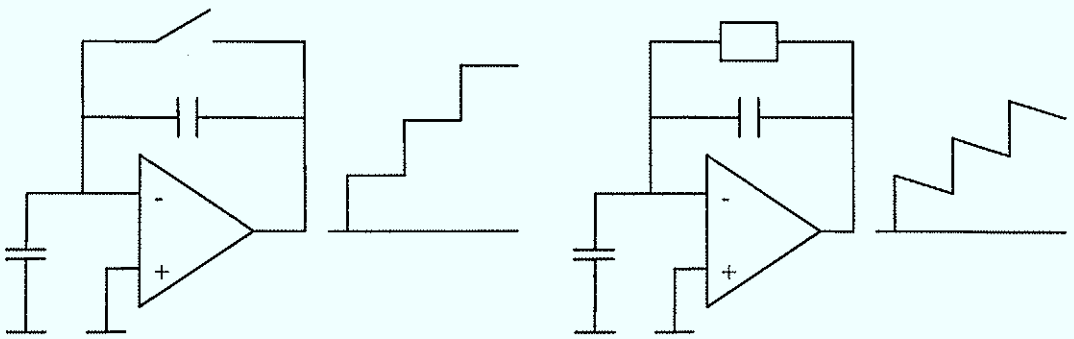


Figure 114 Gated integrator vs. continuous discharge

If the arrival time of the detector signal is known a gated integrator can be used as front-end amplifier. The switch is always closed to reset the feedback capacitor and before the arrival of the signal the feedback transistor opens. This process induces random kTC noise across the feedback capacitor. Techniques like correlated double sampling are available to improve the noise performance.
The continuously sensitive configuration uses a parallel resistor for the discharge. Especially at long peaking times noise constraints force this resistor to be in the MΩ region. As indicated in Figure 114 a big time constant of the CSA leads to pulse pile up. Nowadays at low supply voltages the available voltage room is strongly limited what makes

preamplifiers working in the transimpedance mode more attractive. Combining both approaches and introducing a SC feedback the gated integrator disadvantage of dead time can be removed.

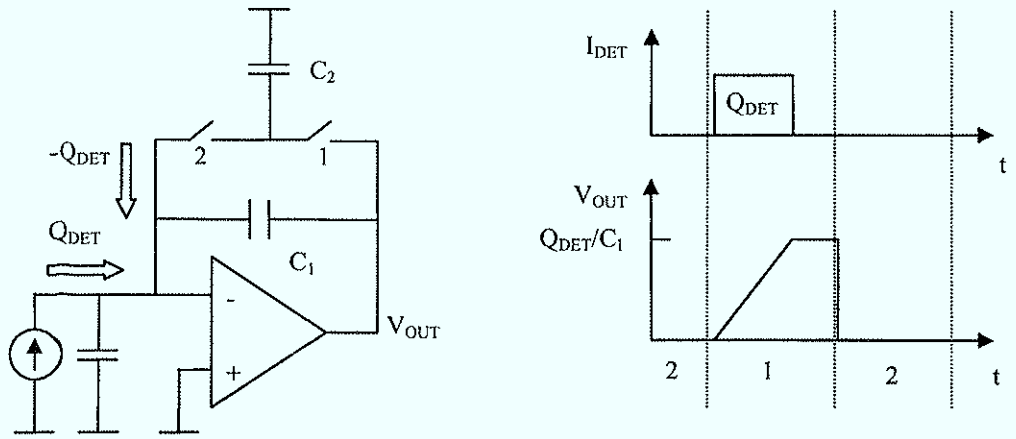


Figure 115 Principe of operation

For $C_1 = C_2$, C_1 gets completely discharged each clock cycle and no charge remains on the detector capacitance.

5.4.3 Read Out

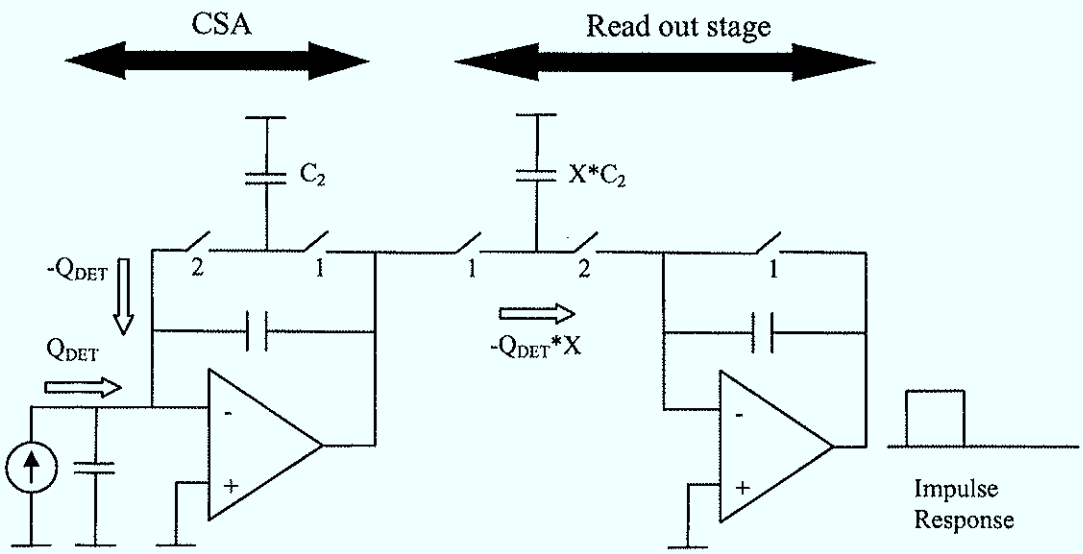


Figure 116 Charge sampling amplifier

At the end of clock phase 1 the same voltage is sampled onto C2 and X*C2. Since the coupling branch between CSA and read out stage is built of X multiples of the CSA's feedback branch every systematic distortion like clock feed through and power supply

noise injected to the input will be also injected to the read out stage. Neglecting kT/C switch noise the injected inverse signal is exactly known.
If the clock period is much smaller than the duration of the detector pulse many samples are taken. But imagine the detector pulse is shorter than a clock cycle. The information about the arrival time is limited to the clock period. Therefore the basic QSA architecture was modified:

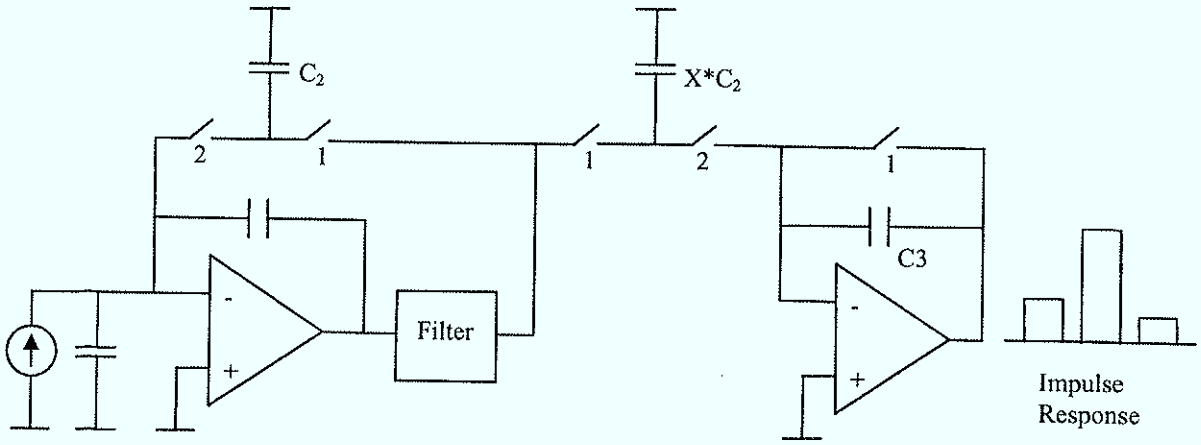


Figure 117 Charge sampling amplifier with increased timing resolution

The analogue low pass filter after the CSA broadens the detector pulse to several clock periods.

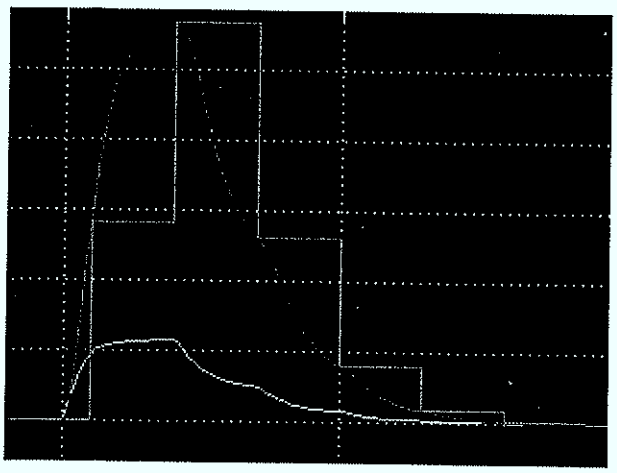


Figure 118 Fraction of charge cancelled at each clock cycle

Due to the limited bandwidth within the feedback loop, the feedback factor had to be reduced in order to preserve stability. Now only a portion of the detected signal gets cancelled within one clock cycle. Figure 118 shows a configuration where basically after 7 clock cycles all of the integrated charge is removed.
The architecture of Figure 117 is also easily programmable. The size of C_3 changes the gain, whereas the cut off frequency of the filter block changes the impulse response.

The moving average filter (MAF) constitutes one of the possible post processing strategies. The smoothing filter after the MAF serves only for illustration purposes. The following figure clarifies the importance of the filter after the CSA to preserve time resolution. The MAF sums up signals that were injected over a certain number of clock cycles.

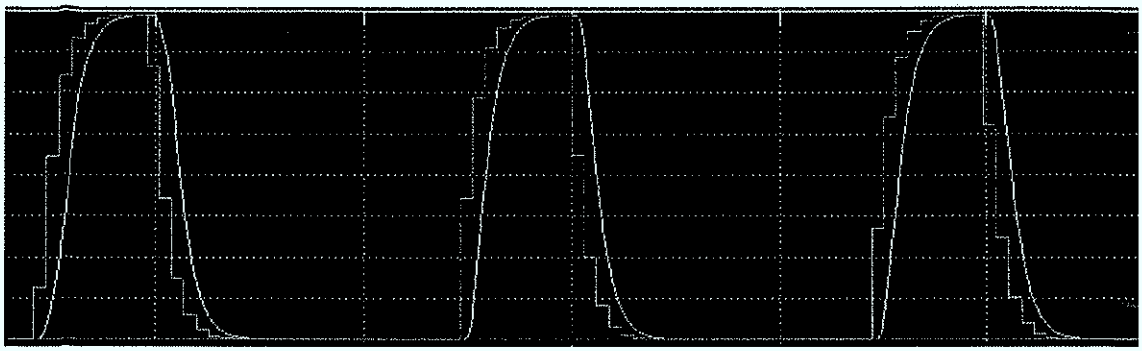


Figure 119 QSA followed by a moving average filter (MAF).

5.4.4 Noise Analysis

Although a capacitor is a noiseless component the switched capacitor feedback will induce extra noise like it is the case for every added component. But what amount of noise?

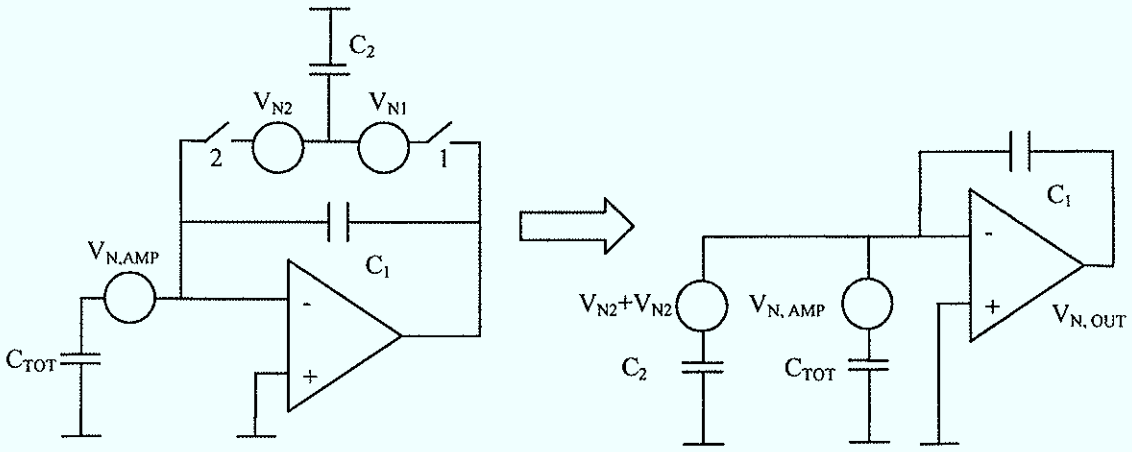


Figure 120 Noise at the end of clock cycle 2

$C_{TOT} = C_{Det}+C_1+C_{parasitic}$, $R_{ON} <<$

$$V_{N1}^2 = V_{N2}^2 = \frac{kT}{C_2} \tag{5.7}$$

Considering the two switching operations uncorrelated:

$$V_{N,OUT}^2 = \frac{\left(V_{N1}^2 + V_{N2}^2\right)\cdot C_2^2 + V_{N,AMP}^2 C_{TOT}^2}{C_1^2} \tag{5.8}$$

The output noise is dominated by the amplifier noise for big detector capacitances, large amplifier noise and small C_2. The switching feed back adds series noise to the amplifier output that does not scale with the detector capacitance. In contrary to the noise derivation of the SC integrator the minimum sampling capacitor will deliver the best noise performance.

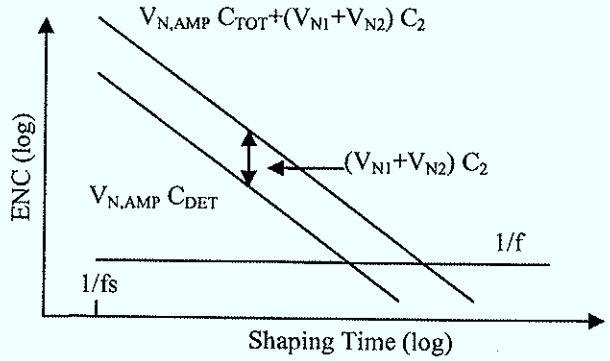


Figure 121 Illustration of noise increase

At first sight it looks rather strange that the switched capacitor feedback introduces series noise because its equivalent resistance would suggest a parallel noise contribution. Due to the non typical charge readout scheme the feed back signal can be regarded as an inverse signal getting corrupted by the kT/C noise that has a white frequency spectrum up to the cut off frequency.

The SC discharge mechanism introduces additional series white noise. An increase in shaping time improves ENC always.

To what accuracy can the CSA output be feed back to the input?

Size of capacitor	$2kTC_2$	$2kTC_2$	T
10 pF	$288\ 10^{-18}\ C_{rms}$	$1798\ el_{rms}$	300 K
1 pF	$91\ 10^{-18}\ C_{rms}$	$569\ el_{rms}$	300 K
100 fF	$29\ 10^{-18}\ C_{rms}$	$179\ el_{rms}$	300 K
10 fF	$9\ 10^{-18}\ C_{rms}$	$56\ el_{rms}$	300 K

Table 6

$$V_{N,OUT}^2 = \frac{2kT \cdot C_2 + V_{N,AMP}^2 C_{TOT}^2}{C_1^2} \qquad (5.9)$$

Assuming a noiseless amplifier $2kTC_2$ is the only noise and sets the ultimate limit for the ENC. For C_2 = 100 fF each clock cycle the charge is cancelled with an accuracy of 179 el_{rms}.

Let sample 1 until n be independent normal random variables each of which has mean μ and variance σ^2. Then the following holds. [34]

The sum $X_1 + \ldots + X_n$ is normal with mean $n\mu$ and variance $n\sigma^2$

- The following random variable $\overline{X}$ is normal with mean μ and variance σ^2/n

$$\overline{X} = \frac{1}{n}(X_1 + \cdots + X_n)$$

The mean μ is 0 for the case where no charge is stored on the feedback capacitor before the first sample. After 10 clock cycles, 10 random samples are taken. Calculating the mean of these samples reduces the initial inaccuracy of 179 el_{rms} to 56 el_{rms}.

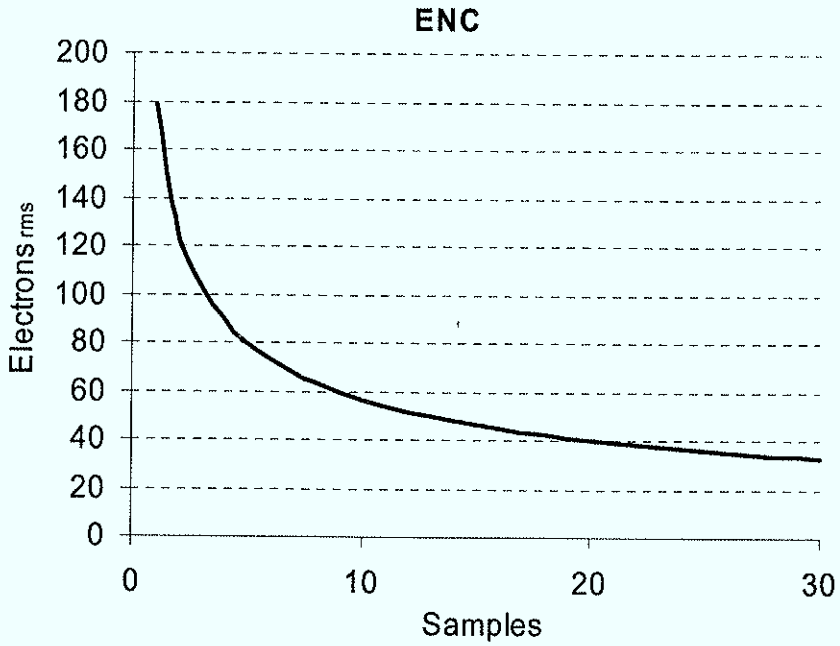


Figure 122 Theoretically possible ENC for 100 fF

The noise contribution of the read out stage can be minimized by selecting sufficiently large capacitors as it was shown in noise the calculation of the switched capacitor integrator.
In the presence of switching digital circuitry together with highly sensitive analogue circuitry on the same substrate the use of differential preamplifier topologies could prove useful in order to minimize substrate coupling effects. However this would increase the amplifiers noise and therefore the theoretically possible ENC.

5.4.5 Digital Post Processing

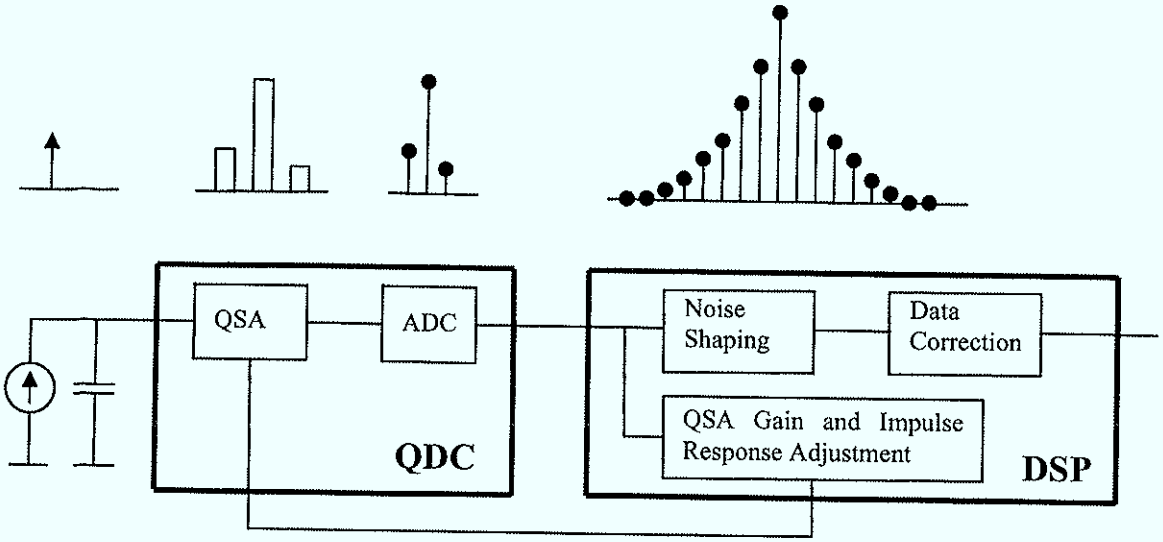


Figure 123 Channel architecture

Digital processing allows applying arbitrary filtering techniques. Whereas with analogue filters it is not easily possible to produce certain pulse shapes. Triangular or trapezoidal pulses with a flat top for ballistic deficit immunity are technically easier feasible with digital pulse shaping.
The QSA is the input stage of the ADC. Since the QSA delivers information on charge detected within one clock cycle, the combination of QSA and ADC can be regarded as charge to digital converter (QDC).

- Charge information
  - Sum of QDC samples
  - Distribution of QDC samples gives information about the original detector signal
- Noise shaping
  - Choose noise shaping filter according to the requirements
    - Parallel noise
    - Series noise
    - Pile up
    - Flat top pulse for ballistic deficit immunity
    - Fast channel, slow channel
- Adjustment of analogue parameters
  - QSA gain
  - QSA impulse response
- Data correction
  - Baseline restoration
    - Additional 1/f noise reduction
  - Removal of systematic errors

- Constant charge injection
- Systematic distortion of the detector signal (closing of gating grid)
- Tail cancellation

o Zero suppression
o Data formatting
o ...

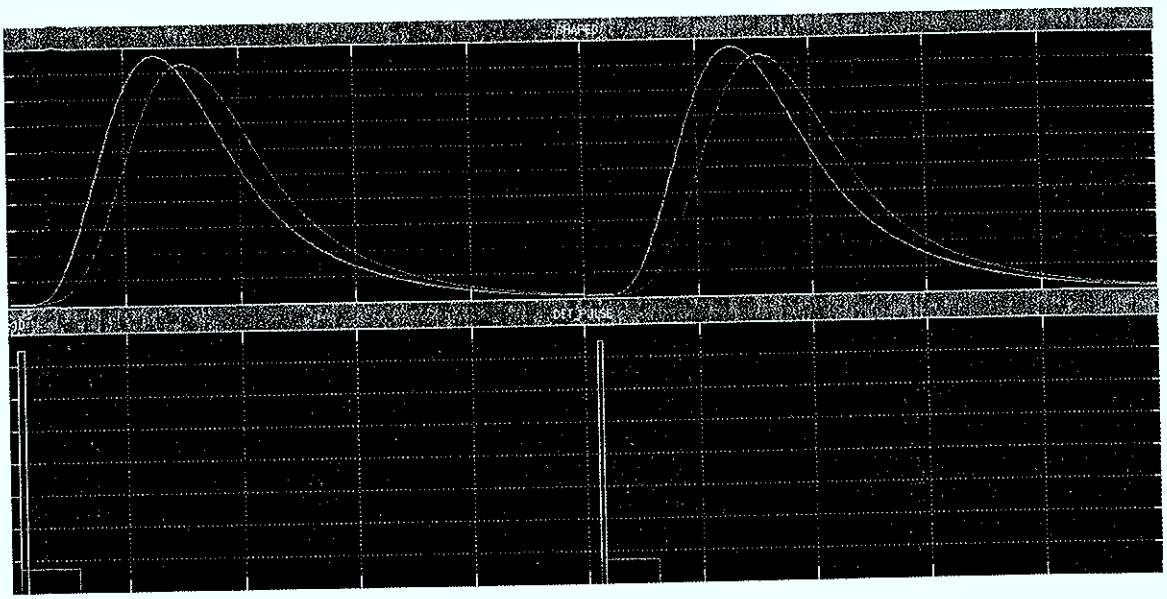


Figure 124 Ballistic deficit

As long as the detector current pulse is much shorter than the shaper peaking time, the amplitude of the shaped signal is a direct function of the released charge. The amplitude and the pulse shape change with the detector pulse duration (ballistic deficit).

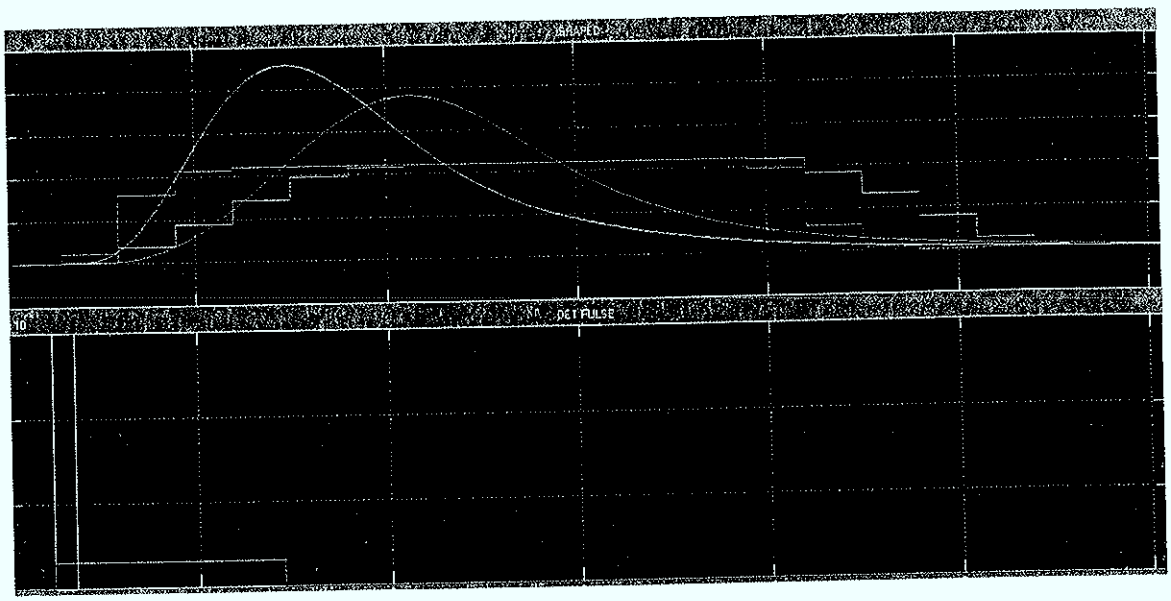


Figure 125 MAF avoids ballistic deficit

The peak amplitude of the MAF stays the same (flat top).

Extraction of pulse features

The presented concept of shaping does not rely on a given pulse shape. The only relevant information is the released charge and the time of arrival.

Charge:
The integral of the pulse is proportional to the charge released by the detector.

Time:
In general, when the shape is exactly known the time of arrival can be computed by samples taken from the pulse. Also discrimination is used where the measured time of arrival is a function of the pulse amplitude.
In the case of the QDC the available information is not an analogue waveform. It delivers information about accumulated charge within the last clock period. Because of that the QDC delivers different pulse shapes depending on the phase between time of arrival and clock period. Taking into account that the pulse shape is a function of phase, the time of arrival can be reconstructed with accuracy much higher than the clock period.

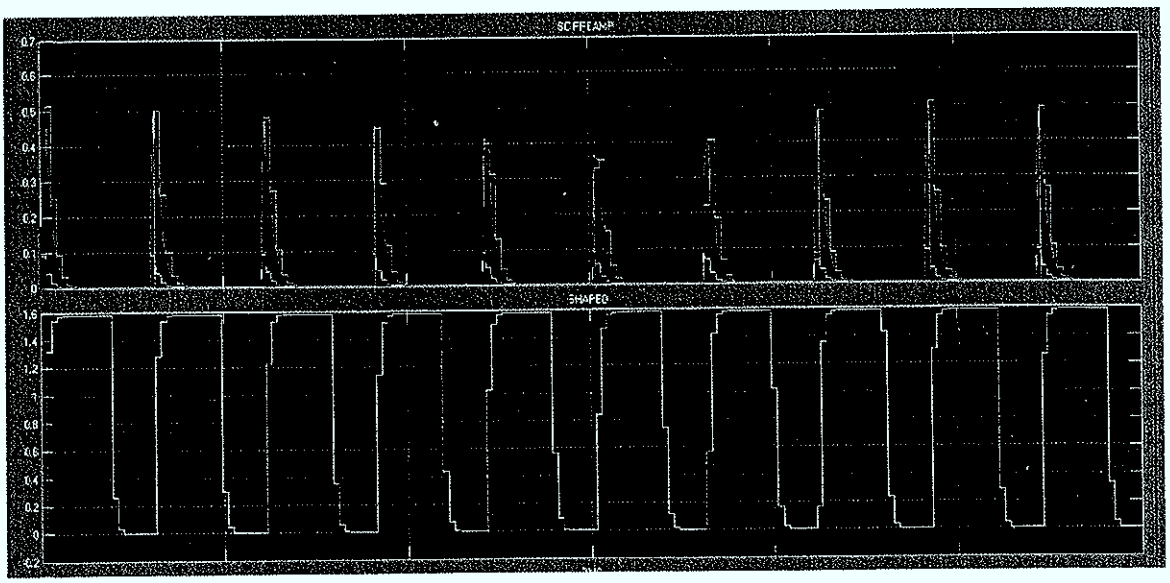


Figure 126 Pulses of different phase with respect to the clock

Figure 126 shows a series of pulses with different phase to the clock. As expected the peak amplitude does not change. But the rising/falling edge shows different shape depending on the phase. The amplitude of the first sample is a nonlinear function of the phase.
Timing information is available by means of an analog voltage. The maximum resolution achievable with this architecture is given by the clock period divided by the dynamic range.

5.4.6 Noise Simulation – A Time Domain Approach

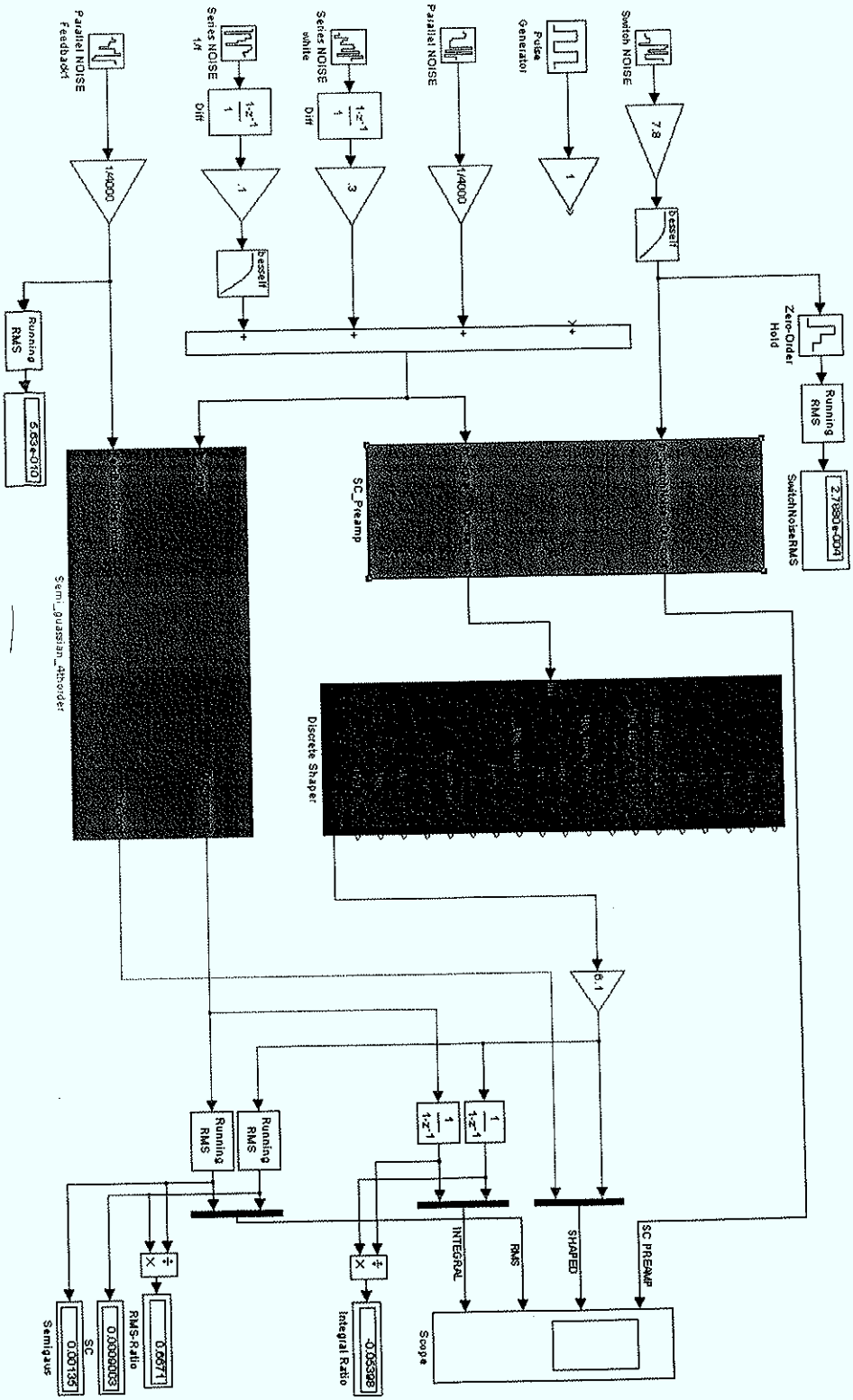


Figure 127 Simulink simulation model

Figure 127 depicts the Simulink model used for the noise characterization and comparison of the charge sampling approach with the conventional analog semi Gaussian filter. Noise sources are illustrated in red, the DSP in green, the QDC in blue and the analog filter in orange. The same signal and noise is applied to both systems.

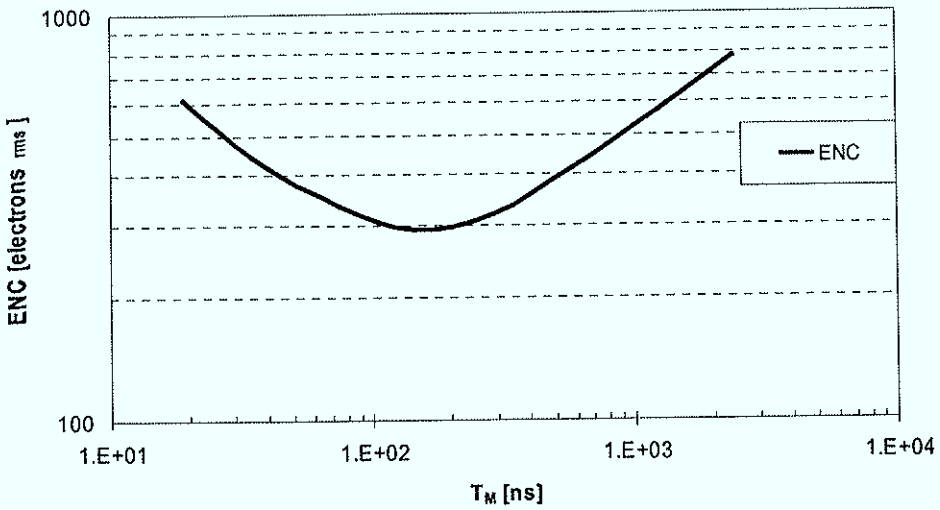


Figure 128 Analog 4th order semi Gaussian shaper

If no signal is injected the noise floor can be determined by measuring the rms of the output. By applying a predefined signal and measuring the peak amplitude the conversion gain is obtained. Changing the cut off frequency of the analog filter alters the peaking time. The ENC plot of Figure 128 was made by measuring noise floor and peak amplitude of the analog semi Gaussian shaper.

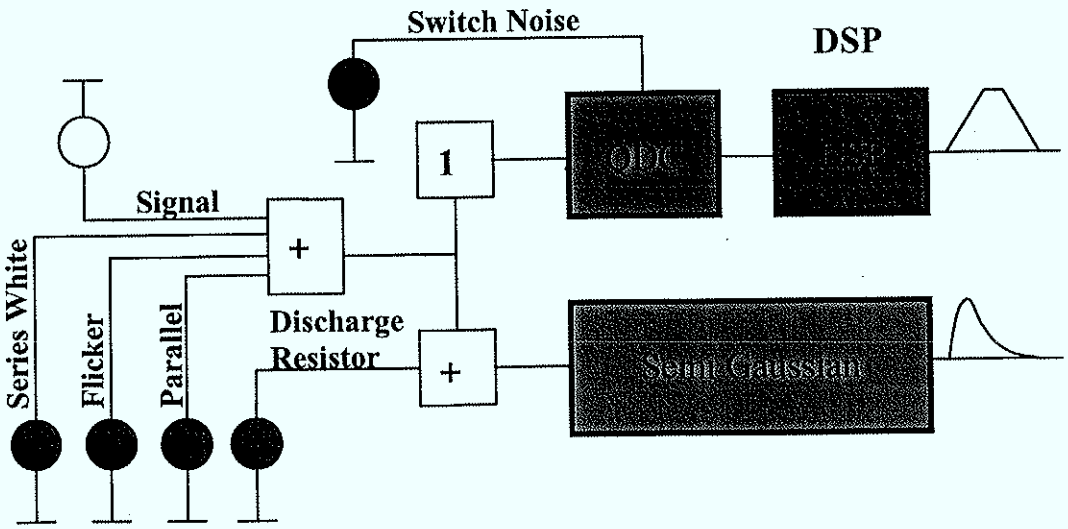


Figure 129 Performance comparison

Under ideal conditions and assuming that the switched capacitor feed back branch does not cause noise, no difference to the conventional architecture in terms of noise was observed. Shaping in the discrete time domain allows the choice of arbitrary pulse shapes. The additional series noise of the QSA can be minimized by choosing a pulse shape that has a lower series noise coefficient. Hence the truncated cusp that is very close to the optimum filter could be used for noise shaping.

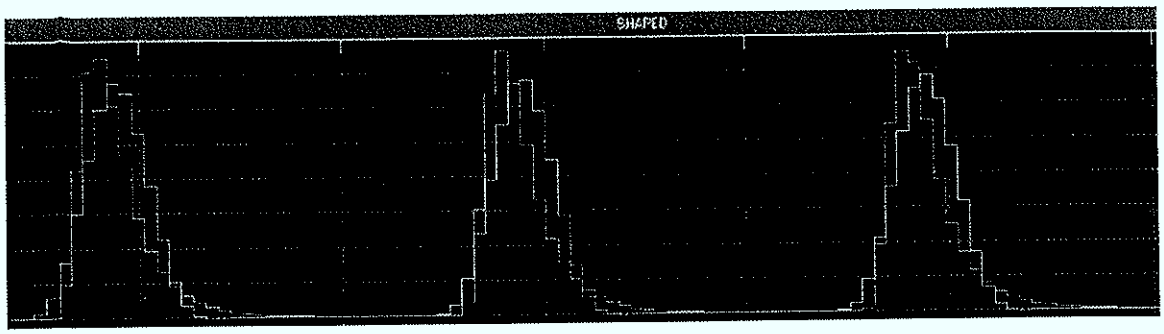


Figure 130 Pulse shape

Figure 130 depicts sampled semi Gaussian pulses (magenta) with 100 ns peaking time generated by an analog filter. The sampling period is 30 ns. The blue pulses are produced by a filter working in the discrete time domain. It consists of a triangular FIR filter (1 5 10 5 1) that is followed by two 5 tap moving average filters. Figure 131 shows the noise floor. Both discrete and analog filter show the same rms noise.

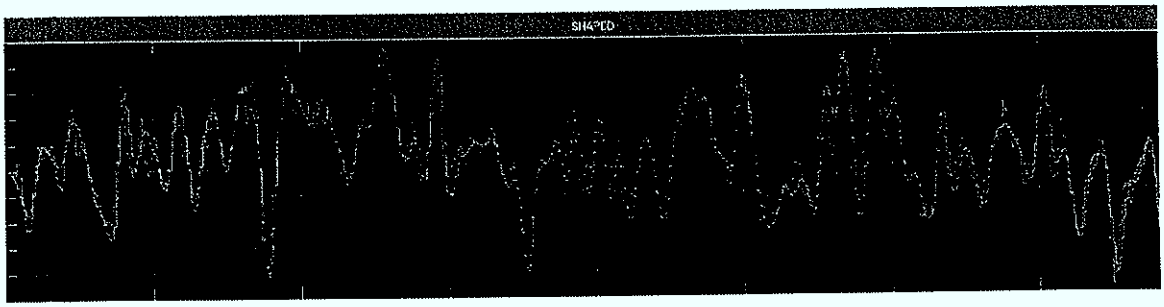


Figure 131 Simulated noise

Current noise estimation:

$$ENC = \sqrt{\frac{A_3\, 2kTt_M}{R_f}}\,\frac{1}{1.6\cdot 10^{-19}} \qquad (5.10)$$

R_f	T	A_3	t_M	$ENC_{parallel}$
10 MΩ	300K	1.85	100 ns	77 el_{rms}
1 MΩ	300K	1.85	100 ns	245 el_{rms}
0.1 MΩ	300K	1.85	100 ns	773 el_{rms}
0.05 MΩ	300K	1.85	100 ns	1094 el_{rms}

Table 7

Figure 118 suggests a discharge time constant in the order of 50 ns. Assuming 1 pF of feedback capacitance the equivalent resistance is calculated to 50 kΩ that corresponds to a noise contribution of 1094 el_{rms} at 100 ns peaking time.

How to quote signal to noise ratio?

If no fast ADC is available, peak stretching circuits are used to freeze the point with the largest SNR. In that case there is only one sample per pulse available. Under such conditions the definition of the ENC proves useful. If a pulse is sampled more often than only once, points with different SNR contribute to the pulse feature extraction algorithms. In that case the ratio between pulse-rms and noise floor seems to be more appropriate for determining the ENC.

In presence of white noise:

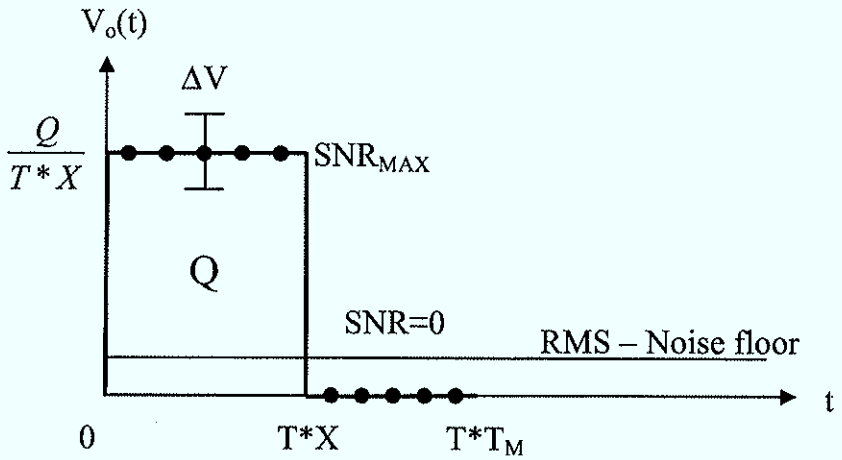


Figure 132 Pulse area is proportional to released charge

Under the assumption that the released charge is proportional to the area of the pulse the accuracy of the area measurement determines the overall ENC. For a constant sampling period T, pulse duration X and measurement time T_M, the area is given by:

$$Area = \sum_{i=1}^{T_M} (\Delta V_i + V_i) = Q + \sum_{i=1}^{T_M} (\Delta V_i) \tag{5.11}$$

$$Signal_{RMS} = \sqrt{\sum_{i=1}^{X} (V_i)^2} = \sqrt{\sum_{i=1}^{X} \left(\frac{Q}{TX} T\right)^2} = \sqrt{\sum_{i=1}^{X} \left(\frac{Q}{X}\right)^2} = \frac{Q}{X}\sqrt{X} = \frac{Q}{\sqrt{X}} \tag{5.12}$$

$$\sigma_{Area} = V_{N,RMS}\sqrt{T_M} \tag{5.13}$$

$$SNR = \frac{Area}{\sigma_{Area}} = \frac{Q}{V_{N,RMS}\sqrt{T_M}} \tag{5.14}$$

Sampling the signal after X where the SNR is zero worsens the area measurement. The maximum SNR for this pulse is described by:

$$SNR_{MAX} = \frac{Q}{V_{N,RMS}\sqrt{X}} = \frac{Singal_{RMS}}{V_{N,RMS}} \tag{5.15}$$

For constant noise floor, signals of same rms-value deliver same SNR. But not signals of same area. The comparison of analog- and SC-filter was carried out for pulses of same rms-value. The resulting noise floor indicates whether the analog- or the SC-filter shows better noise performance.

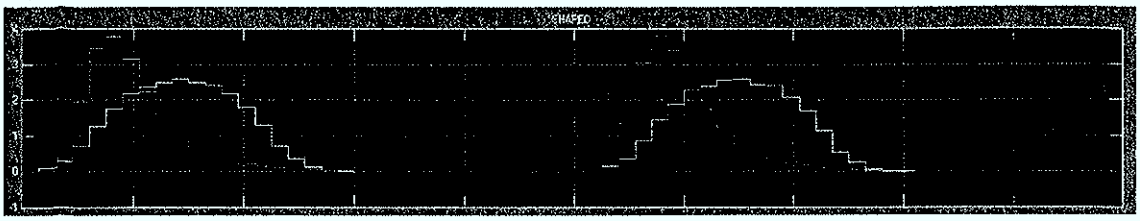


Figure 133 Two different pulse shapes with the same rms-value

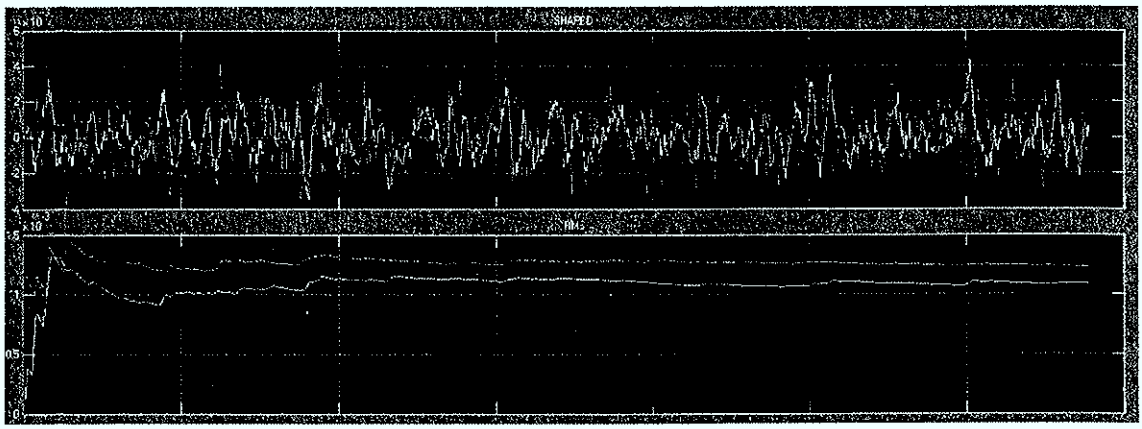


Figure 134 Noise floor of the systems in Figure 133

Figure 133 shows in yellow the switched capacitor and in magenta the sampled waveform of the analog processor. By choosing a different pulse shape, the additional noise from the SC feedback can be reduced. In this case the SC processor shows better noise performance but is inferior in terms of maximum SNR.

In the presence of white noise, pure integration (MAF) proves as best processing. [13]

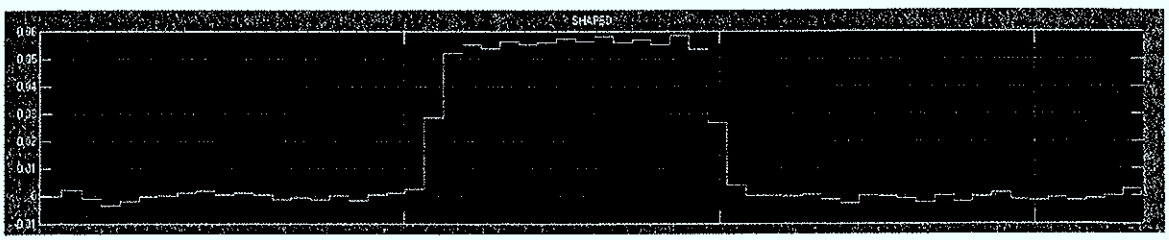


Figure 135 15 tap MAF filter

MAF pulse shape has several advantages:

- Fast rise time for timing measurement
- Flat top for ballistic deficit
- Flat top can be sampled many times to minimize noise

List of Abbreviations

ADC	Analog to Digital Converter
ALICE	A Large Ion Collider Experiment
ALTRO	Alice TPC Readout Chip
BNL	Berkeley National Laboratory
CERN	Conseil Européen pour la Recherche Nucléaire
CMOS	Complementary Metal Oxide Semiconductor
CSA	Charge Sensitive Amplifier
DIBL	Drain Induced Barrier Lowering
DSP	Digital Signal Processor
ENC	Equivalent Noise Charge
ESD	Electrostatic Discharge
FEC	Front End Card
FIR	Finite Impulse Response
GEM	Gas Electron Multiplier
GSI	Gesellschaft für Schwerionenforschung
IC	Integrated Circuit
ILC	International Linear Collider
LHC	Large Hadron Collider
LOCOS	Local Oxidation of Silicon
MAF	Moving Average Filter
MIP	Minimum Ionizing Particle
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPWR	Multi Project Wafer Run
MWPC	Multi Wire Proportional Chamber
NMOS	N – Channel Metal Oxide Semiconductor
PASA	Preamplifier Shaping Amplifier
PMOS	P – Channel Metal Oxide Semiconductor
PSD	Power Spectrum Density
PSRR	Power Supply Rejection Ratio
QDC	Charge to Digital Converter
QSA	Charge Sampling Amplifier
RCU	Readout Control Unit
RHIC	Relativistic Heavy Ion Collider
SC	Switched Capacitor
SEU	Single Event Upset
SI	Strong Inversion
SI	Switched Current
SNR	Signal to Noise Ratio
STAR	Solenoidal Tracker At RHIC
STI	Shallow Trench Isolation
TID	Total Ionizing Dose
TPC	Time Projection Chamber
WI	Weak Inversion

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