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PULSE POWER MODULATOR DEVELOPMENT FOR THE CLIC DAMPING RING KICKERS

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Abstract

The Compact Linear Collider (CLIC) study is exploring the scheme for an electron-positron collider with high luminosity (10^{-34} – 10^{-35} $cm^{-2}s^{-1}$) and a nominal centre-of-mass energy of 3 TeV: CLIC would complement LHC physics in the multi-TeV range. The CLIC design relies on Pre-Damping Rings (PDR) and Damping Rings (DR) to achieve the very low emittance, through synchrotron radiation, needed for the luminosity requirements of CLIC. To limit the beam emittance blow-up due to oscillations, the pulse power modulators for the DR kickers must provide extremely flat, high-voltage pulses: the 2 GHz specification called for a 160 ns duration flat-top of 12.5 kV, 250 A, with a combined ripple and droop of not more than ±0.02 %. In order to meet these demanding specifications, a combination of broadband impedance matching, optimized electrical circuit layout and advanced control techniques is required. A solid-state modulator, the inductive adder, is the most promising approach to meeting the demanding specifications; this topology allows the use of both digital and analogue modulation. This report describes the preliminary design of the inductive adder and the use of active-filtering control algorithms for achieving the required pulse waveform. The report introduces the components of the inductive adder and presents equations and reasoning for selecting the main components: semiconductor switches, storage capacitors and transformer cores. Dimensioning of the adder stack structure is also covered, for achieving good impedance matching between the adder stack and the load.

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Table of Contents

1. Introduction

The CLIC pre-damping (PDR) and damping ring (DR) kicker systems are challenging systems as they require low beam coupling impedance, high voltage and high current pulses and must be of high stability (low ripple and droop) [1]. In order to achieve the required low beam coupling impedance the pre-damping and damping ring kickers will be stripline devices [2-4]. Very high precision pulses are required for the extraction kickers from the CLIC damping ring and hence the impedance of the system must be well matched, or any impedance mismatches must be of a short electrical delay relative to the required rise and fall times. The pulse generator is an extremely important element in achieving the required high voltage, high current and very high precision, pulses.

The striplines for the kicker systems will be designed and built under the Spanish Program "Science for Industry". The research reported here concerns the pulse generator.

2. Specifications for the pulse generators of the DR and PDR kickers

The specifications for the CLIC PDR and DR kickers are shown in Table 1 below. The 2 GHz specifications called for a pulse width requirement of 160 ns for both the PDR and DR kicker systems. The rise and fall time may be up to 700 ns for the PDR kicker and 1000 ns for the DR kicker, but for several reasons the target rise time is approximately 150 ns: for example long rise and fall times increases stress for switches of the pulse generators and termination resistors of the kicker system. The flat-top stability requirements for the extraction kicker systems are extremely tight: $\pm 2 \times 10^{-3}$ for the PDR extraction and DR injection kicker and $\pm 2 \times 10^{-4}$ for the DR extraction kicker system. These correspond to ±0.2 % and ±0.02 %, respectively. An extensive literature survey of existing pulse generators has been carried out (see section 6. Literature Review); the flat-top stability requirement for the DR extraction kicker is tighter than for any high voltage pulse generator found in the literature. The output voltages and currents for the pulse generators are ±17 kV and ±340 A for the PDR kickers, and ±12.5 kV and ±250 A for the DR kickers, respectively.

Table 1: 2 GHz specifications for CLIC pre-damping ring and damping ring kicker systems.

	CLIC Pre-Damping Ring (PDR)	CLIC Damping Ring (DR)
Field rise time (ns)	700	1000
Field fall time (ns)	700	1000
Pulse flat-top duration (ns)	~160	~160
Flat-top reproducibility	$\pm 1 \times 10^{-4}$	$\pm 1 \times 10^{-4}$
Flat-top stability [incl. droop], (Inj.) per Kicker SYSTEM (Ext.)	$\pm 2 \times 10^{-2}$ $\pm 2 \times 10^{-3}$ (±0.2 %)	$\pm 2 \times 10^{-3}$ $\pm 2 \times 10^{-4}$ (±0.02 %)
Field inhomogeneity (%) [3.5mm radius] [1mm radius]	 ±0.1 (Inj.) ±0.1 (Ext.)	 ±0.1 (Inj.) ±0.01 (Ext.)
Repetition rate (Hz)	50	50
Pulse voltage per Stripline (kV)	±17	±12.5
Stripline pulse current [50 Ω load] (A)	±340	±250

3. Machine Protection and Reliability

Discussions concerning machine protection have emphasized the importance of reliability and redundancy of the kicker system:

- If only one of the two striplines is powered, the beam will receive 50 % deflection, in which case the high intensity beam could cause considerable damage to other equipment. This could result if a "single" switch were used for each stripline: multiple switches are desirable to reduce the probability of this situation occurring.

- Fast rise and fall times of the field are desirable, e.g. if beam is mistimed, with respect to the kick pulse: a fast rise and fall time will result in beam being swept faster across downstream materials and devices, minimizing potential damage.

4. Pulse Definition

Fig. 1 shows the pulse definition for the CLIC PDR and DR kickers.

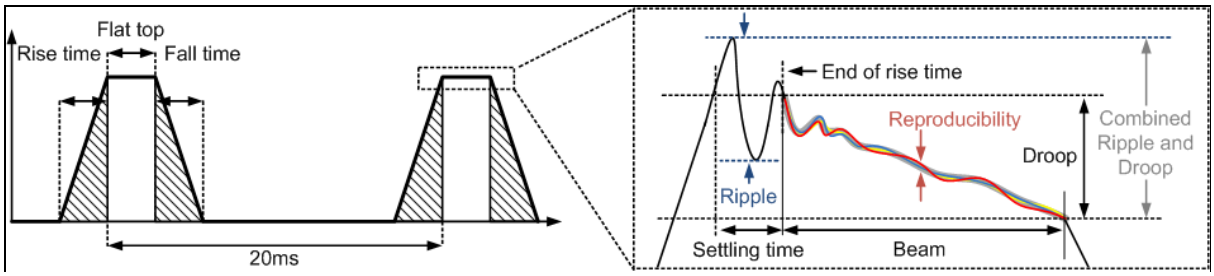

Figure 1: Pulse definition for the CLIC PDR and DR kickers.

- Rise time: time needed to reach the required flat-top voltage (includes settling time). Rise time of DR extraction: 1000 ns rise time allowed, ~150 ns desired;
- Settling time: time needed to damp oscillations to within specification;
- Beam: 160 ns time window during which any ripple and droop (i.e. flat-top stability) must be within specification;
- Flat-top stability: within $\pm 2 \times 10^{-4}$, for combined ripple and droop for DR extraction. This corresponds to a maximum, combined, ripple and droop of ±2.5 V for a 12.5 kV output pulse for the DR extraction kicker;
- Reproducibility: maximum difference allowed between any two pulses, of $\pm 1 \times 10^{-4}$;
- Fall time: time for voltage to return to zero. For DR extraction, 1000 ns allowed, ~150 ns desired.

To minimize settling time, the impedance of the system has to be well matched.

5. The Stripline Kicker System

Fig. 2 shows a simplified schematic of a stripline kicker system with an inductive adder. A stripline kicker consists of two parallel metallic electrodes which are connected at each end to the external circuit by feedthroughs. The two stripline plates are driven to an equal magnitude of voltage but of opposite polarity. The inductive adder feeds pulses towards the striplines. For simplicity, Fig 1. only shows one inductive adder which feeds the upper stripline. For feeding both striplines, either one bipolar or two unipolar inductive adders are required. The pulse propagates through the striplines and is then deposited in a terminating resistor. The characteristic impedance of the inductive adder, transmission lines, striplines and terminating resistors are matched as far as possible to minimize reflections, which could cause ripple on the flat-top of the deflection waveform.

The cross-section of the striplines will be optimized to achieve the desired characteristic impedance and the required field homogeneity. The beam coupling impedance defines the interaction of the beam with the striplines, resulting beam energy loss and beam shape perturbation. The beam impedance should be low to avoid beam instabilities and depends on the even-mode characteristic impedance of the stripline kicker [3]. In even-mode the striplines are not driven by the pulse generator and the characteristic impedance of the kicker depends on the proximity of each stripline to the beam pipe.

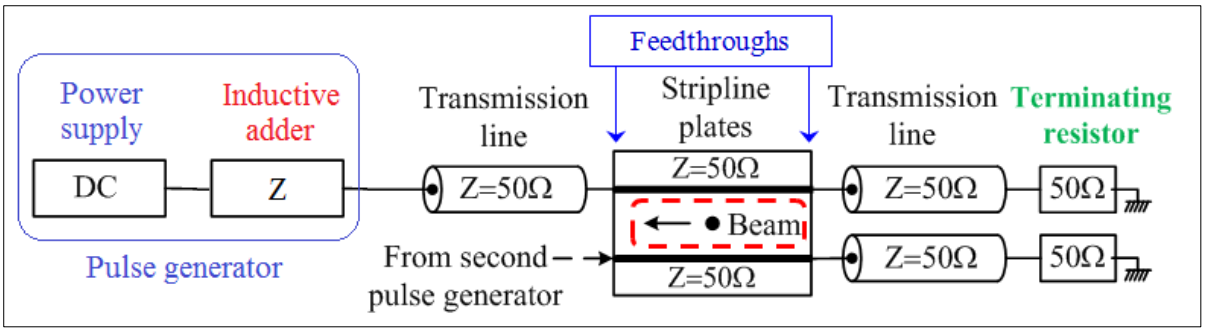

Figure 2: Stripline kicker system with an inductive adder.

The even-mode characteristic impedance should be ideally matched to the terminating resistor value of 50 Ω. When the striplines are pulsed to equal magnitude but opposite polarity voltages, the characteristic impedance of the kicker is odd-mode [3]. In the odd-mode, there is a virtual ground mid-way between the striplines and the characteristic impedance of each stripline is dependent upon the proximity of each stripline to both the beam pipe and the virtual ground. The even-mode characteristic impedance will be greater than the odd-mode characteristic impedance and it may not be feasible to match the odd-mode characteristic impedance of the striplines to the characteristic impedance of the other elements of the kicker system [3]. This means that the odd-mode characteristic impedance of the kicker, which is seen by the pulse generator, may not be matched to the terminating resistor and the generator.

Mismatched impedance causes reflections, which make the settling time of a voltage pulse longer. The simulation studies of the settling time with different rise times of the pulses are shown in Fig. 3. In this simulation, the pulse generator has been modelled as an ideal controlled voltage source. The delay of the pulse generator and the first transmission line has been modelled as a total of 10 ns, the

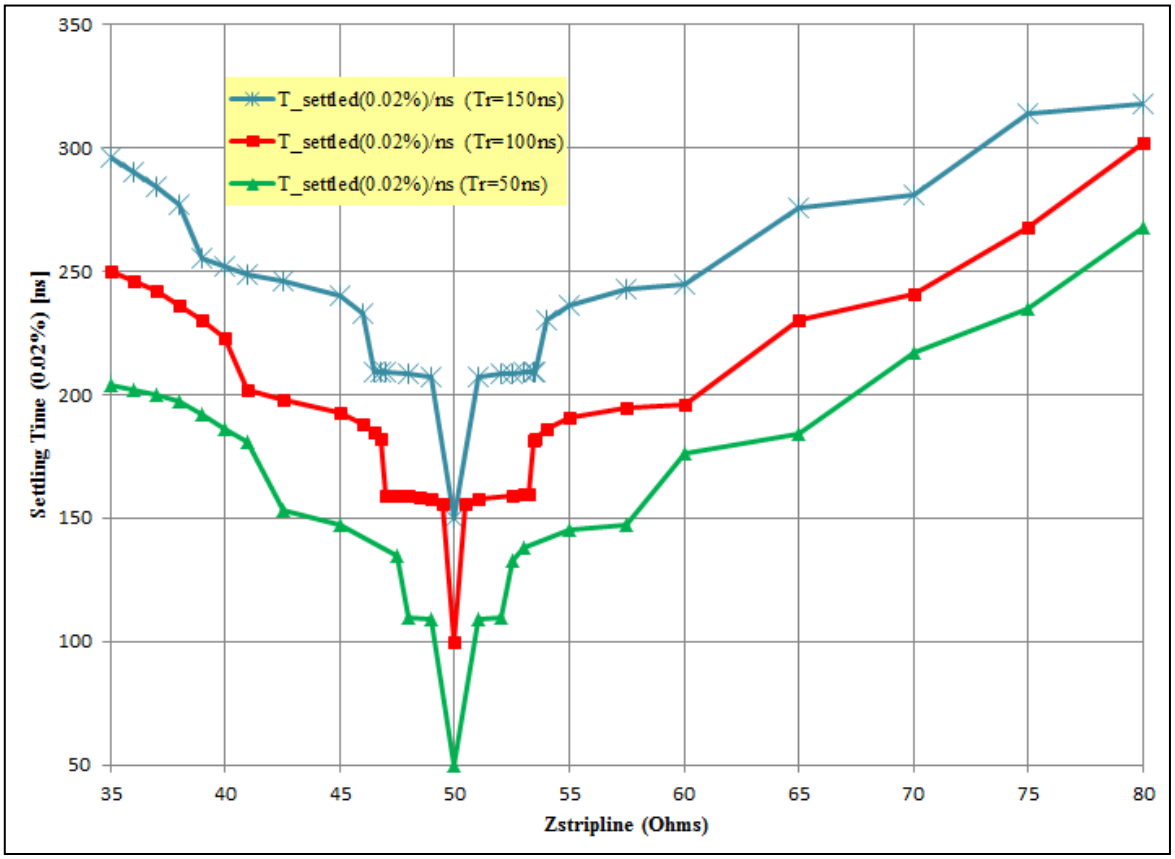

Figure 3: Settling time (to ±0.02 %) of the stripline voltage pulse as a function of stripline impedance with different pulse rise times T_r, for an inductive adder, transmission line and terminating resistor impedance of 50 Ω.

propagating delay of the stripline 10 ns and the load is 50 Ω. The transmission line between the stripline kicker and termination resistor has not been taken into consideration, and the pulse generator, the striplines and the transmission line are considered to be lossless. The simulations have been run using rise times (0 % to 100 %) of 50, 100 and approximately 150 ns for the voltage pulse. The allowed ripple was ±0.02 % of the pulse flat-top value. With 35 Ω of stripline kicker impedance, the settling time is 150 ns longer than with matched 50 Ω stripline kicker regardless of the rise time of the pulse. In reality, the losses of the transmission lines, striplines and the inductive adder may shorten the settling time. This will be verified by testing.

6. Literature Review

Bearing in mind the kicker system specifications and the requirements for reliability and machine protection, an extensive review of literature of existing pulse generators has been carried out to determine the best means of achieving the very demanding specifications for the pulse generator. The following conclusions have been reached:

- A pulse generator using a thyratron switch would not achieve the required reliability and redundancy.

- A Pulse Forming Line (PFL) would result in significant attenuation and dispersion of the pulse – this can be compensated with a suitable length of transmission cable [2]. The resulting droop is theoretically within specification, but there is no means of controlling ripple. In addition an impedance matched PFL needs to be charged to twice the load voltage.

- A double kicker system could be a good means of reducing ripple. However KEK achieved only a factor of 3.3 reduction in ripple [5], which is not sufficient for the CLIC DR extraction kicker.

- An Inductive Adder is a solid-state modulator capable of providing relatively short and precise pulses and with a proper design of the adder it may be possible to meet the ripple and droop requirements of the DR and PDR kickers [6-15]. The inductive adder is the most promising approach to meeting the specifications for the DR extraction system.

- A method to measure the output ripple of the pulse generator requires significant development. In the case that a direct electrical measurement of the 160 ns, 12.5 kV, flat-top pulse with accuracy better than ±0.02 % is not possible, the measurement may be required to be carried out at an accelerator facility with the prototype striplines [16].

Following the extensive literature review the inductive adder has been selected as a very promising means of achieving the specifications for the PDR and DR kickers and will be studied further.

7. The Concept of the Pulse Generator - The Inductive Adder

Fig. 4 shows a schematic of an inductive adder. The inductive adder consists of coaxial pulse transformers, the secondary windings of which are connected in series, while the primaries of which will be independent and each is referenced to ground: both primary and secondary windings will have a single turn. The inductive adder primary windings consists of stacked layers of printed circuit boards (Fig. 5), each of which will include capacitor banks, high power and fast solid-state switches with driver circuits and transient protection components.

Existing inductive adders have been used in applications with output voltages in the range from 15 kV to 500 kV, pulse widths from nanoseconds to microseconds and with ripple requirements from 1 % down to 0.2 % [8-11]: this is still an order of magnitude worse flat-top ripple than required for the CLIC DR extraction kickers. Digital and analogue methods, with sophisticated control schemes, may be used to modulate the output pulse waveform of the inductive adder [9, 12-15, 17]. This may

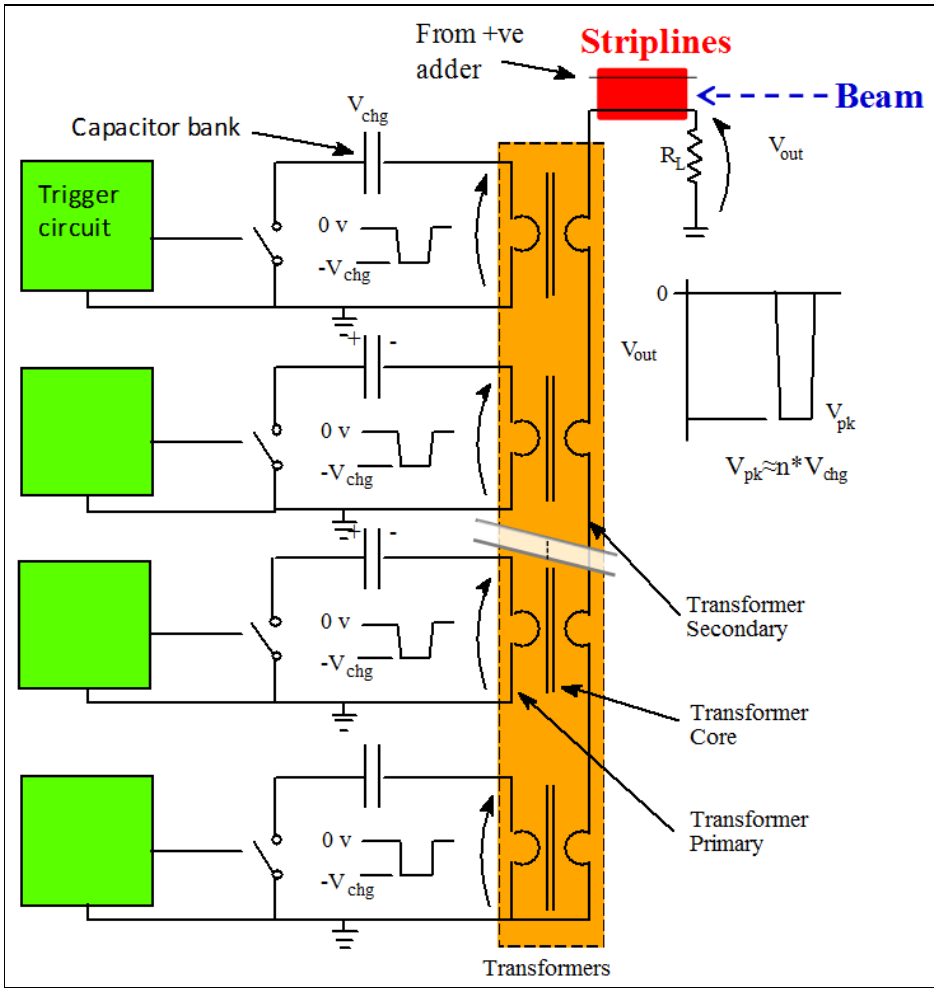

Figure 4: Schematic circuit of an inductive adder.

help to meet the demanding ripple requirements for CLIC, because the analogue modulation can potentially be used to cancel, for example, the voltage droop and ripple components of the output pulse [14, 15]. A suitably chosen relative gating time of the high power semiconductor switches may also be used to avoid resonances in the adder stack and thus reduce ripple. The use of analogue modulation will require selection and testing of suitable high-power and fast switching components and gate drivers.

7.1 Benefits of the Inductive Adder

Benefits of the inductive adder (IA) are the following:

- the IA uses solid-state switches, the control electronics of which can be referenced to ground;
- there are no electronics referenced directly to the high voltage output pulse;
- if one or more solid state switches of a layer of the inductive adder stack fails to switch, the adder still gives a significant proportion of the pulse magnitude;
- the same stack can be used to generate positive or negative pulses, depending on the grounding of the adder secondary winding;
- the source impedance of the adder is low and therefore, unlike a PFL, it does not require a significant increase in source voltage to obtain the output voltage;
- the same PCB and adder stack design can probably be used for both DR and PDR kickers.

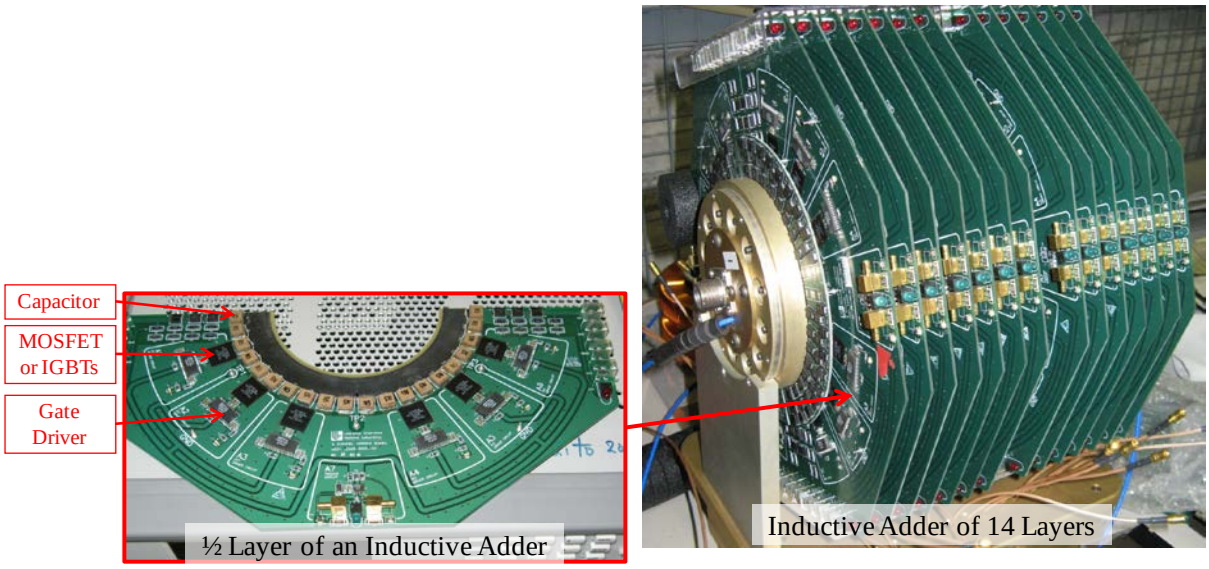

Figure 5: Photographs of an existing inductive adder at KEK.

7.2 Drawbacks of the Inductive Adder

A drawback of the inductive adder is that it is a rather complex device requiring many components – although this is good for machine protection (redundancy) – and each layer must switch full load current. In addition the fault currents may be very large. In general, the pulse width of the adder is limited by the saturation of the transformer core: however a 20 kV, 160 ns pulse is practical with a reasonable size of transformer. The layers of the inductive adder stack must be designed to have very small loop inductances and this may require custom-made capacitors. The minimum pulse rise time of the inductive adder is limited by the leakage inductance of the transformer units and the number of the primaries (layers) in the adder [18].

7.3 Costs and Size

The cost of the inductive adder scales approximately with voltage squared (for a 50 Ω load), because if the voltage is doubled, the number of layers are doubled, but each cell needs to provide double the current. This means twice the capacitance per layer and twice the number of semiconductor switches. The estimate for a 20 kV (50 Ω) inductive adder is 240 kCHF [4]. This includes the trigger system, power supplies, enclosure and personnel safety interlocks. A significant part of the costs is in the capacitors and switches: the transformers contribute less than 10 %. The inductive adder needs to be designed for the required load current, ripple and droop. The DR extraction kicker has the most demanding ripple requirements and this will require considerable research and development to achieve. It is presently proposed to design the prototype inductive adder to achieve the higher voltage isolation and current requirements of the PDR kicker: hence, by selecting the number of layers, the prototype will achieve the requirements of either the PDR or the DR kicker systems. The droop of the output pulse of the PDR generator will, however, likely be greater than that of the DR generator. For a 50 Hz repetition rate, the stack can be air-cooled and it would occupy approximately a half of a standard rack.

8. Specifications for Several Existing Applications of the Inductive Adder

The Advanced Radiograph Machine (ARM) at Lawrence Livermore National Laboratory (LLNL) was one of the first high power pulse generators built with solid-state switches [19]. ARM was designed to generate 45 kV and 5 kA pulses with voltage rise and fall times of 100 ns. The flat-top pulse width was adjustable from 200 ns to 1.5 µs and the repetition rate up to 2 MHz.

Another of the earliest inductive adder applications found in the literature was a solid-state kicker modulator for the Dual-Axis Radiographic Hydrodynamic Test Facility (DARHT-2), which was also designed and built at LLNL. The output voltage of the modulator was ±20 kV to the 50 Ω load, voltage rise and fall times were less than 10 ns from 10 % to 90 % of the pulse, the flat-top pulse

width was continuously adjustable from 16 ns to 200 ns and the maximum burst rate was four pulses with 600 ns between leading edges [8].

A DARHT II Fast dipole kicker modulator at LLNL was developed to provide 18-20 kV to a 50 Ω load with voltage rise and fall times of 10 ns from 10 % to 90 %. The flat-top pulse width is adjustable from 20 to 200 ns and the flat-top ripple is ±1 % [9]. An interesting feature of this device was the possibility to use analogue modulation to modulate the output pulse over 10 % of the output voltage range and with modulating frequencies up to the MHz range. This analogue modulation approach is being investigated for CLIC to determine whether it could be used to cancel droop of the capacitor voltages as well as ripple in the output of the pulse generator.

Another pulse generator developed at LLNL is the DARHT II Fast extraction kicker. It is designed for 50 kV output voltage [9]. The flat-top pulse width is 73 ns and pulse flatness specification is better than one percent. The rise and fall times are 64 ns from 0 to 100 %. The intra-pulse voltage ripple was required to be less than 300 V, which is 0.6 % of the maximum output voltage. To achieve this, digital amplitude modulation was used to cancel the droop of the capacitor voltages: some layers of the adder stack are charged to a fraction of the maximum voltage of other layers and switched on later than most of the layers to compensate droop. This approach will be investigated for the CLIC PDR and DR kickers.

Another example of applying digital modulation to manipulate the output of the inductive adder pulser is the conceptual design of a 4 kV, 40 A adder for the Muon Electron Conversion Experiment (MECO) at Brookhaven National Laboratory. The pulse rise and fall times are 20 ns, pulse flat-top 100 ns, pulse repetition rate 300 kHz and the output is a sinusoidal wave, modulated by 60 kHz. Therefore, the pulser gives five pulses per modulation frequency period. By charging each layer of the adder stack to different fractional voltages of the full voltage, to a maximum of half, a quarter or an eighth of full voltage, and so on, it is possible to achieve the desired output with the resolution, which is defined by the lowest charging level of a layer. By using 12 layers, the output voltage can be adjusted with the resolution of better than 0.5 % of the maximum output voltage [17].

The power modulator for LINAC klystrons at FNAL is based on the inductive adder but it has an auxiliary pulse transformer in the output. The output voltage is 320 kV and peak current 350 A. The output pulse width of the modulator is 4.5 μs and voltage rise and fall times less than 500 ns. The pulse to pulse reproducibility is below 0.2 % of the peak voltage and the flat-top ripple is specified to be less than 1 % of the peak voltage. In order to achieve this, droop of the output pulse caused by a finite value of capacitance is compensated by a passive R-L circuit [11].

One of the most recently published papers concerning applications of the inductive adder is the solid-state driver for the National Ignition Facility (NIF) at LLNL. This modulator consists of 27 layers, designed to operate at 750 V per layer, and the output voltage is 17 kV. The rise time is 20 ns and the fall time is in the same range but purposely held longer to avoid voltage transients in the overall system. The generator provides the ability to generate flat-top pulses with little droop, burst mode capability and continuously variable pulse spacing and pulse burst frequency agility [20].

To conclude, the inductive adder type solid state modulator has been used in many pulse generator applications. The required voltage ranges and pulse lengths of the PDR and DR kicker systems are moderate in comparison with existing applications. The ripple and droop requirements for CLIC are much tighter than for existing applications, however analogue modulation is a promising solution to keep ripple and droop within the demanding specifications for the CLIC PDR and DR kickers.

9. Components of the Inductive Adder

9.1 Capacitor Banks

The capacitor banks feed the primaries of the transformers when the switches are on. To directly keep the sum of droop and ripple below ±0.02 % requires a large value of capacitance on each layer of the adder. The absolute voltage droop of an individual layer in the adder stack, with N layers, is allowed to be (1/N)th of the allowed absolute voltage droop of the stack, because the total droop

and ripple in the output of the stack is summed over all the layers. To give an example for the DR kicker (±12.5 kV and 250 A):

- assume 18 modules with an operating voltage of 700 V per module (neglects redundancy);
- 280 A of current, which includes 30 A of magnetizing current for the transformer;
- 160 ns pulse width;
- 0.02 % of droop (which is assumed, here, not to be corrected by modulation etc.): this corresponds to a total droop of 2.5 V, which corresponds to a droop of 0.14 V per layer.

The capacitors need to have extremely low inductance [8, 9] especially to avoid excessive voltage transients during turn-off, due to energy stored in the parasitic loop inductance. This may require custom-made capacitors, in which several small capacitors are connected closely in parallel in the same package. The capacitors also need to be located close to the transformer primary.

The required capacitance, *C*, per layer for a given droop *ΔU per layer*, flat-top pulse length t_p and required current *I* can be calculated from the following equation:

$$C = \frac{It_p}{\Delta U} = \frac{280 \times 160e-9}{0.14} = 320\mu F \qquad (1)$$

From equation (1), the required capacitance to ensure a droop of no more than 0.14 V per layer, during the 160 ns flat-top, is 320 µF per layer. This could be achieved by using, for example, 27 pieces of 12 µF, 1 kV, capacitors in parallel per layer. However it may be impractical to fit the required amount of the capacitance on the PCB, therefore analogue modulation (see section 10. Modulation and Gating Schemes to Achieve Low Ripple and Droop) may be needed to compensate the voltage droop of the capacitors during the flat-top of the pulse.

9.2 Semiconductor switches

MOSFETs and IGBTs are used in the existing applications of the inductive adder. However, other components, for example IGCT, may also be applicable. The switch has to be capable of being switched off at full current to generate the falling edge of the pulse. Each layer of the adder stack must switch and conduct full load current, which may require several switches to be connected in parallel in each layer: however the parallel switches must have low time jitter. To compensate the droop of capacitor voltage, an analogue modulation layer may also be required. Modulation may also be used to compensate ripple. Operation over the linear region may be a very demanding specification for the semiconductor switch. The loop inductance of the primary circuits of the inductive adder must be very low to avoid excessive voltage transients turning turn-off, due to energy stored in parasitic loop inductance. Thus, the package of the switch and layout of the PCB need to be low inductance.

The advantages of MOSFETs in the inductive adder applications are that the switching transitions are very short in time, thus the repetition rate of the adder may be high and it is possible to generate short duration pulses. However, fast switching transitions, especially turning off load current, have the disadvantage that they can generate large voltage transients due to parasitic inductance (L.di/dt). The MOSFETs are also easy to control and they have low time jitter, usually in the order of sub-nanoseconds. The MOSFETs also have a long life potential, when properly utilized. The disadvantages of the MOSFETs are that they have, in general, a relatively low voltage rating (up to 1.2 kV) and low current devices (circa 150 A pulse at 1 kV rating), therefore parallel devices are needed for high currents. The low voltage rating may also require more layers in the adder than other switches with higher voltage ratings. As a result of its structure, the MOSFETs do not have a reverse blocking capability. Voltage induced failures are usually catastrophic; therefore snubber and clamping circuits are needed.

IGBTs have relatively fast switching transitions and they can be used with relatively high repetition rate, up to tens of kHz of switching frequency. For example, IRF and Fairchild produces IGBTs rated

for 1200 V with promising specifications: current rise time 41 ns and 22 ns, turn-off delay times 130 and 200 ns and current fall time 56 and 140 ns, respectively [21, 22]. IGBTs are also relatively easy to control and have a low time jitter. IGBTs are available with considerably higher maximum current and voltage ratings than MOSFETs. The disadvantages of the IGBTs are that, during the turn-off, there is a tail current which may take hundreds of nanoseconds to extinguish and turn-off delay time is often relatively long in comparison with rise and fall times. This excludes the use of the IGBTs for generating short duration pulses and in applications of very high repetition rate. As in the case of MOSFETs, a voltage induced failure is usually catastrophic for an IGBT and hence snubber circuits are needed to protect the switch. The IGBTs are available with ratings up to 600 A and 6.5 kV.

The selection of the semiconductor switch for the inductive adder requires a detailed study to identify suitable candidates and then testing in the laboratory. The operation in the linear region may be the most important feature, if analogue modulation is needed for controlling droop or reducing ripple in the output of the adder. The following MOSFETs have been used or tested in building a few kV to 20 kV inductive adders at LLNL: APT 1001RBVR [9], APT ARF449A [12] and APT ARF446 [12]. The latter two MOSFETs have been used with analogue modulation schemes. These components will be used as reference points in identifying suitable candidates for the inductive adder of the DR and PDR kickers.

A certain voltage margin needs to be reserved to protect the switching components against cosmic ray failures and transients. In the case of MOSFETs, about 70 % of the rated voltage range can be used, although a larger safety margin is advisable [23, 24]. For the current rating, the magnetizing current of the transformer needs to be taken into consideration. The load currents of the PDR and DR kickers are 340 A and 250 A, respectively. The magnetization current depends on the core material of the transformer, and based on the equations given in [25], it should be less than 10 % of the load current for the coaxial transformer unit of the inductive adder stack. Therefore each primary layer needs to be capable of feeding up to approximately 400 A of pulse current during normal operating conditions.

Analogue modulation techniques can be used to modulate the output voltage of the inductive adder and this may be necessary to keep output ripple to the desired level. The analogue amplitude modulation is explained in detail in the next chapter, but it is worth noting that applying this method requires switches which operate in their linear region. Fast power MOSFETs are available, for example from Microsemi and IXYS, which have been designed for linear region operation and, in addition, are built with a low inductance package. These linear switches are available with voltage ratings up to 1200 V, current ratings to tens of amperes and operating frequencies up to tens of MHz. Contradictory to that, IGBT manufacturers do not give specifications for linear operation. The current sharing inside a multi-die IGBT may be bad and as a consequence the die may overheat even with low currents, if used in the linear region [26].

9.3 Gate Drivers

In order to achieve fast rise and fall times of the drain-source current, gate drivers need to be able to provide sufficiently large current for rapidly charging and discharging the Miller capacitance. If analogue modulation is used to modulate the output of the adder, the gate driver circuit needs to have wide bandwidth for cancelling high frequency ripple components and an output voltage which is variable (i.e. not just low or high). The gate drivers of the switches are referenced to ground in each layer of the inductive adder.

9.4 Transformers

The transformers of the inductive adder must provide adequate insulation between the primary and secondary windings. The secondary windings of the transformers are connected in series whereas the primary windings are independent (Fig. 2). Both primary and secondary windings consist of a single turn to keep the bandwidth of the transformer high. With a coaxial design of the transformer and the adder stack, the high voltage is present only inside the adder structure and at the HV ends of the adder. Mechanical design of the transformer is similar to an induction accelerator cell and the secondary is usually a straight conducting rod (also known as a “stalk”) which goes axially through all the transformer layers. Each primary current drive must provide both the full load current and the

magnetization current of the transformer. Thus the magnetizing inductance should be as high as possible to minimize the magnetizing current.

The maximum output pulse-width of the inductive adder is limited by saturation of the transformer core. After each pulse, the core is typically reset to a negative remanence value, to utilise the maximum flux-density range of the core. Hence cores made of amorphous alloys or nanocrystalline material could allow flux-density swings up to 3 T. For ferrite cores, the maximum flux-density swing is only approximately 0.5 T. The cross-sectional area (CSA) of the magnetic core is computed from the pulse duration t_p and pulse voltage V_c divided by the maximum flux-density swing ΔB which can be used. Thus, the minimum CSA of the core can be approximately calculated with the following equation:

$$A_c = \frac{V_c t_p}{\Delta B} \qquad (2)$$

The larger the flux-density swing of the core, the smaller is the volume of the transformer. However, in addition to the CSA, the inside radius of the core must be large enough that the magnetic field does not saturate the inside of the core.

The parasitic leakage inductance of the transformer is desired to be as low as possible to avoid excessive voltage transients during turn-off, due to energy stored in the parasitic loop inductance. Hence, in the undesirable case of core saturation, the transformer primary is seen as a very low inductance by the circuit of the primary layers, which may cause very large fault currents and thus destroy the semiconductor switches. To avoid saturation, the core size has to be large enough for all operation conditions and a fairly large margin is used to ensure this: a margin, for example 100 % [27], is recommended to avoid the magnetic core becoming saturated during any normal operating or fault conditions.

The cores can be made of nanocrystalline or amorphous materials, manufactured from thin wound tape with suitable insulation between each turn. The selected core needs to have adequate insulation, which is suitable for the fast pulse applications, to avoid break down and large interlaminar eddy currents between adjacent turns. To give an example, Vacuumschmelze's Vitroperm F500 cores for EMC applications are tape-wound type and withstand typically only 0.3 V per turn and the thickness of one turn is about 20 µm [28]. In specific pulsed power cores, the interlaminar voltage stress may exceed 10 V per layer [29].

The interlaminar voltage, V_{il} , for non-magnetic interlaminar insulation (i.e. a material with constant relative permeability) is given by:

$$V_{il} = \left(\frac{A_{il}}{2 \cdot \pi \cdot r} \right) \cdot N \cdot \mu_0 \cdot \mu_r \cdot \frac{di}{dt} \qquad (3)$$

The derivation of this equation is shown in appendix [A]. In the above equation, μ_r is the relative permeability of the insulating gap between turns (for free space, µr equals to 1), N is the number of primary turns (for a single-turn transformer, N=1), di/dt is the rate of change of the current, A_{il} is the interlaminar cross-sectional area, and r is the radius of interest.

From equation (3), using 20 ns as the pulse current rise time, 7 µm thickness of insulation between turns (resulting in a packing factor of 75 % [26]), 2.5 cm core height, 400 A primary current and 1 cm radius r, the computed induced voltage is 0.07 V/layer. The interlayer voltage insulation of cores can be increased by impregnating the cores with oil under vacuum [28], but this is not a desirable solution [28].

Under fault conditions, if the core were to saturate, and assuming a primary leakage inductance of 20 nH [18] per layer, the primary di/dt would be approximately 35 A/ns (700 V/20 nH). The corresponding interlaminar voltage, assuming the same core parameters as utilized above, would be approximately 0.14 V (in comparison with 0.07 V during normal operation).

To give an example of the transformer core design, the dimension for the core of the DR kicker pulser can be computed for the following values:

V_c = 700 V (switches with 1 kV ratings used).

t_p = 750 ns + 150 ns = 900 ns (assumes equal and linear rise and fall times of 150 ns, and a worst-case pulse width of 750 ns. The large pulse width is chosen to ensure that ripple, resulting from impedance mismatches, is fully damped).

Hence, the integral $\int V_c \cdot dt$ gives 6.3 x 10^{-4} V·s as the required volt-second product.

ΔB = 1.4 T is considered to be a reasonable value. For example, the saturation flux density B_s, for the core material 2605SA1 is known to be 1.56 T and the remanence value 1.2 T [30]. However the full 2.76 T swing, from the negative remanence to the positive saturation, cannot be used as it is recommended to remain within the linear region of the B-H curve of the transformer core, to avoid non-linearities which will be more difficult to compensate for. In addition the core should be chosen such that temperature variations do not result in non-linear B-H characteristics, over the complete B-H curve working range. An annealed core with square-loop magnetizing characteristics will have the lowest leakage inductance [27]. A reset circuit, either passive or active, is needed to force the magnetic flux of the transformer cores to a negative value after the pulse, to allow to use both the negative and the positive side of the flux swing.

With these values, the effective cross-sectional size of a solid core should be at least 9 cm^2 per layer (this includes a 100 % margin). The packing factor of the insulation must also be allowed for when the cross-sectional area of the core is chosen. Assuming a packing factor of 70 % for the magnetic core, the cross-sectional area of the core should be at least 12.9 cm^2. The cross-sectional area of the core increases linearly as a function of total pulse width, which includes the pulse rise and fall times. The pulse length has been assumed to be 750 ns instead of 160 ns flat-top pulse width, because depending on impedance matching of the pulse generator and the striplines, some excess time may be required to damp reflected pulse components down to the acceptable value. The required damping time may be up to 500 ns, if the impedance of the kicker is 30 Ω, which is considered as the worst case situation.

9.5 Snubber and Clamping Circuits

A diode clamping snubber, in parallel with the power MOSFET (Fig. 6), can be used to protect each semiconductor switch of the primary circuits against voltage transients. In addition a fast diode clamp is needed in parallel with the transformer primary to provide a free-wheeling path for the transformer magnetization current, following turn-off of the power semiconductor switch (Fig. 6). The fast diode clamp is also needed in the case when a single layer fails to switch on in the adder stack. In that case, the secondary current induces current in the primary winding of this layer, which needs a path to avoid failures for the components. The behaviour of the fast diode clamp determines the voltage over that layer in which the switching failure occurred.

10. Modulation and Gating Schemes to Achieve Low Ripple and Droop

10.1 Digital Modulation

Digital modulation techniques can be applied to modulate the output pulse of an inductive adder. Individual layers of the adder stack can be pre-charged to a suitable fraction of the maximum voltage and the layers switched on and off at different times [9]. Digital modulation is applied by controlling the output voltage of the power supplies, which charges the capacitors banks of the individual layers to a desired level, and gating times of the semiconductor switches. It does not require any modifications to the basic cell structure or layout, as can be seen in Fig. 6. Digital modulation scheme may not be applicable to reduce ripple in the case of DR and PDR kicker pulse generators, because the permissible ripple range is only a few volts in total, but the technique will be investigated further.

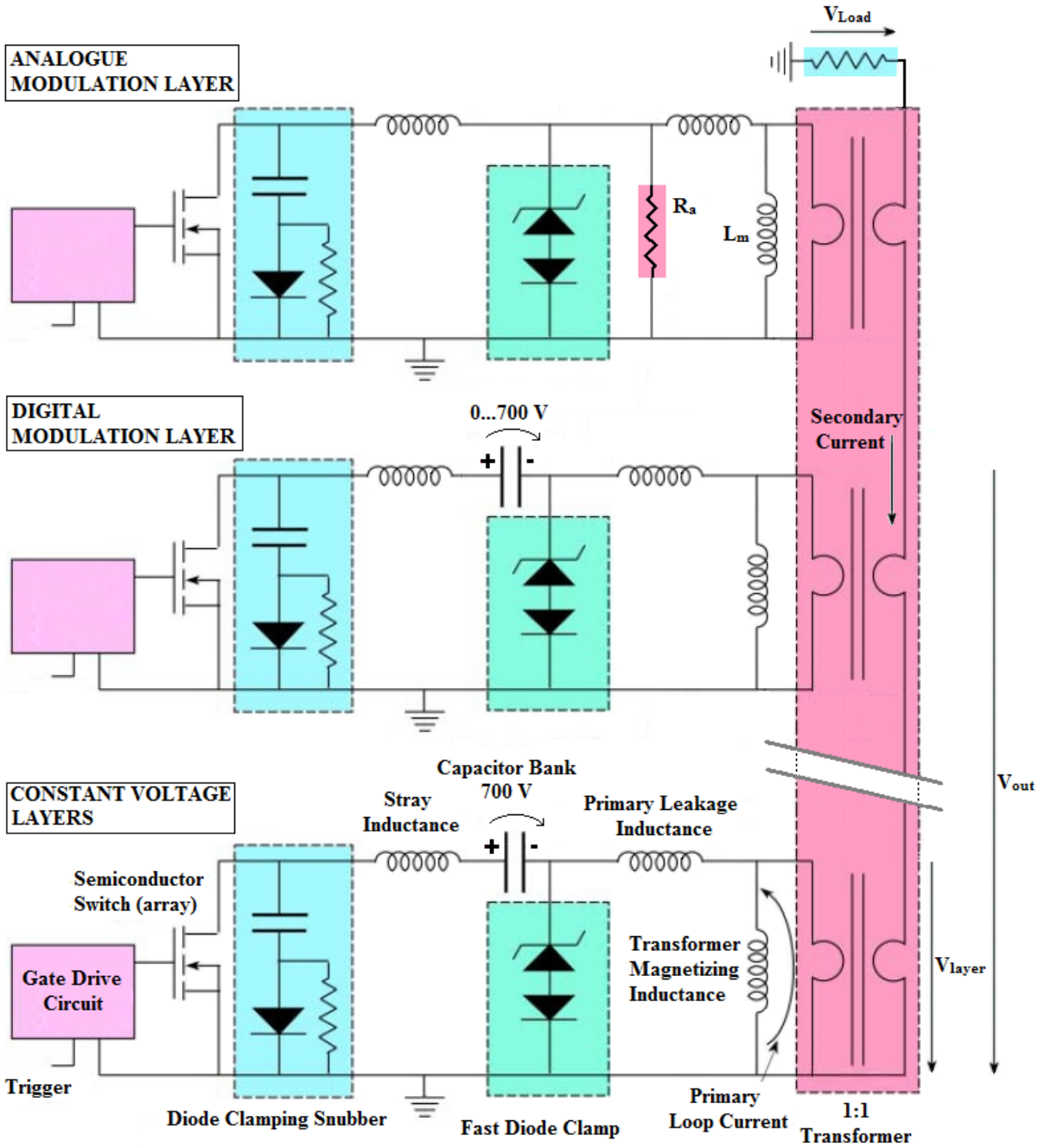

Figure 6: Schematic of inductive adder layers with a snubber and a diode clamp. Revised after [9].

10.2 Analogue Modulation

The output pulse of an inductive adder can be modulated using analogue modulation technique. This requires that there are layers in the adder in which the switches operate in the linear region instead of being switched on or off completely. When operating in the linear region, the output of the switches can be controlled and therefore the output of the adder can be modulated. A ramp type (analogue) modulation may be needed to compensate droop of the capacitor banks. Analogue modulation may also be needed to cancel known or predicted ripple components. Applying analogue modulation to the adder requires extensive testing of the semiconductor switches together with gate drivers. In addition a detailed understanding of the transient circuit response is required: circuit simulations, using PSpice, are being carried out.

The analogue modulation layer shown in Fig. 6, differs in two ways from a “constant voltage” layer. In the analogue modulation layer, the capacitor bank is not needed, however, there is a low valued resistance (R_a) connected in parallel with the transformer primary.

10.3 Passive Analogue Modulation

During the output pulse, resistor R_a is effectively in series with both the load resistor and the secondary winding of the adder. Therefore, the load voltage, V_{load}, is given by the following equation:

$$V_{load} = \frac{R_{load}}{R_a + R_{load}} V_{out} \qquad (4)$$

where V_{out} is the sum of the output voltages of the other layers. If there is no modulation, the load voltage V_{load} during the pulse is smaller than without the modulating layer.

Simulations were carried out with a 5-cell inductive adder model, using different capacitor values and the analogue layer as a passive and an active compensator. There were four constant voltage layers supplying 700 V each, one analogue modulating layer and an 11.2 Ω load. The circuit analysis showed that the analogue modulation layer behaves as an R-L circuit in the passive mode. The current through resistor Ra decreases during the pulse as current transfers into the magnetizing inductance, which causes the voltage over the resistor Ra to decrease. The ratio of the magnetizing inductance of the transformer primary to the resistance Ra can be defined to provide the desired time constant for the voltage decrease across R_a and thus compensate the voltage droop across the capacitors in the other layers. In reality, the magnetizing inductance should be as large as possible to minimize magnetizing current: in addition R_a cannot be very large to avoid excessive power loss.

The simulation results are shown in Fig. 7: with a well-chosen ratio of magnetizing inductance value to resistance R_a, the droop of the load pulse can be reduced to within specification. In addition the capacitance per layer can be reduced significantly without causing excessive droop in the load voltage. However a passive layer does not allow the possibility of compensating for long-term effects.

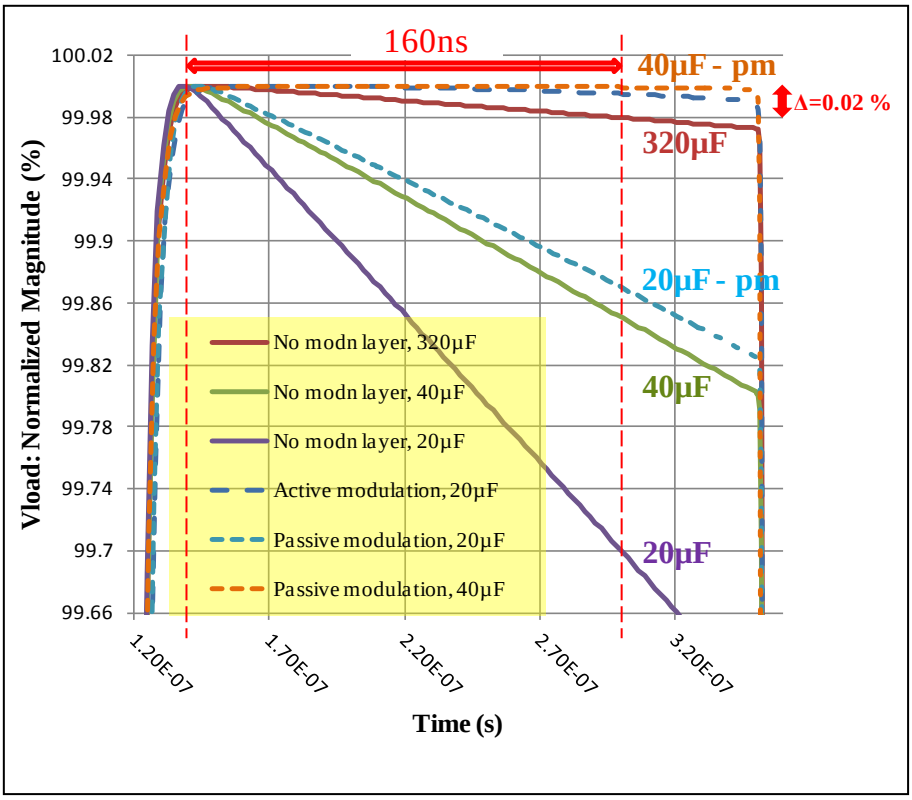

Figure 7: The simulated normalized output voltage of an inductive adder with different capacitor bank values: with passive modulation (pm), with active modulation and without modulation.

10.4 Active Analogue Modulation

The semiconductor switch in the analogue modulation layer provides a shunt path for the current, which flows through the parallel resistor R_a. If the switch is conducting, a share of the current flows through it and thus the voltage over the parallel resistor R_a is decreased. This means that the load voltage is increased with respect to not having active modulation. By choosing the parallel resistor value suitably, it is possible to control the output voltage with a relatively small share of the current flowing in the active switch. With an active analogue modulation scheme, the modulating frequency can be tens of MHz and the amplitude can be modulated more than 10 % of the maximum flat-top pulse voltage [12]. The modulation bandwidth is limited by the cut-off frequency of the LR-type low-pass filter which is given approximately by the inductance of the adder stack and the resistance $R_{load}/(R_{load}+R_a)$.

In fig. 7, the simulation results of the inductive adder with and without analogue modulation are presented. In these simulations, the voltage of each constant voltage layer was 700 V and the load current 250 A. The red, green and dashed purple curves show the normalized load voltage of an inductive adder without an analogue modulating layer. These three curves, with 20 µF, 40 µF and 320 µF, show the voltage droop of the capacitors, as seen in the load voltage. The red curve, simulated with 320 µF of capacitance, has 0.02 % of droop, which fulfils the CLIC DR kicker requirements.

With 20 and 40 µF of capacitance per layer, without modulation, the voltage droop across the load (0.4 % and 0.2 %, respectively) is significantly larger than with 320 µF. The dashed light blue curve shows the load voltage of the adder for 20 µF of capacitance per layer and the analogue modulating layer being used as a passive RL-circuit. In this simulation, the modulating semiconductor switch, which provides a shunt path for the current flowing through resistor R_a in the analogue modulating layer, was switched off completely. The droop is significantly smaller than in comparison with 20 µF of capacitance without a compensating layer, but more than nine times larger than desired. The upper dashed dark blue curve shows the load voltage of the inductive adder with 20 µF of capacitance and with the modulating layer actively compensating the voltage droop. In this simulation, the linear switch in the analogue modulating layer was controlled and the current through the switch was modulated with a ramp modulation. The droop in the load voltage is less than 0.02 %, despite that the capacitance per layer being only 20 µF: this is one sixteenth of 320 µF, the amount of capacitance which is required to meet the 0.02 % droop specifications without the analogue modulating layer. The maximum predicted current through the shunt switch is less than 2 % of the load current. Without an analogue layer, the droop of the load voltage with 20 µF of capacitance per layer was ~0.4 % and with a passive analogue modulation layer it was ~0.2 %. In these simulations, resistance Ra was 1.2 Ω and the magnetizing inductance of the analogue modulation layer 13.1 µH. The time constant, L/R, of the analogue modulation layer was 10.9 µs. This corresponds to 1.46 % of current change through the resistor R_a in 160 ns. Therefore, the maximum current through the magnetizing inductance Lm at the end of the pulse is 3.28 A. With the active analogue modulation and 20 µF capacitors, the peak power dissipation of the analogue switch was 1.15 kW and the average power dissipation for 50 Hz repetition frequency was 7 mW. For resistor R_a, the power dissipation was 60.2 kW (peak) and 700 mW (average for 50 Hz). With passive analogue modulation and 40 µF of capacitance per layer, the power dissipation in the resistor was 60.5 kW (peak) and 710 mW (average for 50 Hz). The pulse width in these simulations was 250 ns and the rise time (from 10 % to 90 %) of the output pulse was 8.5 ns. Resistor R_a and the linear switch can be implemented using several parallel components to reduce the power dissipation per device, in comparison with a single device.

10.5 Gating Schemes, Ripple and Droop

Carefully chosen relative gating time of the semiconductor switches could be used to avoid resonances in the adder stack. The relative timing of layers could be delayed by the time corresponding to a half wave length of the most significant resonance frequency. This might damp resonances quickly. A feed-forward compensation may also be needed to cancel predefined ripple components, for example predictable slow variations of the system. This requires detailed simulation studies.

11. Design of an Inductive Adder Cell

11.1 Dimensioning of the Cell

In Fig. 8 below, a generalized equivalent circuit for a single cell (a) and for the N cell inductive adder (b) are presented [25]. In fig. 9, an illustration of the inductive adder cell is shown. The primary leakage inductance L_{kp} is very small, because of the single turn primary, i.e. relatively short electrical length and large cross-sectional area of conducting path. The primary resistance R_p may also be small, if the primary encloses the core, i.e. is a relatively short length. The parasitic elements in the secondary, which are secondary leakage inductance L_{ks}, secondary resistance R_s and coupling capacitance C_c between primary and secondary, are dominated by the stalk. The secondary leakage inductance, L_{ks}, per layer is given by:

$$L_{ks} = \frac{\mu_0 l_p}{2\pi} \ln \frac{D_2}{d} \quad \textbf{[25]} \qquad (5)$$

in which l_p is the length of the adder layer, D_2 is the inner diameter of the magnetic core, d is the outer diameter of the stalk and μ_0 is the permeability of free space. The secondary resistance R_s is the stalk resistance per cell length l_p. L_{ks} corresponds to the distributed inductance of the stalk per stack section length [31, 32].

The coupling capacitance, C_c, is given by the following equation [25]:

$$C_c = \frac{2\pi\varepsilon_i l_p}{\ln \frac{D_1}{d}} \qquad (6)$$

In this equation ε_i is the produce of the relative permittivity and the permittivity of free space of the insulation between the magnetic core and the secondary stalk. C_c corresponds to distributed capacitance of the stalk per stack section length [31, 32].

The primary inductance L_m is given by the following equation [25]:

$$L_m = \frac{\mu_c l_c}{2\pi} \ln \frac{D_3}{D_2} \qquad (7)$$

where μ_c is the permeability of the magnetic core, l_c is the height of the core and D_3 is the outer diameter of the magnetic core.

An important step in the design of the inductive adder cell is dimensioning the magnetic core. The cross-section of the core depends on the selected core material. The core must provide the required volt-seconds for the pulse time so that the transformer is never driven into saturation (see section 9. Components of the Inductive Adder). The insulation requirements of the stalk, which depend on the output voltage, sets the minimum core inner diameter: this is shown as D_2 in Fig. 9.

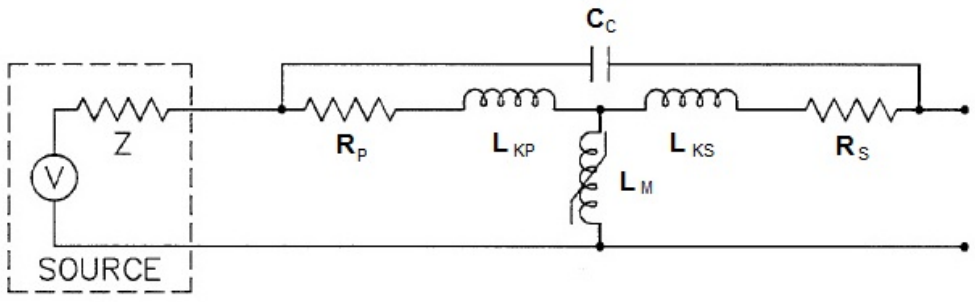

Figure 8: Equivalent circuit of a single layer inductive adder. Revised after [25].

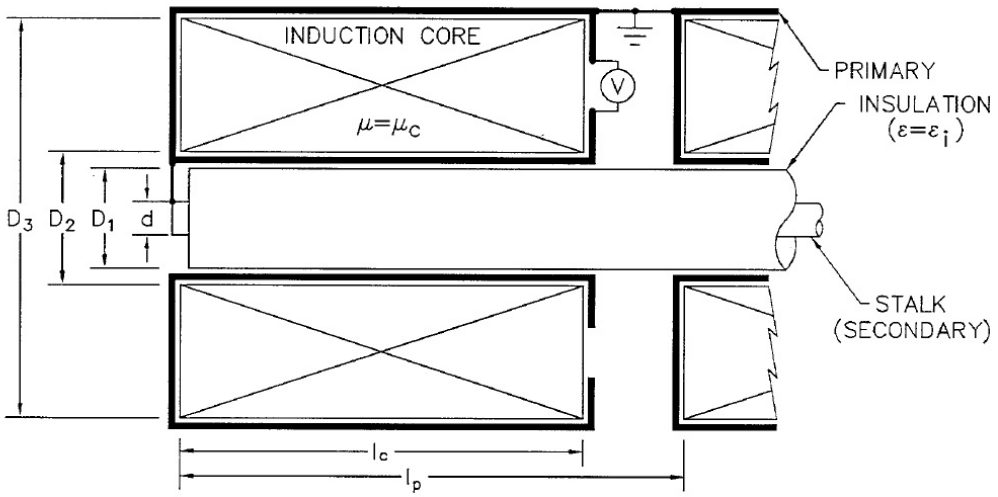

Figure 9: Illustration of an inductive adder cell [25].

The outer diameter D_3 and the length of the core l_c are adjusted to satisfy the following equation:

$$A_c = l_c(D_3 - D_2) \quad (8)$$

in which A_c is the required cross-sectional area of the magnetic core of one layer. The secondary leakage inductance scales with the core length as does the primary inductance [25]. The parasitic coupling capacitance (eqn. 5) can be reduced by decreasing the diameter of the stalk, *d*, but this increases the secondary leakage inductance L_{ks} (eqn. 5).

11.2 Features of the Adder Stack

The output voltage of the inductive adder is the sum of the output voltages of the individual layers,

$$V_{out} = NV_{layer} \quad (9)$$

in which *N* is the number of the layers and V_{layer} is the voltage of an individual layer: in this equation, it is assumed that every single layer is charged to the same voltage before switching on. The adder stack can be used as a bipolar or single-ended voltage source. The pulses produced by each layer will propagate bi-directionally and add up at the load. If the inductive adder is used as a bipolar source and is terminated at both ends with matched impedance loads, the pulse rise time of each output is the one-way propagation time of a TEM pulse through a layer multiplied by the number of the layers [33].

The electrical propagating delay through the secondary of the inductive adder can be computed from the following equation [31]

$$T_{rd} = N\sqrt{(L_{kp} + L_1)C_1} \quad (10)$$

In which L_{kp} is the primary leakage inductance, L_1 is the secondary leakage inductance per cell, corresponds to L_{ks} in eqn. 5, and C_1 is the distributed capacitance per cell length (which corresponds to coupling capacitance C_c shown in eqn. 6).

The electrical propagation delay time of a single-ended adder stack, with a matched impedance load and a direct connection to ground on the other end, is the two-way propagation time of the TEM pulse from the top of the stack to the bottom and back [33]. This can be written as [31]

$$T_{rd} = 2N\sqrt{(L_{kp} + L_1)C_1} = 2N\sqrt{(L_{kp} + L_{ks})C_c} \quad (11)$$

The output impedance of the stack has to be matched to the load to avoid reflections and to keep the electrical propagation delay short. The output impedance depends on the stalk impedance and leakage inductance of the transformer, namely [31]

$$Z_{out} = \sqrt{\frac{L_{kp} + L_1}{C_1}} = \sqrt{\frac{L_{kp} + L_{ks}}{C_c}} \qquad (12)$$

The above parameters can be computed from the stalk dimensions and layer dimensions and material parameters, as shown below. Primary leakage inductance L_{kp} has a large effect on the output impedance, which was shown in [31] and [18]. In the first design step in [18] and [31], L_{kp} was mistakenly neglected, in which case the output impedance Z_{out} was calculated as L_1 divided by C_1, and for given values of L_1 (corresponding to L_{ks}) = 6.5 nH and C1 (C_c) = 2.6 pF it corresponded to 50 Ω [32]. By taking primary leakage inductance L_{kp} into consideration and computing the output impedance with a given value of 20 nH, which still is quite small, the stalk impedance is 101 Ω [31]. Therefore, the primary leakage inductance has to be taken into consideration in defining the dimensions of the stalk structure and layer length, to match the output impedance to the load.

11.3 Design Steps

The design of the dimensions of the inductive adder is an iterative process. The process can be carried out as follows:

- choose the type of semiconductor switches, their voltage rating and operation voltage;
- calculate the number of primary layers, including redundancy;
- estimate the value of capacitance per layer;
- determine the minimum CSA or the magnetic core, including a suitable safety margin;
- determine the dimensions of the coaxial transformer structure.

The first four steps have been described in detail above. Dimensioning the coaxial transformer structure is an iterative design process in itself and all the other design steps affect it. Primary capacitors need to be located very close to the primary winding to keep the loop inductance low. If a large value of capacitance is required per layer, the outer diameter of the transformer core can be selected to fit the primary capacitors in a circle around it. The storage capacitors can be quite bulky in comparison with the other components in the primary circuit, therefore the minimum height of one layer is defined by the height of the primary capacitors.

The space between the primary and secondary windings is filled with dielectric material to provide sufficient insulation between the high voltage secondary and the low voltage primary circuits. The outer and inner diameters of the dielectric are set by the insulation requirements of the output. Below 20 kV, air insulation may be sufficient [34]. The outer diameter of the secondary conductor is calculated based on equations of the inductance and capacitance of a coaxial transformer. The value of leakage inductance of the primary winding may not be computed exactly at this point, hence dimensioning of the adder stack may require several iterative steps. The primary leakage inductance effects on the output impedance of the adder stack, which is desired to be matched to the load. One iterative round of designing the coaxial transformer structure for the inductive adder is shown in appendix [B].

Fig. 10 below shows the cross-section of the three-dimensional model of a single layer of the inductive adder stack for the CLIC damping rings. The model has been built to design the mechanical structure of the adder stack and to visualize the dimensions, parts and assembly of the stack. The single circuit elements located on the printed circuit board are not shown. The primary circuit,

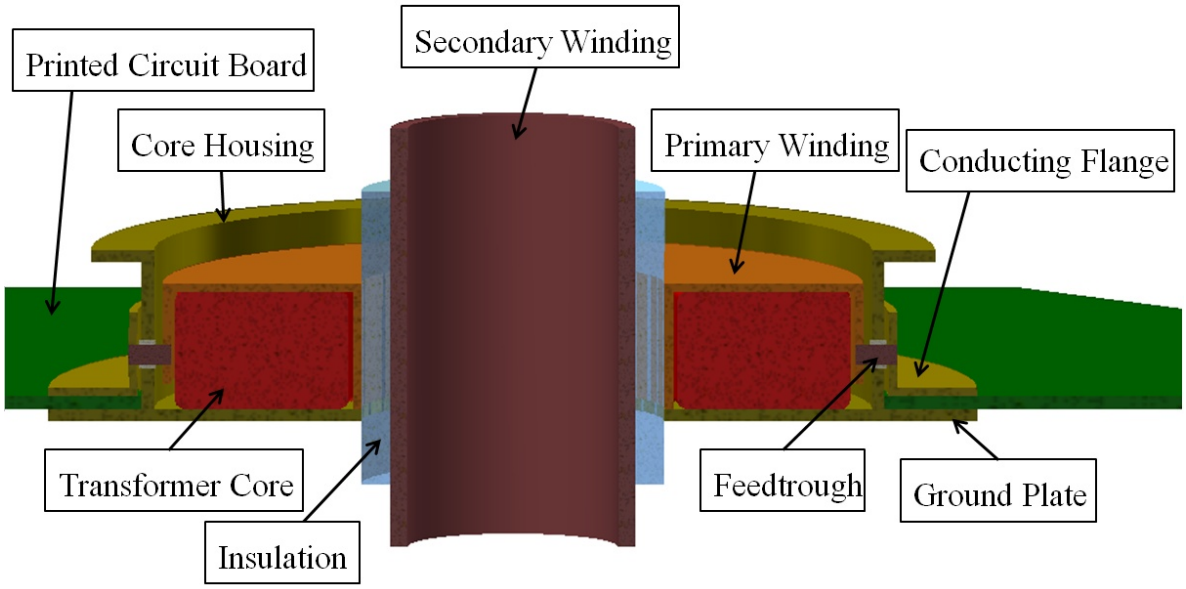

Figure 10: Cross-section of a single layer of the inductive adder stack.

consisting of the primary capacitors, switches, snubbers and fast diode clamps, is connected to the primary winding via a conducting flange, which provides a low inductance current path from the upper side of the printed circuit board to the primary winding. There are several feedthroughs in the flange which connects it to the primary winding. Two of these feedthroughs are shown. The primary winding is made of metal "foil" which surrounds the transformer core with a single turn. The secondary winding is a metal rod, which passes through all the transformer cores of the adder stack. Insulation is also shown; it may be an air gap or made of dielectric material. The ground plate, which is on the lower side of the transformer core, provides the return path for the primary current to the bottom side of the printed circuit board and it is connected to the ground potential. The core housing is a made of metal and it is a base support structure of the adder stack. It is also connected to ground potential, and its upper side can be fastened to the ground plate of a preceding layer by screws.

12. Circuit Simulations

Extensive circuit simulations are needed to design the inductive adder. The dimensions of the adder cell have an effect upon the electrical quantities of the transformer and therefore different options need to be compared. The transient effects on the circuit need to be simulated to design the clamping and snubber circuits required to protect the switches. The value of components may be investigated with simulations to ensure the desired behaviour of the adder circuit. Analogue modulation may be needed to cancel ripple and droop components of the output pulse of the adder. This requires simulations to set specifications for the switches as well as the gate drivers.

13. Challenges and Issues

There are two very challenging issues which need to be studied in detail to test the inductive adder in the laboratory. The first concerns measuring the output pulse flat-top with better than ±0.02 % of relative accuracy. It is not obvious that this could be done using a direct electrical method. The current transformers can be found with the following specifications [35]: maximum peak current 10 kA, droop 0.002 %/µs, rise time 7 ns and 3 dB cut-off frequency 50 MHz. These specifications are good enough, but the required accuracy of the measurement is far greater than the precision of available oscilloscopes (typically ±1 %). Along with precision requirement, the problem arises from the short pulse width, 160 ns, because this is in the same order as the settling time of the measuring preamplifiers [36].

A method to measure the ripple of the pulse generator could be to test it together with the striplines. The kicker would be followed by a static dipole magnet, with a high stability DC power supply, which deflects the beam equally but in the opposite direction to the kicker [37]. The fluctuations seen in the beam after the second kick are caused by ripple of the pulse source. However, this requires machine time in an accelerator facility and a specific set-up for the beam line.

13.1 Analogue Modulation Circuit

Another challenge will be to get the gate drivers and switches to work together so precisely that the droop caused by the capacitors and possible ripple components can be compensated, by modulation, to be smaller than ±0.02 % of the pulse value. This will require extensive simulations and testing. Individual semiconductor switches and gate drivers might be tested by "controlled" ramping of current at low drain-source voltage.

The mechanical structure of the adder is similar to that of an induction accelerator cell. The dimensions of the adder are critical to achieve the desired low ripple. The mechanical design of the adder stack as well as PCB design will also be of great importance in achieving relatively short rise and fall times for the output pulse. Matching of the output of the adder to the load needs to be very good to minimize reflections and this may require custom-made output connectors. In addition interconnecting coaxial cables need to be of relatively short electrical delay, so that ripple introduced by mismatches is rapidly damped.

14. Required Testing

The switch and the gate drivers need to be tested to verify their performance, i.e. pulse shape and repeatability, bandwidth of the gate driver and modulation capability. The on-state resistance in the saturation and linear regions might be the most demanding specification for the switch. Tests need to be carried out to identify a selection of candidate switches. The features of the magnetic core need also to be measured, for example remanence value, temperature stability, linearity of the B-H characteristics, and their suitability for pulse power applications. Verification of the low inductance of capacitor banks will also require testing because this is very important for the desired functionality of the adder.

15. Conclusion and Schedule

The inductive adder is the most promising solution for meeting the strict ripple and droop requirements for the pulse generator of the DR and PDR kickers for CLIC. Simulation and preliminary design of the inductive adder is planned to be finished by the mid of 2012. Selection of the components and also testing of switches in the linear and saturation region will be completed during the first half of 2012 so that long delivery time items can be ordered. A prototype of the inductive adder consisting of two or three layers is planned to be ready by the end of 2012. The first full prototype of the inductive adder is presently planned to be ready by the end of 2013.

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Appendix A:

Derivation of the equation for the interlaminar voltage stress in tape-wound magnetic cores

From Faraday's law, the interlaminar voltage, V_{il} , is equal to the rate of change of flux, $d\phi/dt$, between laminations:

$$V_{il} = \frac{d\phi}{dt} .$$

Using

$$\phi = B \cdot A_{il}$$

where B is flux density (T) and A_{il} is the interlaminar cross-sectional area.

Thus:

$$\frac{d\phi}{dt} = A_{il} \cdot \frac{dB}{dt}$$

Substituting

$$B = \mu_0 \mu_r H$$

$$V_{il} = A_{il} \cdot \frac{d(\mu_0 \cdot \mu_r \cdot H)}{dt}$$

where μ_0 is the permeability of free space, μ_r is the relative permeability of the intelaminar insulation between turns, H is the magnetic field strength, and r is the radius of interest.

Substituting

$$H = \left({Ni}/{l} \right)$$

where N is the number of turns (for a single-turn transformer, N=1), and i is the current:

$$V_{il} = \frac{A_{il}}{l} \cdot N \cdot \mu_0 \cdot \left(\frac{d\left(i \cdot \mu_r\right)}{dt} \right)$$

For a toroidal core, the magnetic path length of interest, $l = 2\pi r$, where r is the radius of interest. Hence, in the general case for a toroidal core:

$$V_{il} = \frac{A_{il}}{2 \cdot \pi \cdot r} \cdot N \cdot \mu_0 \cdot \left(i \cdot \frac{d\mu_r}{dt} + \mu_r \cdot \frac{di}{dt} \right)$$

For the case where the interlaminar insulation has a constant relative permeability, i.e.

$$\frac{d\mu_r}{dt} = 0$$

the preceding equation can be simplified as follows:

$$V_{il} = \left(\frac{A_{il}}{2 \cdot \pi \cdot r} \right) \cdot N \cdot \mu_0 \cdot \mu_r \cdot \frac{di}{dt}$$

Appendix B:

Design steps for the coaxial transformer structure of an inductive adder

1. The height of a single layer is defined by either the height of the storage capacitors or the height of the transformer cores. Let the height of a pulse capacitor be 3.2 cm [38]. This gives the limiting height, to which it is needed to add a few millimetres for the printed circuit board (say 3 mm) and air gap between the components on a layer and the neighbouring layer of the stack. Thus, the height of a cell, l_p, is at least 4 cm. This means that the height of the transformer core needs to be less than 4 cm, to reserve some space for the primary winding, which encases the core, and an air gap between the winding and the next transformer core in the stack.

2. The minimum outer diameter of the coaxial transformer structure is defined by the size and number of the capacitors, so that the printed circuit board can house them. Assume 12 pieces of 3 cm wide capacitors, which are placed on a circle with a circumference of at least 36 cm. Having some space between the primary circuit branches, a suitable outer diameter D_3 for the core could be as large as 160 mm.

3. The maximum inner diameter of the transformer core is defined by the required flux-density, the height of the single layer and the cross-sectional size of the transformer core. Let's assume that the required effective cross-sectional size for the core is 9 cm^2 (see section 9.4 Transformers) and the height of the core l_c is 25.4 mm, which is a typical size for an off-the-shelf core. Using 65 % of package factor would give 12.9 cm^2 for the size of the core, but the package factor may be even smaller with the pulse cores. Taking in the consideration 160 mm of outer diameter of the core, these values define the inner diameter D_2 to be 105.5 mm as maximum. Tape wound cores are wounded around a mandrel, which in this case could be 80 mm of diameter. Therefore, the dimensions of the core are 160 mm as outer diameter, 80 mm as inner diameter and 25.4 mm as height.

4. The primary winding encloses the transformer core completely. Thus, its thickness limits the outer diameter of the dielectric, which is located between the transformer core and the secondary winding, i. e. the "stalk". The thickness of the primary winding is expected to be 2 mm, which gives 7.60 cm for the outer diameter D_1 of the dielectric.

5. The last two parameters to define are the diameter *d* of the rod or "stalk" of the secondary winding and relatively permittivity ε of the dielectric material, which fills the gap between the primary and secondary windings. These parameters, and the height of the cell, can be modified to get the output impedance to be matched for the load impedance. At first, assume air insulation, in which case the permittivity of the dielectric is 1.0. Having several parameters to play with, the convenient way to compare the effects of parameters is to fill in a spreadsheet and try to find a good combination, which gives feasible values for the missing parameters. As a first guess, the diameter of the stalk is chosen to be 5.90 cm. Using equations which are shown in chapter "Design of an Inductive Adder Cell", the values for the following parameters can be found: secondary leakage inductance L_{ks} is 2.44 nH and coupling capacitance C_c is 8.79 pF. Primary leakage inductance L_{kp} is estimated to be 20 nH. The output impedance can be computed from these values and it ends to be 50.5 Ω. However, in this case the insulation thickness (D1-d)/2 between the primary winding and the stalk is only 8.5 mm. This may not be enough if the output voltage of the stack is very high. Therefore, the insulation may be changed for polyethylene with a permittivity of 2.3. By trying a few values and computing backwards through equations, 4.5 cm of radius of stalk gives the desired output impedance of 50 Ω. The inductance and the capacitance of the stalk structure are also changed, but not drastically: L_{ks} is in this case 4.60 nH and C_c is 9.77 pF. Analytical equations (see section 11.2 Features of the Adder Stack) and simulation studies may be used to check the effects of these changes to the rise and fall times of the output pulse. Table 2 summarizes the parameter values.

Table 2: Design parameters for two inductive adder stacks with different dielectrics.

l_p cm	l_c cm	D_3 cm	D_2 cm	D_1 cm	d cm	$(D_1-d)/2$ mm	ε	L_{ks} nH	L_{kp} nH	C_c pF	Z_{out} Ω
4.00	2.54	16.00	8.00	7.60	5.90	8.5	1.0	2.44	20	8.79	50.53
4.00	2.54	16.00	8.00	7.60	4.50	15.5	2.3	4.60	20	9.77	50.19

Remarks

Permeability of the core material affects the magnetizing inductance and hence the value of the magnetizing current, but this does not affect the inductance of the stack. The exact value of the primary inductance is difficult to compute analytically beforehand, therefore a few iteration steps with prototypes may be required to get the impedance of the adder stack to be matched to the load. However a code such as FastHenry [39] or Opera3D [40] could be useful to calculate the inductance. Diameter of the rod, the height of the cell and the permittivity of the dielectric can be modified to match the output impedance of the stack to the load. The coupling capacitance and the secondary leakage inductance are desired to be as low as possible, but there is a trade-off between these parameters.