FE-I4 pixel readout chip and IBL module

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On behalf of ATLAS FE-I4 / IBL collaboration

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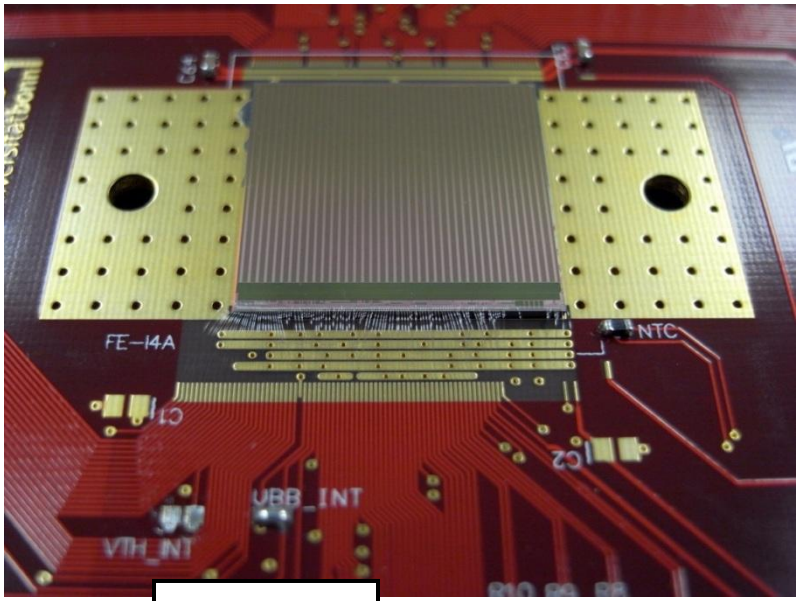
SI LAB
Silizium Labor Bonn

ATLAS Pixel Detector Collaboration

Plan

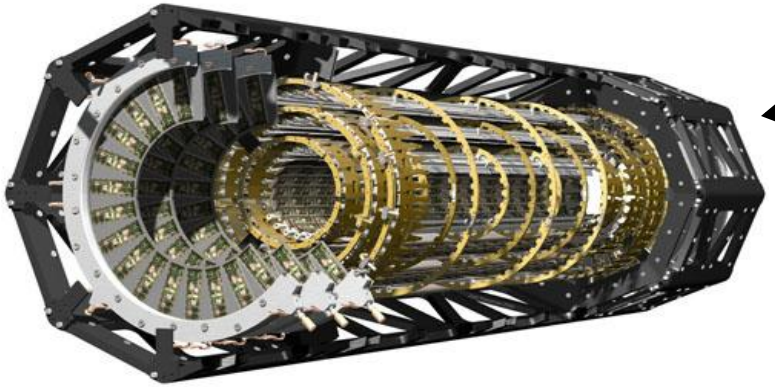
- FE-I4: A new Front-End generation for the upgraded ATLAS pixel detector.
- IBL module concept.
- Sensor technologies for IBL.
- Conclusion.



FE-I4A

FE-I4 what for?

Present beam pipe & B-Layer



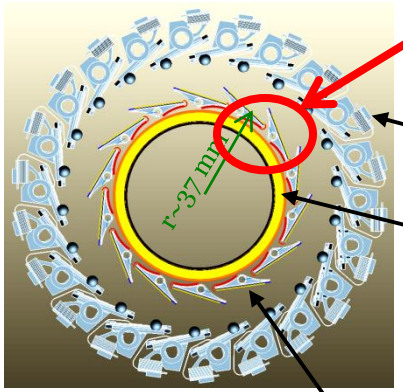
ATLAS Pixel Detector

FE-I3

3 barrel layers / 3 end-caps
end-cap: z± 49.5 / 58 / 65 cm
barrel: r~ 5.0 / 8.8 / 12.2 cm

- Fast IBL ('13): inserted layer in current detector.

FE-I4



Existing B-layer

New beam pipe

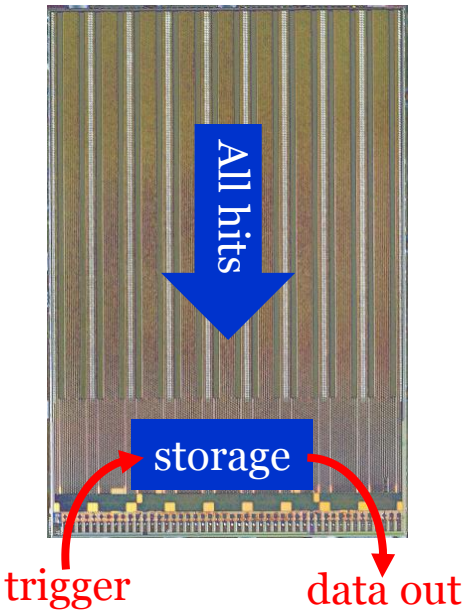
IBL mounted on beam pipe

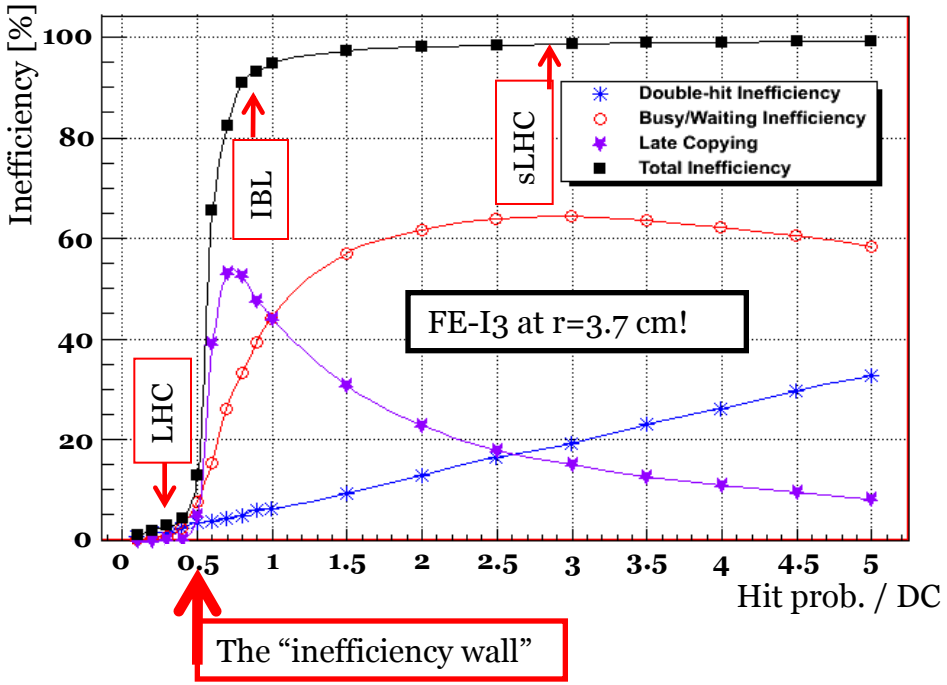
•Phase1 tentative layout (>'17): 4-5 pixel layers, small radii / large(r) radii (note: Discussion on boundary pixel / short strips, ...).

- All Silicon.
- Long Strips/ Short Strips / Pixels.
- Pixels:
  - 2 or 3 fixed layers at 'large' radii (large area at 16 / 20 / 25 cms?)
  -2 removable layers at 'small' radii

High hit rate

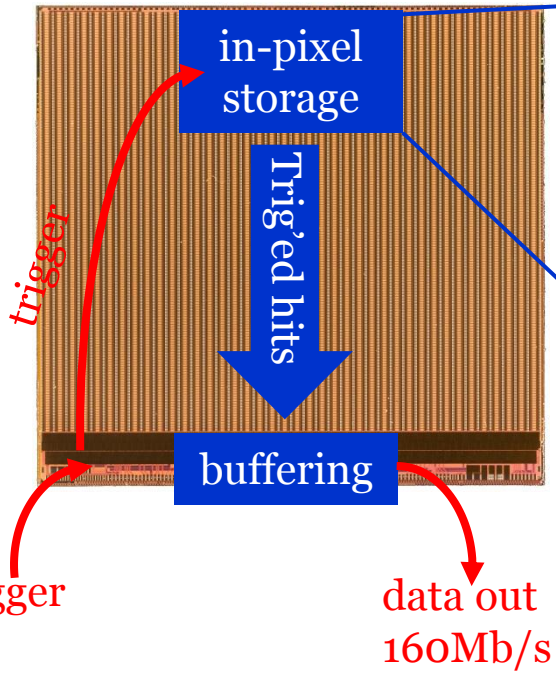
- FE-I3: All hits go to periphery (column drain architecture).

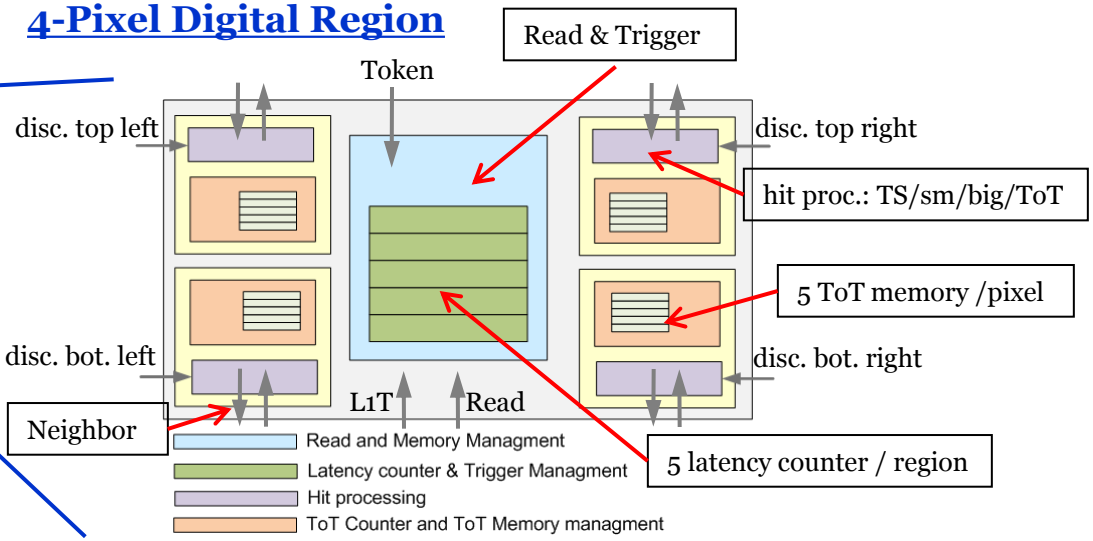




High hit rate

- FE-I3: All hits go to periphery (column drain architecture).
- FE-I4: local "in-pixel" storage + trigger propagated up the array.



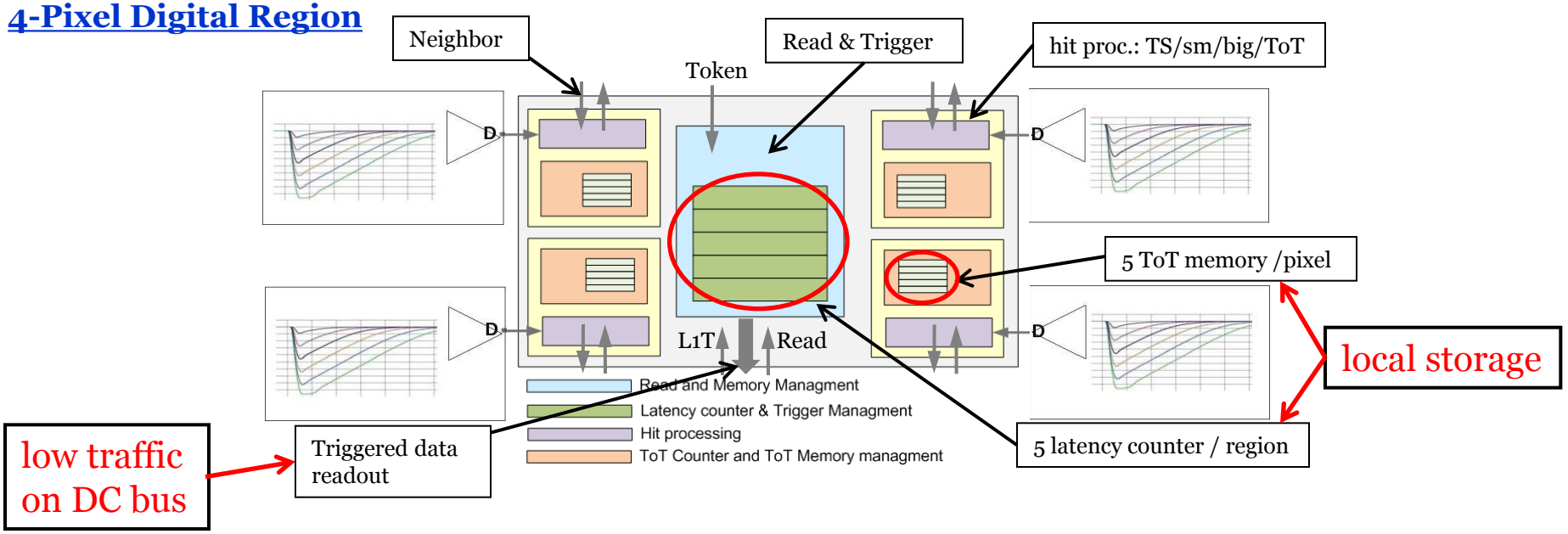


At 3×LHC full lumi, ineff: ~0.6%

4-PDR other advantages: better active fraction (memory in array), low power (un-triggered hits do not move), spatial association.

Digital Pixel: Regional Architecture

4-Pixel Digital Region



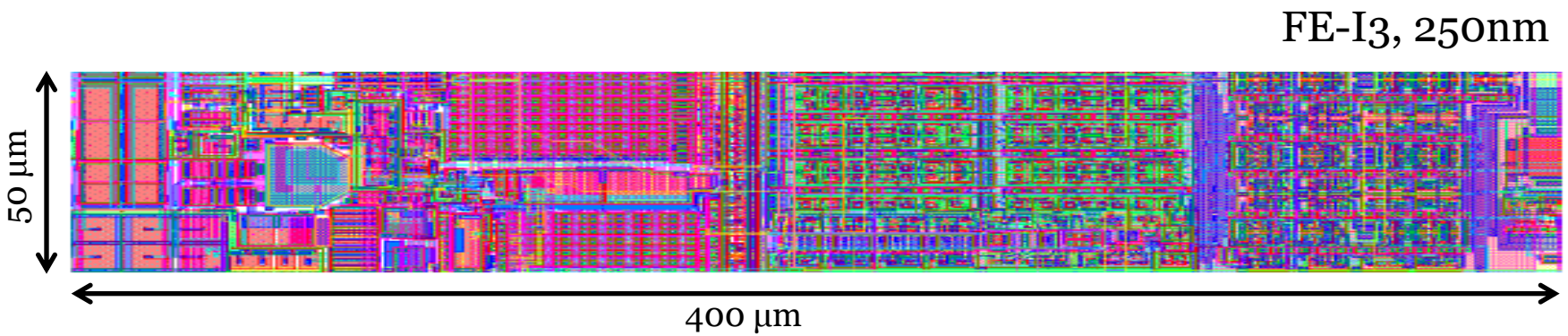
- Store hits locally in region until L1T.
- Only 0.25% of pixel hits are shipped to EoC → DC bus traffic "low".
- Each pixel is tied to its neighbors -time info- (clustered nature of real hits). Small hits are close to large hits! To record small hits, use position instead of time. Handle on TW.

Consequences:

- Spatial association of digital hit to recover lower analog performance.
- Lowers digital power consumption (below 10 µW / pixel at IBL occupancy).
- Physics simulation → Efficient architecture.

Process & granularity

- FE-I3: 0.25µm process, 50×400µm².

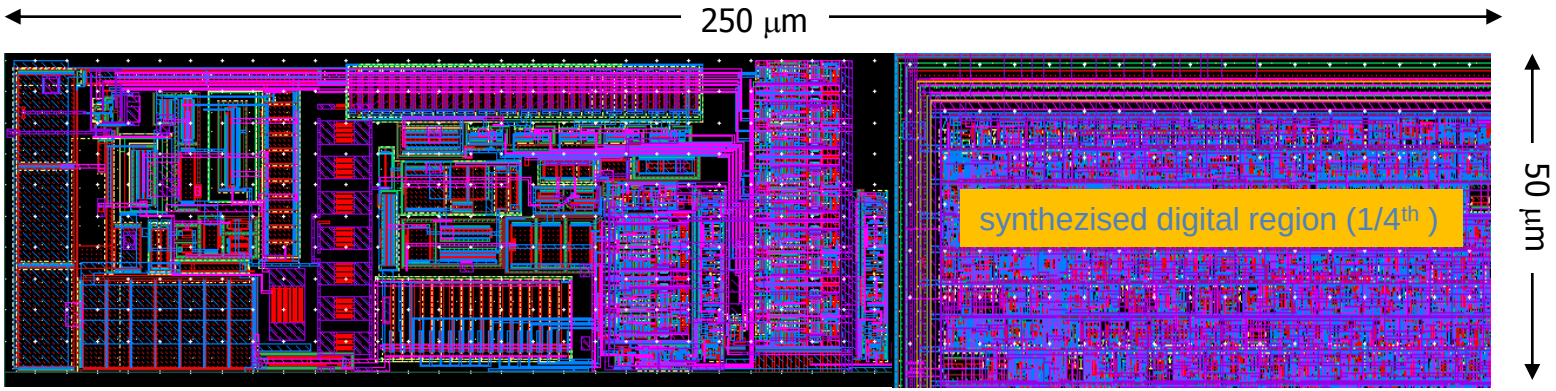


Needed ELT for radiation-tolerance.

- Tolerant to 50MRad

Process & granularity

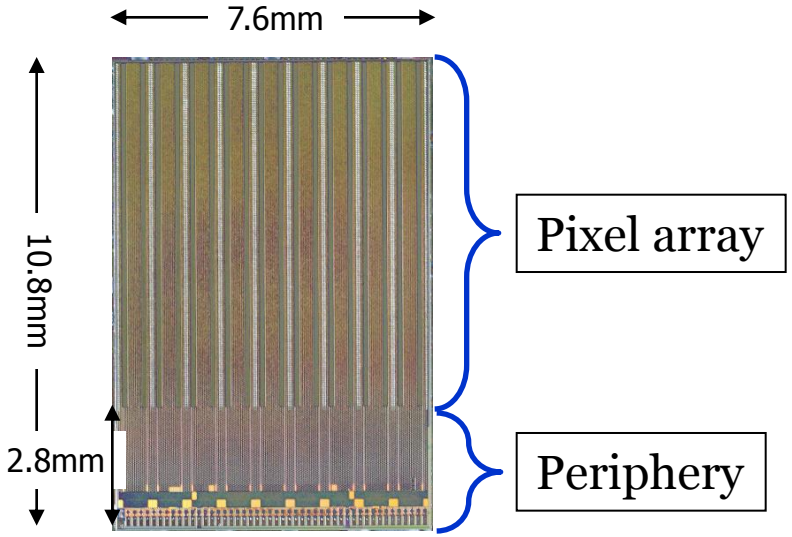
- FE-I3: 0.25µm process, 50×400µm².
- FE-I4: 130nm process, 50×250µm².

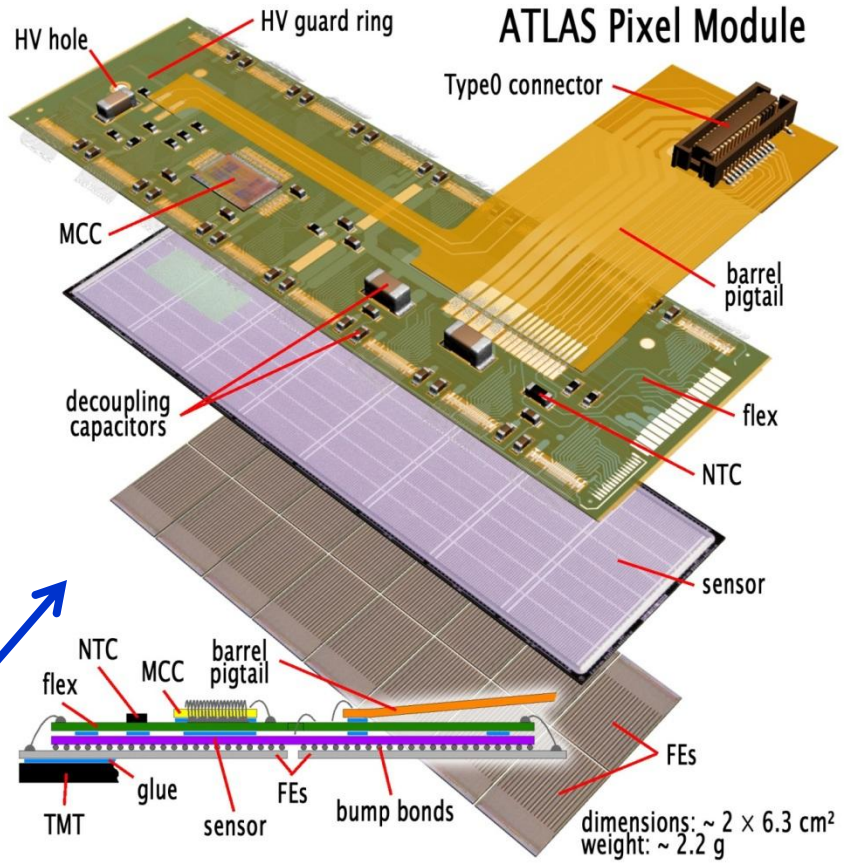


- Radiation hardness with minimal effort & substrate isolation (T3 well) → Can use standard synthesized cells!
- Tolerant to 250MRad.
- 8-metal layers, good power distribution → Can make big IC.

Size of the IC & module concept

- FE-I3: 0.76×1.08cm².
- Active area: 74%.
- 2,880 pixel (18×160).

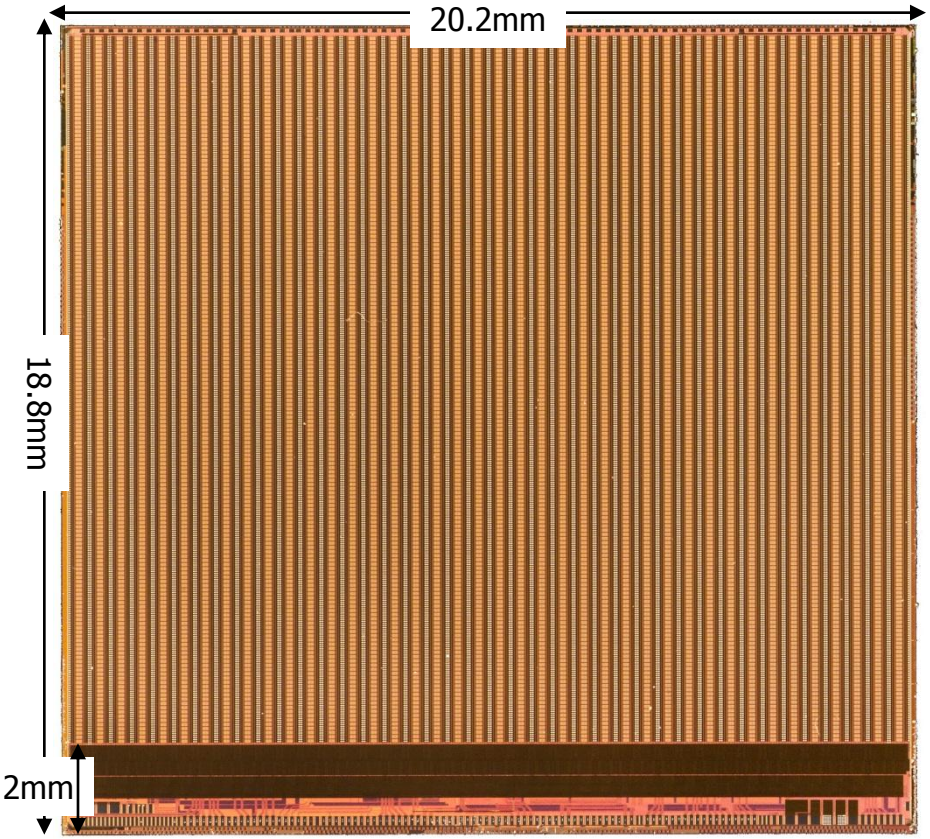




- 16-FE-I3 module with MCC

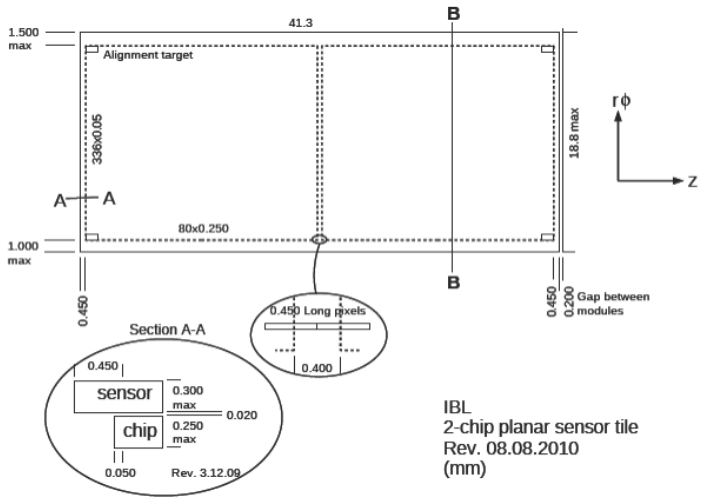
Size of the IC & module concept

- FE-I3: 0.76×1.08cm².
- FE-I4: 2.02×1.88cm².



Active area: ~90%

26,880 pixels (80×336)

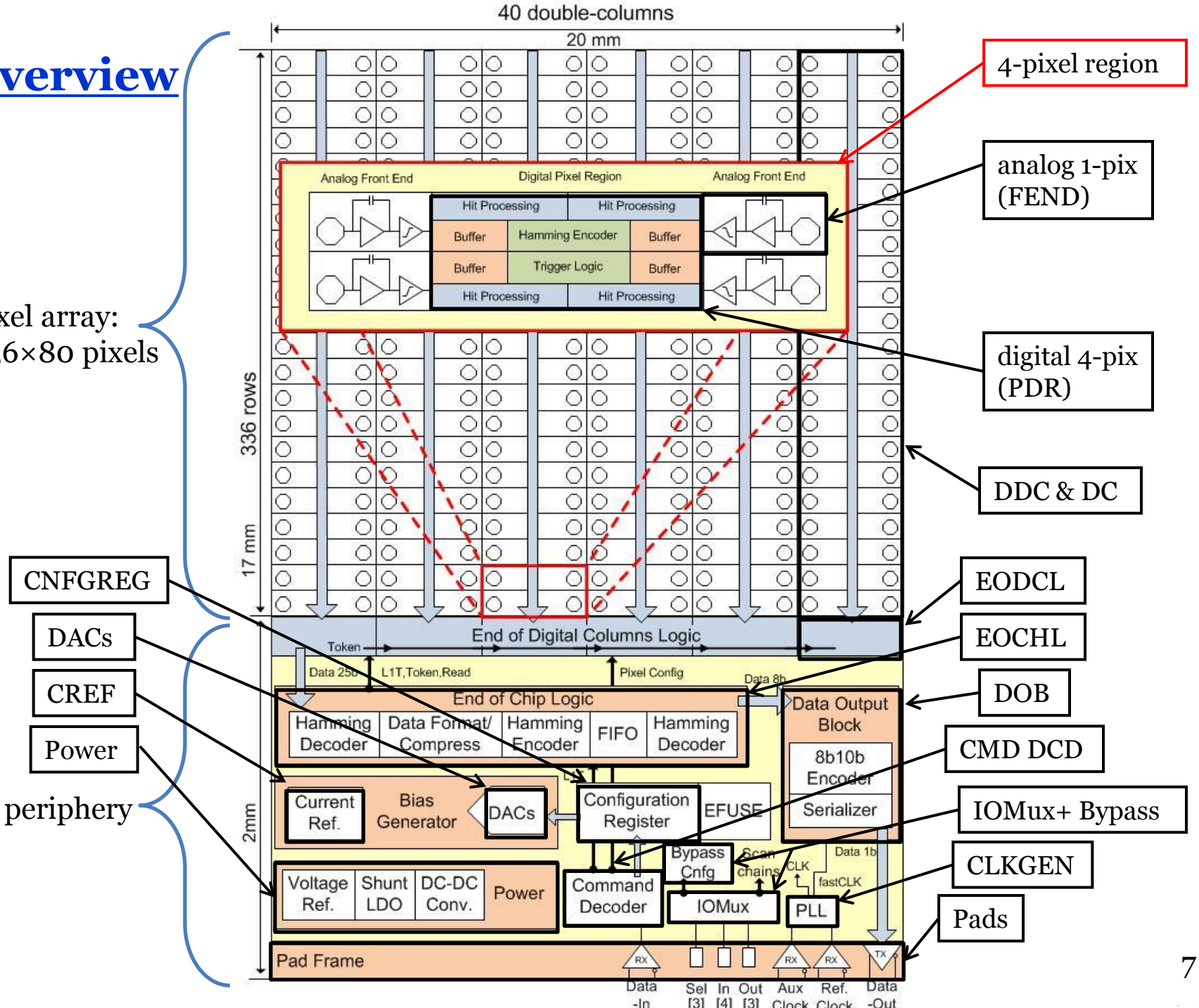


2 ICs: Shared clk and cmd inputs.

But each IC has dedicated output.

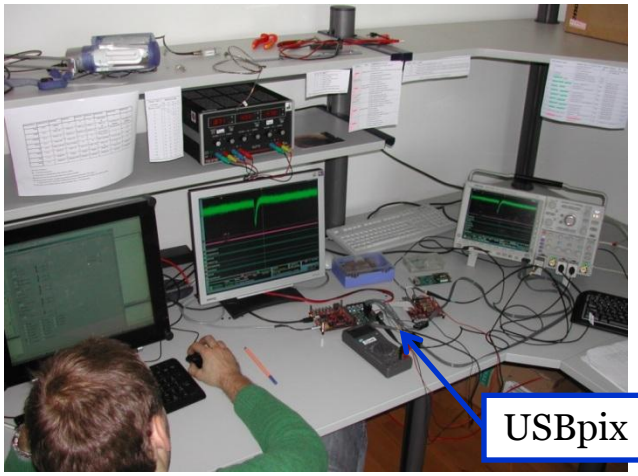
→ Simpler module concept!

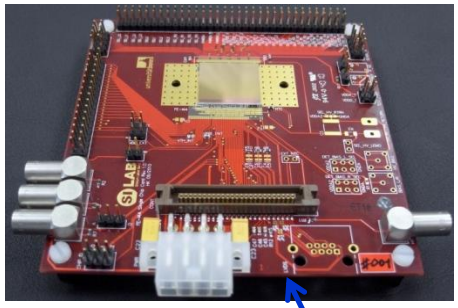
- **Overview**

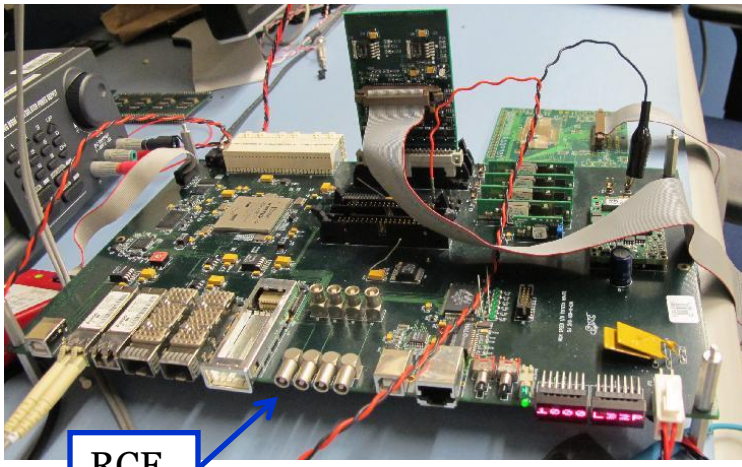

40 double-columns
20 mm
4-pixel region
analog 1-pix (FEND)
digital 4-pix (PDR)
DDC & DC
pixel array: 336×80 pixels
336 rows
17 mm
Analog Front End
Digital Pixel Region
Analog Front End
Hit Processing
Hit Processing
Buffer
Hamming Encoder
Buffer
Buffer
Trigger Logic
Buffer
Hit Processing
Hit Processing
CNFGREG
DACs
CREF
Power
periphery
EODCL
EOCHL
DOB
CMD DCD
IOMux+ Bypass
CLKGEN
Pads
End of Digital Columns Logic
Token
Data 25b
L1T,Token,Read
Pixel Config
Data 8b
End of Chip Logic
Hamming Decoder
Data Format/ Compress
Hamming Encoder
FIFO
Hamming Decoder
Data Output Block
8b10b Encoder
Serializer
Current Ref.
Bias Generator
DACs
Configuration Register
EFUSE
2mm
Bypass Cnfg
Scan chains
CLK
fastCLK
Data 1b
Voltage Ref.
Shunt LDO
DC-DC Conv.
Power
Command Decoder
IOMux
PLL
Pad Frame
RX
RX
RX
TX
Data -In
Sel [3]
In [4]
Out [3]
Aux Clock
Ref. Clock
Data -Out

FE-I4A testing

- Upstream efficient test setup development led to test all main features of this complex chip in few months.





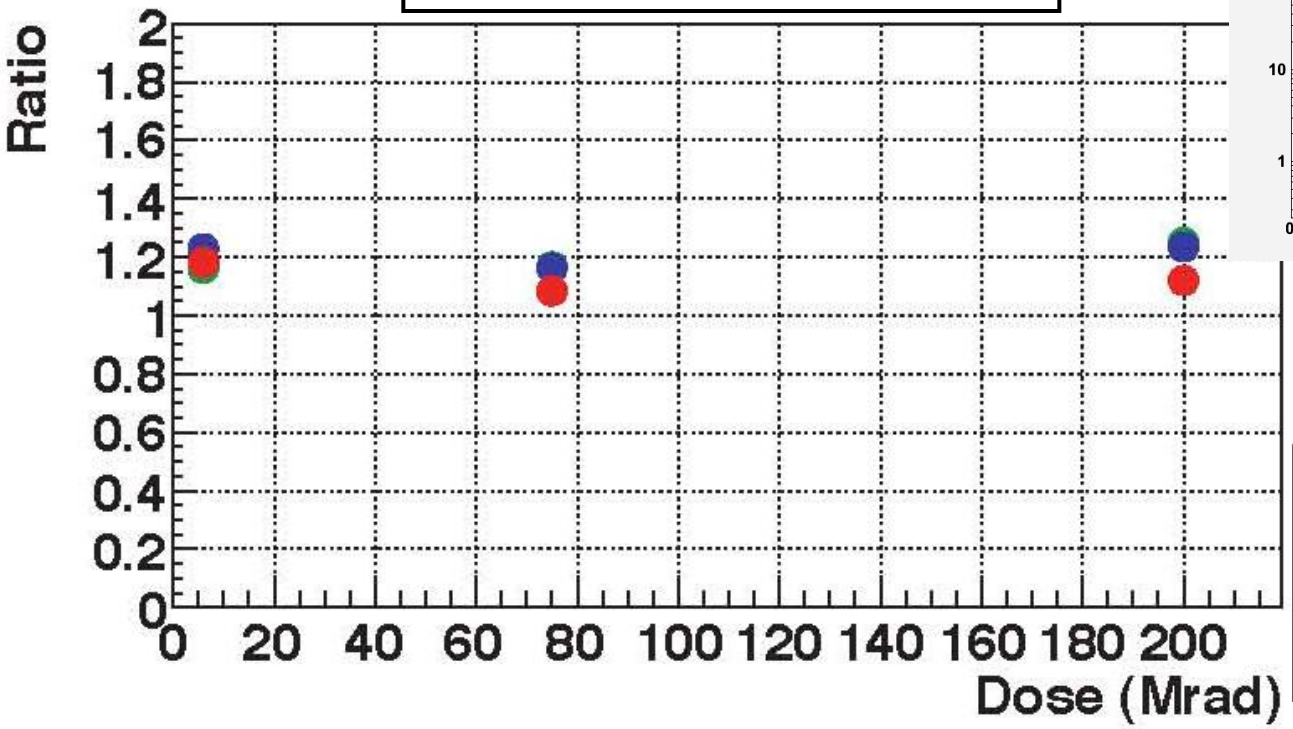


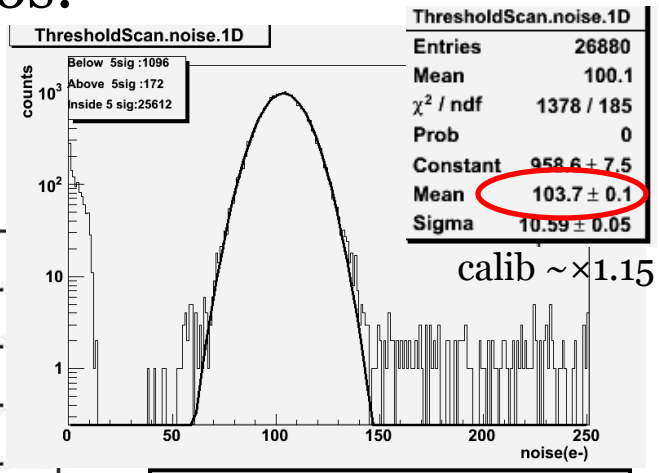
- All digital functionalities OK.
  - 4-pixel digital region.
  - Formatting (EOCHL + DOB). (small fixes necessary)
  - Communication + memories.
- PLL for 160Mb/s data transfer. Yield ~70%
- Powering (Shunt-LDO) working ~specs. (Tuning for IBL on-going)

Dose and noise

- Typical noise bare IC after calibration ~ 110e$^-$.
- 800MeV proton irradiation at Los Alamos:
  - 6 / 75 / 200 MRad.

Ratio noise after / before dose





calib ~×1.15

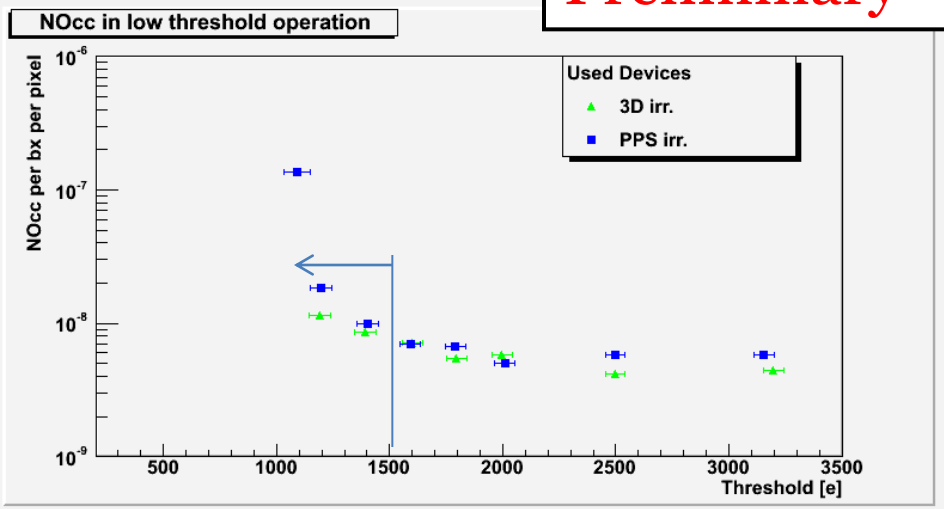
e.g. noise histogram

TDAC 0: unirradiated
TDAC 0: irradiated
TDAC 8: unirradiated
TDAC 8: irradiated
TDAC 16: unirradiated
TDAC 16: irradiated

Low threshold behavior

Preliminary

- Studies on PPS and 3D assemblies irradiated with protons to **5.10^{15} n_{eq}/cm^2**.
- Noise occupancy increase when below ~1500e^-.
- At 1100 e^-, NOcc~10^{-7}. Threshold down to 1100 electrons possible!
- Low threshold operation w. irradiated sensors demonstrated!
- Note: Masked pixel floor = digitally un-responsive pixels. Due to no Ileak compensation in pixel?



IBL Sensor Specifications

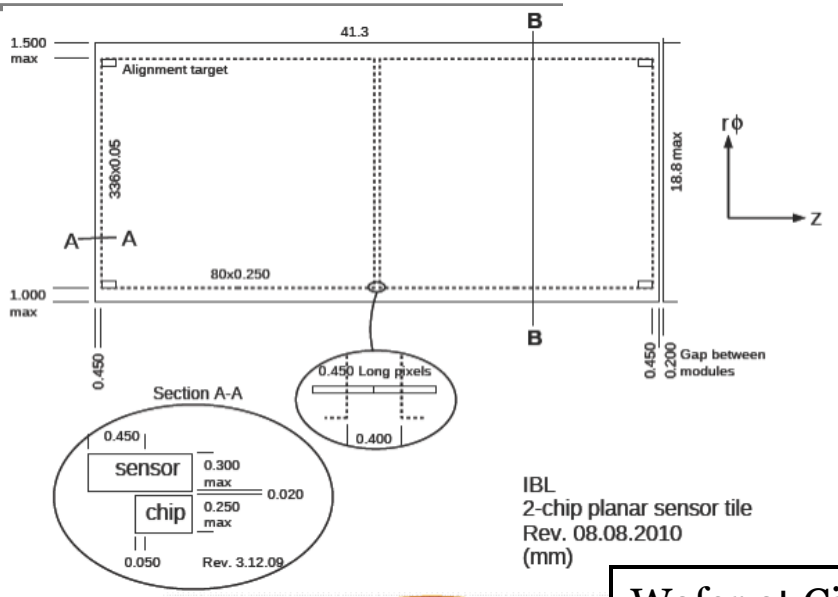
- IBL environment: Radiation hard FE and sensor.
- So far, two different pixel sensor technology candidates: n-in-n planar / partial-3D silicon.
- Specifications:
  - HV: max 1000V.
  - Thickness: 225±25µm.
  - Max. power dissipation: 200mW/cm² at -15°C.
  - No shingling in z → Edge width: below 450µm.
  - Tracking efficiency: above 98%.

- Choice for technology: Install Summer 2013 → Sensor Prod. completed Summer 2012 → Sensor choice in July 2011.

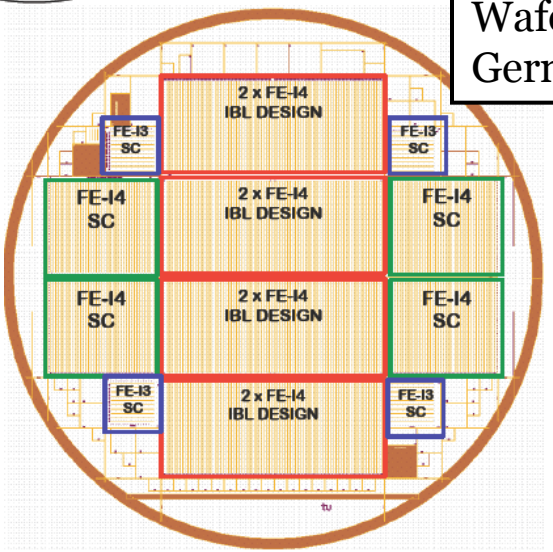
Detailed schedule / Procurement: Heinz Pernegger's talk Tuesday

2-Chip Planar Sensor Tile

- Some R&D areas:
  - Slim edge sensors.
  - Radiation damage.
  - Low threshold FE-operation.
  - Low cost, large scale prod.
- Main advantage:
  - All benefits of a mature technology (yield, cost, experience).
- Main challenges:
  - Low Q collection after irrad.
  - Inactive area at sensor edge.



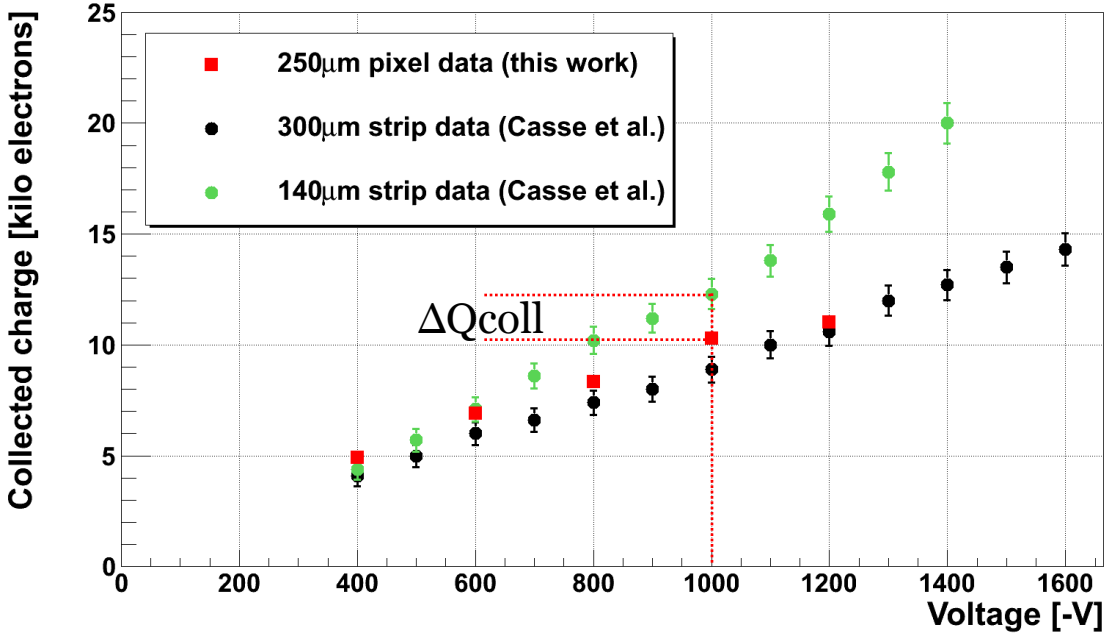
Wafer at CiS, Germany



IBL design choice for planar

- n-in-n slim edge 200 µm thick with ~200µm inactive edge.
- Thinner sensors generate more charge after 5.10^5 n_{eq}/cm^2 than thicker ones at same HV (higher field).
- Low material

good for tracking

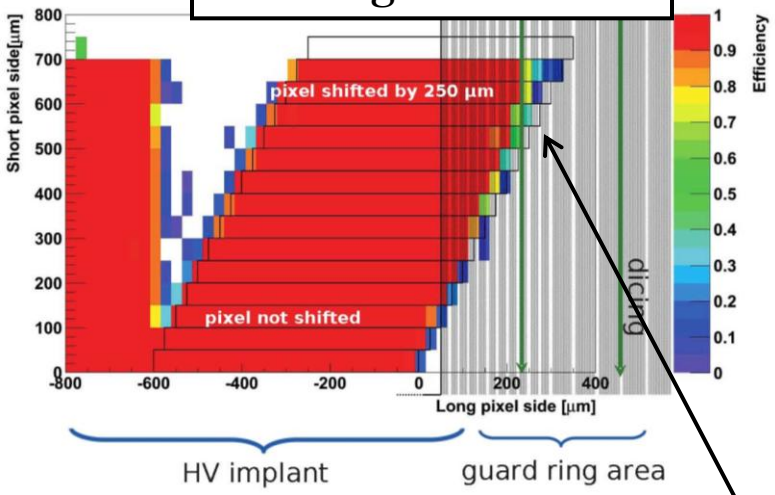


- + Constraints from safe processing at sensor provider + handling by flip-chipping provider → 200µm thick sensor.

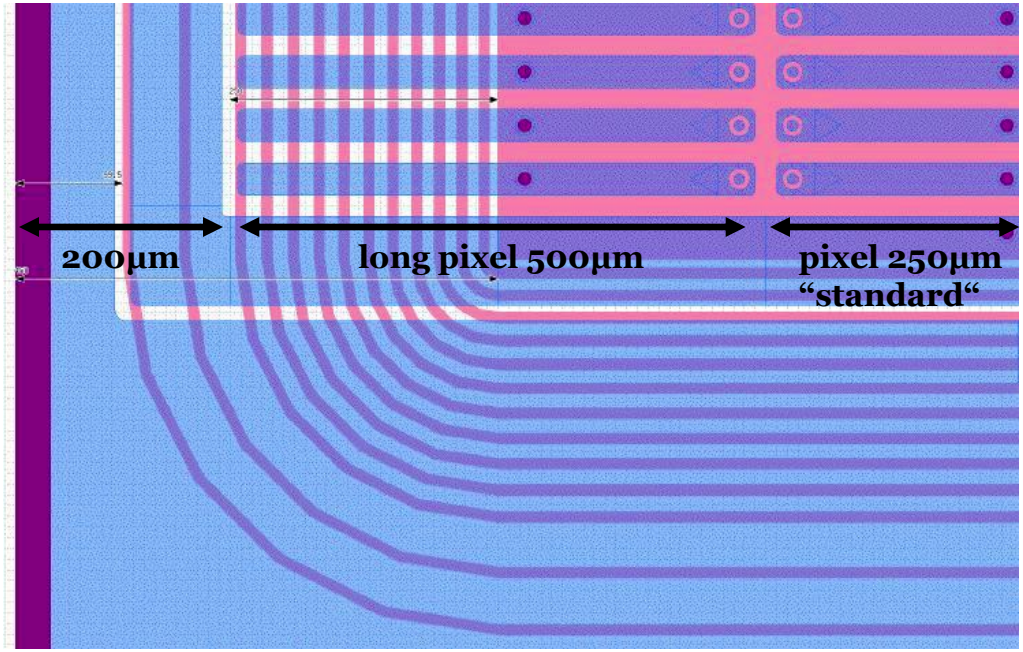
IBL design choice for planar

- n-in-n slim edge 200 µm thick with ~200µm inactive edge.
- As guard ring opposite side from pixel implant, shift guard rings under active pixel region. Lose homogeneity at edge, but after irradiation Qcollection mainly from under pixel implant.

Slim edge studies



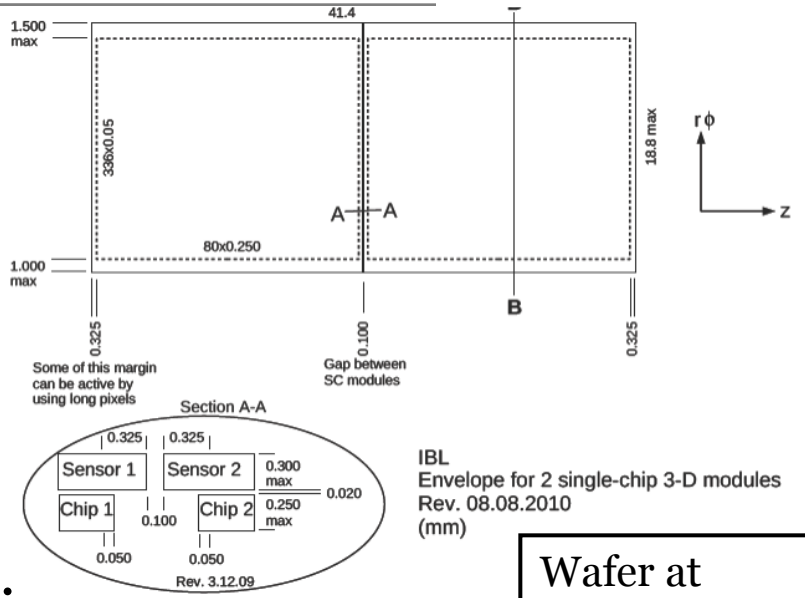
from dedicated test structure

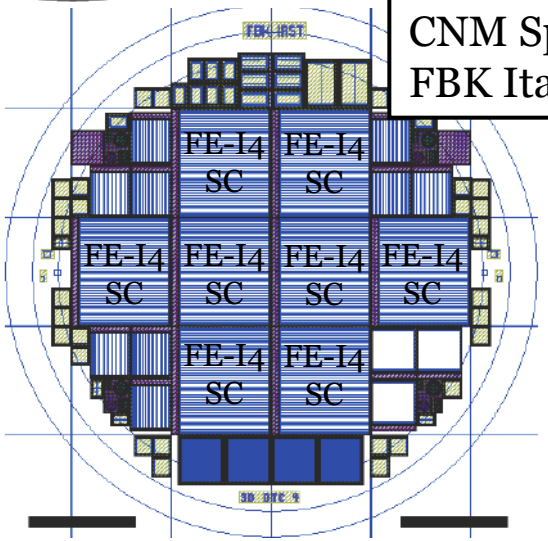


Test beam: >99% efficiency (pre-irrad) for 250µm inefficient edge

1-Chip 3D Sensor Tile

- Some R&D areas:
  - Processing of TSV.
  - Yield.
  - Signal vs # electrodes / cell.
- Main advantage:
  - Radiation hardness.
  - Low depletion voltage (max 180V).
  - Active edge.
- Main challenges:
  - Production yield.
  - In-column inefficiency at normal incidence.

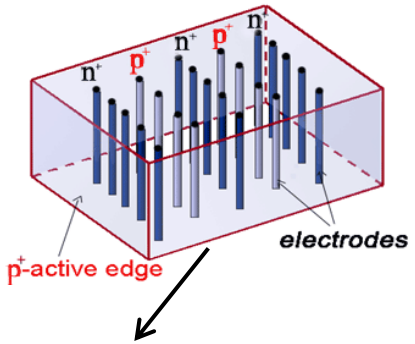




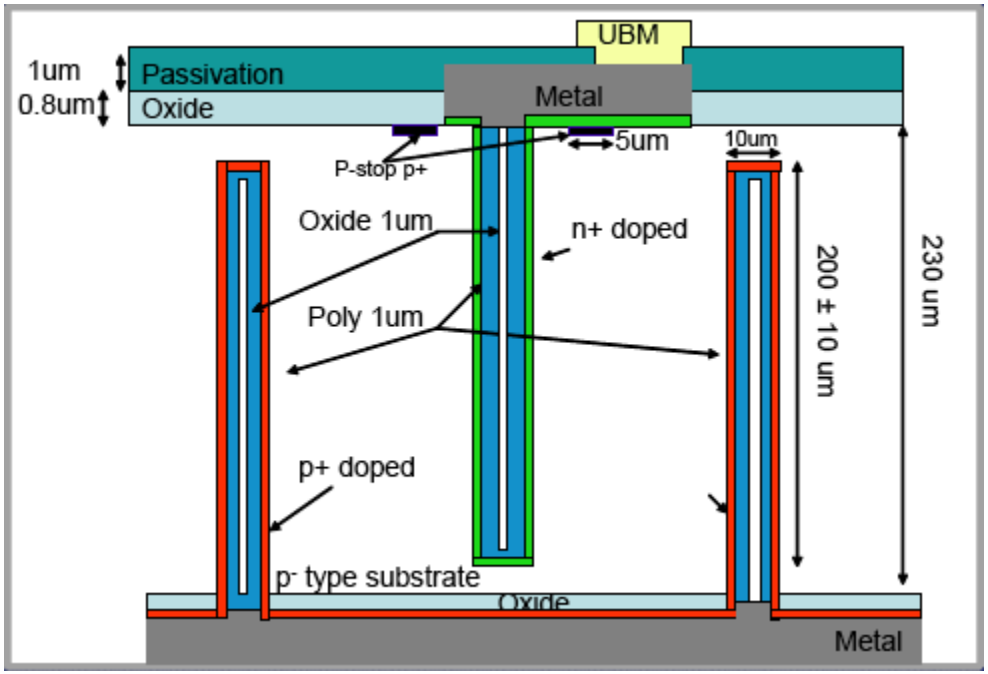
Wafer at CNM Spain / FBK Italy

IBL design choice for 3D

- Double-Sided partial 3D, 2E250 electrode configuration, slim edges:

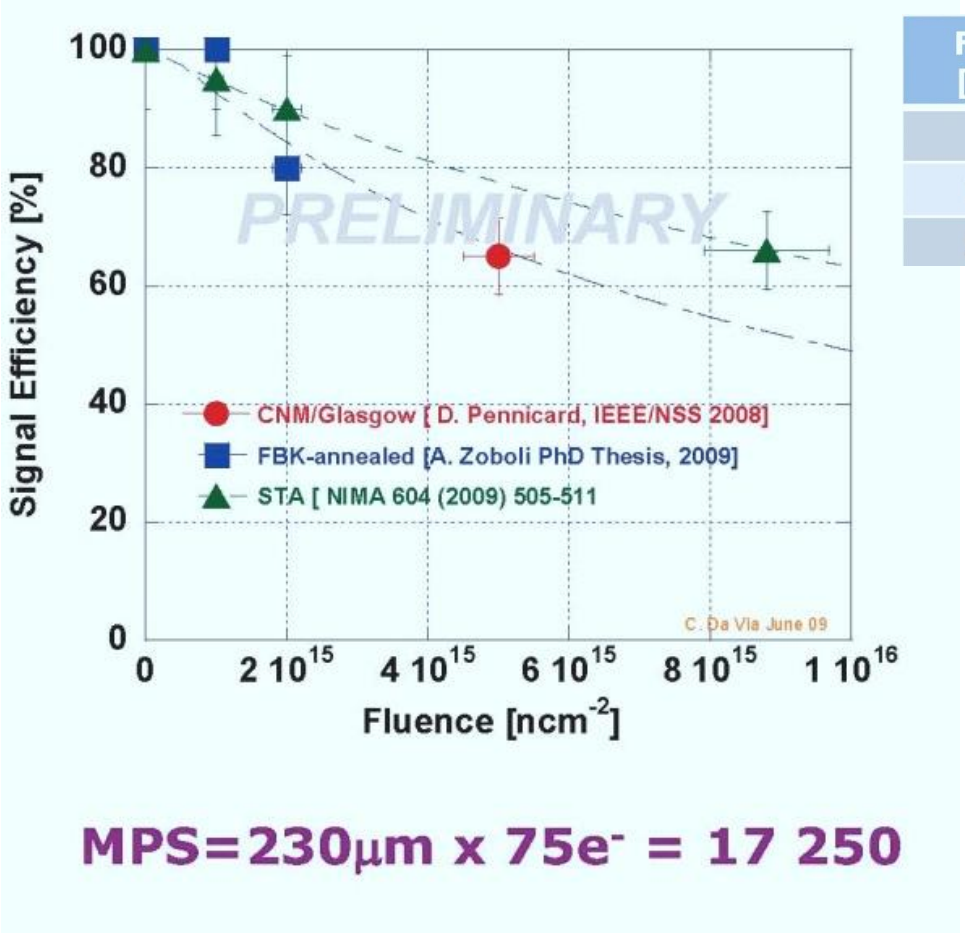


- 2E250: Inter-electrode pitch ~70µm. Compromise between CCE and capacitive noise.
- Active edges & full 3D processing not established enough on project time scale.

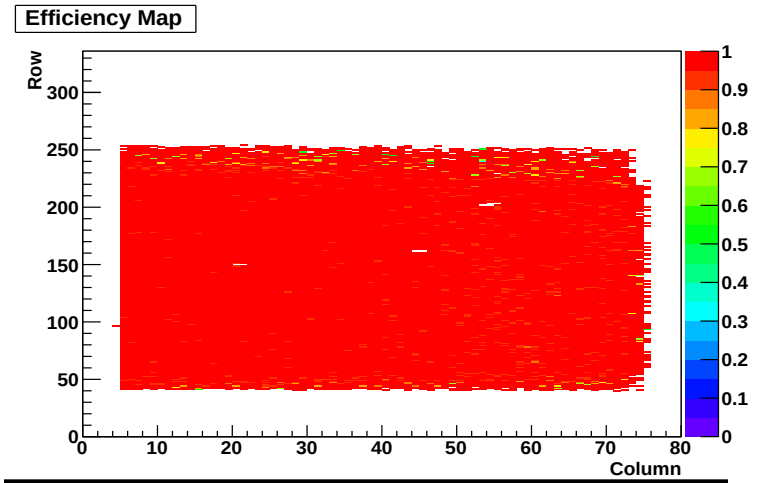


3D charge collection wrt irrad.

- High charge collection even at 5.10^{15} n_{eq}/cm^2.



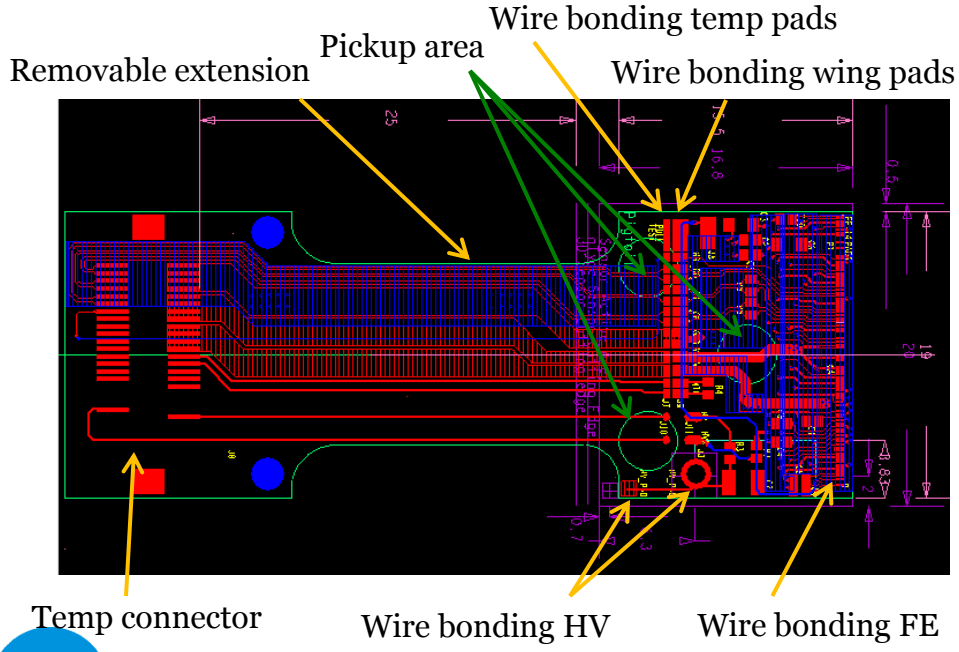
Fluence [ncm^{-2}]	MPS [e$^-$]
0	17250
1x10^{15}	16380
5x10^{15}	12075

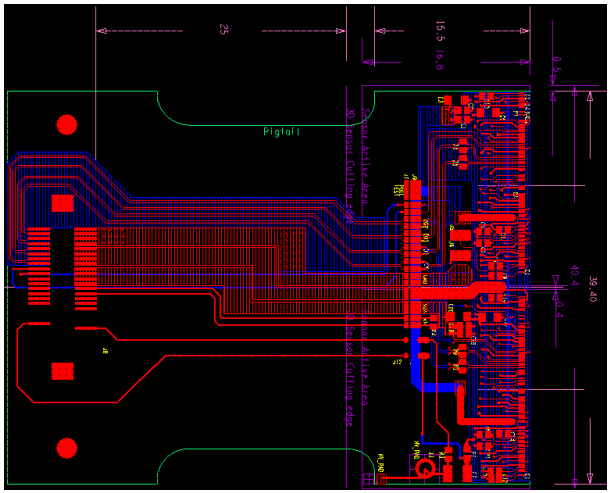


FBK un-irrad. 98% eff for normal incidence → ~100% for tilted tracks

Flex development

- Flex routes signals and supplies from FE/sensor to internal services(sensor: HV ; IC: LV, DCI, CLK, Dout, HitOr).
- Make loading on stave easy (alignment marks, area for pick-up), and testing of module too.
- 2 versions currently developed: Single-Chip or Double-Chip.

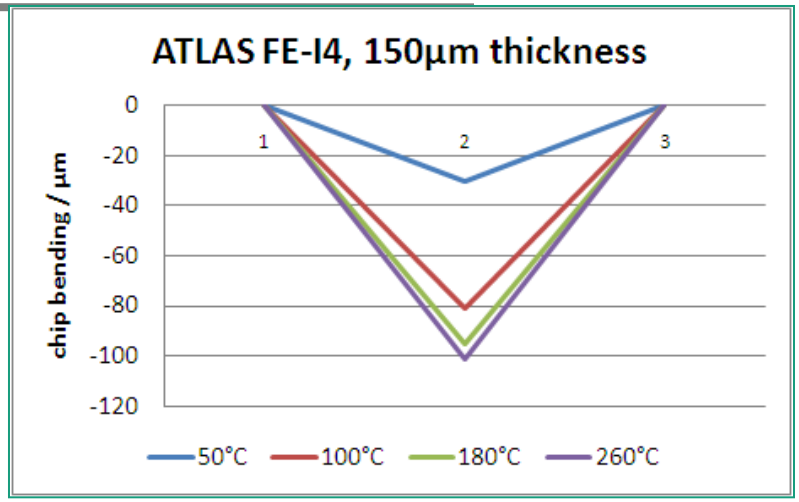


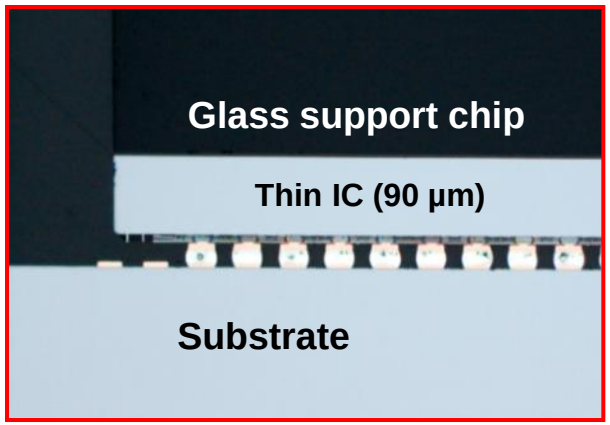


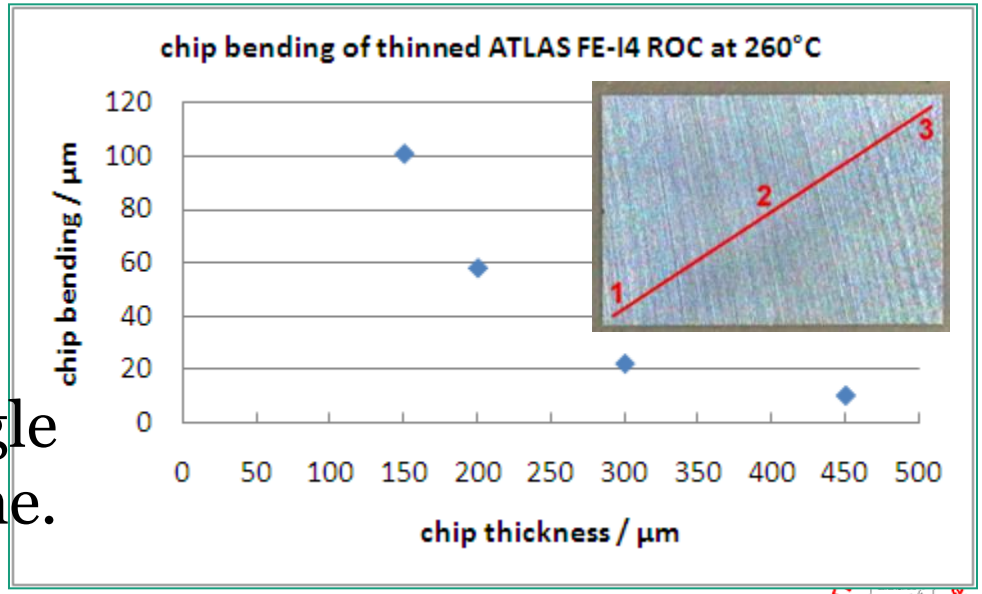
Ordered at Phoenix (Ivrea, Italy), back end June

Thin Chip Bump-Bonding

- Safe bump-bonding requires max bend ~15µm.
- Minimal thickness of 450µm.
- Use temporary glass handling wafer + laser de-bonding.



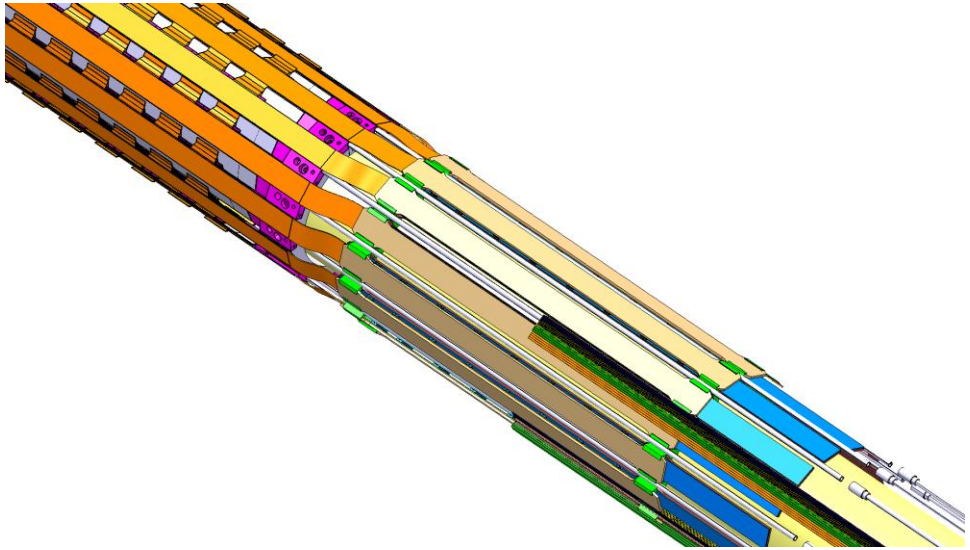




- Prelim test: promising! 8 single chip 150µ assemblies end June.

Conclusion

- Based on success of FE-I4A development, and characterization work of sensor communities
- Not much contingency in schedule means success oriented developments.



- FE-I4B design: July 2011.
- Sensor choice: July 2011.
- IBL module R&D on-going:
  - Flex design.
  - Thin chip bump-bonding

→ fast track IBL with installation in 2013.