Readout Electronics for the ATLAS LAr Calorimeter at HL-LHC

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On behalf of the ATLAS Liquid Argon Calorimeter Group

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BROOKHAVEN
NATIONAL LABORATORY

a passion for discovery

Office of Science
U.S. DEPARTMENT OF ENERGY

Outline

- Introduction
  - ATLAS Liquid Argon Calorimeter
  - Current LAr Readout Electronics
  - LAr Electronics Upgrade Motivations
- Readout Electronics R&D Studies for HL-LHC
  - Front-end mixed-signal ASIC design
    - BNL, Columbia Univ., Univ. of Penn., INFN Milan, IN2P3
  - HEC cold electronics
    - MPI Munich
  - Radiation tolerant optical link in Silicon-on-Sapphire
    - SMU
  - High speed back-end processing unit based on FPGA
    - BNL, Univ. of Arizona, SUNY Stony Brook, IN2P3 LAPP, INFN Milan, Dresden, CERN
  - Power supply distribution scheme
    - BNL, Yale, INFN Milan, Univ. of Milan
- Evolution from Today to HL-LHC
  - Staged upgrade with demonstrator system
- Summary

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  - **Current LAr Readout Electronics**
  - **LAr Electronics Upgrade Motivations**
- **Readout Electronics R&D Studies for HL-LHC**
  - **Front-end mixed-signal ASIC design**
    - **BNL, Columbia Univ., Univ. of Penn., INFN Milan, IN2P3**
  - **HEC cold electronics**
    - **MPI Munich**
  - **Radiation tolerant optical link in Silicon-on-Sapphire**
    - **SMU**

ASICs Development Overview

  - **High speed back-end processing unit based on FPGA**
    - **BNL, Univ. of Arizona, SUNY Stony Brook, IN2P3 LAPP, INFN Milan, Dresden, CERN**
  - **Power supply distribution scheme**
    - **BNL, Yale, INFN Milan, Univ. of Milan**
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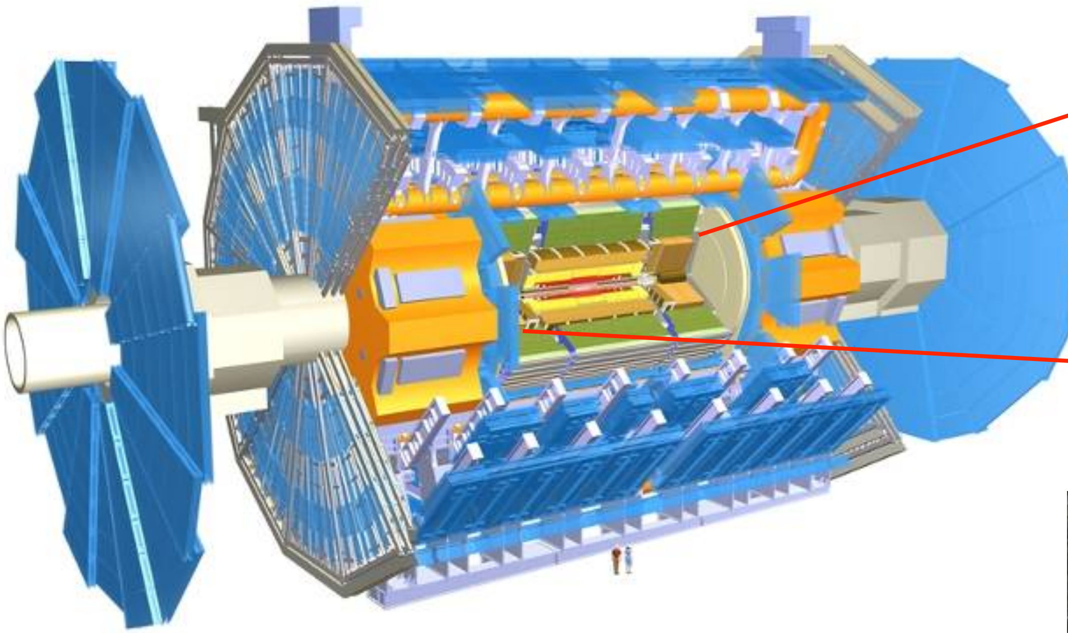
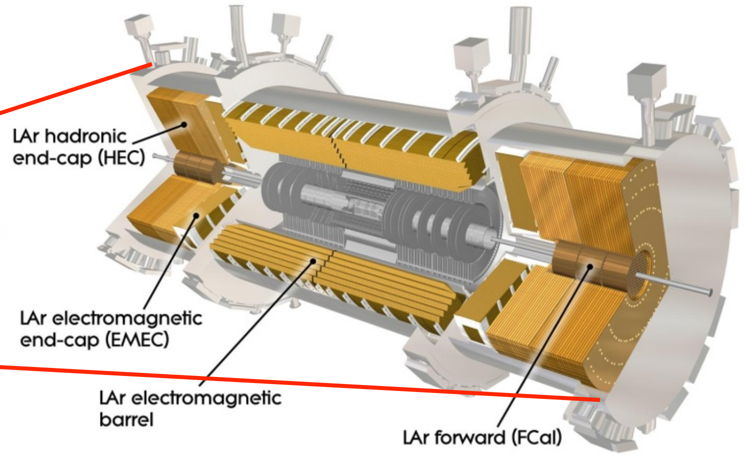
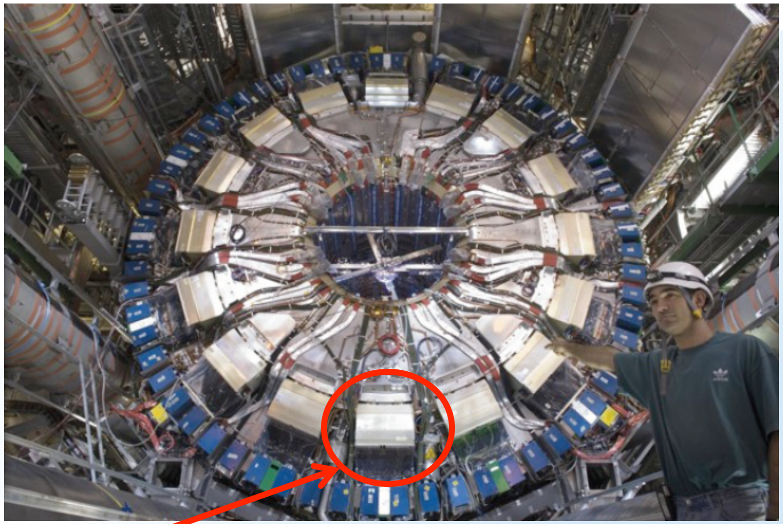
ATLAS Liquid Argon Calorimeter (LAr)





- **Liquid Argon Calorimeter**
  - **Electromagnetic Barrel (EMB)**
    - **$|\eta|<1.475$ [Pb-LAr]**
  - **Electromagnetic End-cap (EMEC)**
    - **$1.375<|\eta|<3.2$ [Pb-LAr]**
  - **Hadronic End-cap (HEC)**
    - **$1.5<|\eta|<3.2$ [Cu-LAr]**
  - **Forward Calorimeter (FCAL)**
    - **$3.1<|\eta|<4.9$ [Cu,W-LAr]**

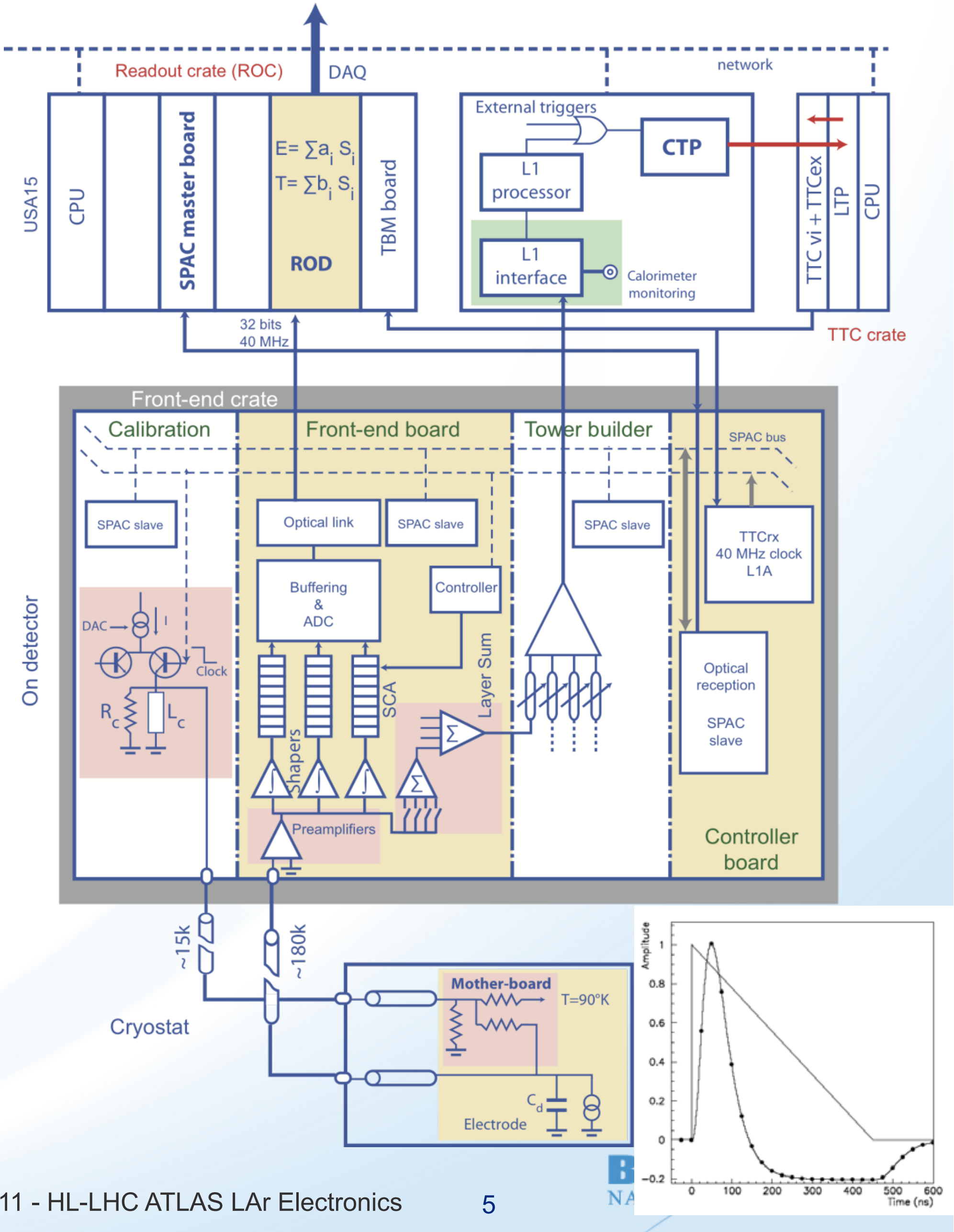


Front End Crate

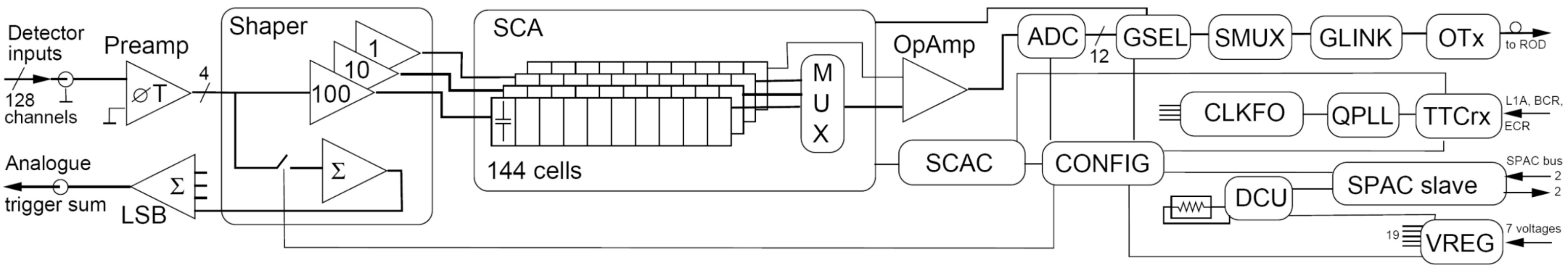
Barrel calorimeters in detector hall, surrounded by barrel toroids

Current LAr Readout Electronics

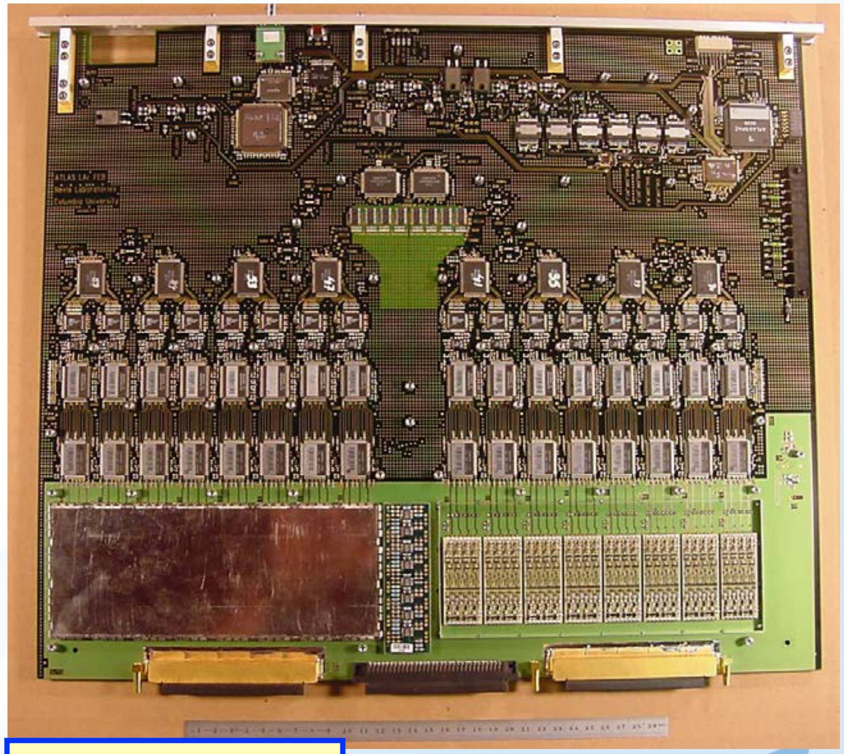
- **182,468 detector channels**
  - **EMB: 109,568 channels**
  - **EMEC: 63,744 channels**
  - **HEC: 5,632 channels**
  - **FCAL: 3,524 channels**
- **Front-end Electronics**
  - **58 Front End Crates**
  - **1524 Front End Boards**
  - **~300 other boards (calibration, tower builder, controller, monitoring)**
  - **58 LV Power Supplies**
  - **~1600 fiber optic links between FE and BE**
- **Back-end Electronics**
  - **16 Back End Crates**
  - **192 Read Out Driver Boards**
  - **68 ROS PCs**
  - **~800 fiber optic links between ROD and ROS**



Current Front-end Architecture

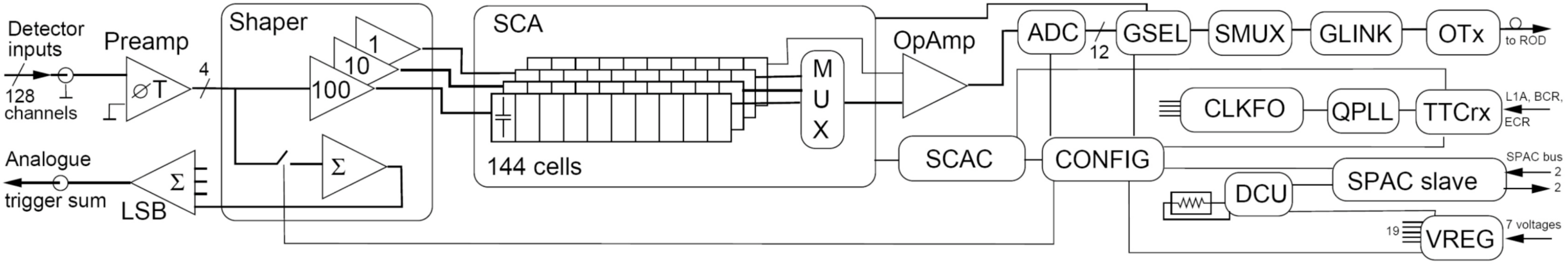


- **FEB Complexity**
  - **11 ASICs**
  - **Several technologies with obsolescence of some technologies (e.g. DMILL)**
  - **19 voltage regulators**
  - **Analog pipelines (SCA)**
  - **~80W/board, water cooled**
- **Radiation/lifetime issues**
  - **Qualified for 10 years LHC operation**
  - **Limited number of spares (~6%)**



Front End Board

Current Front-end Architecture



- **FEB Complexity**
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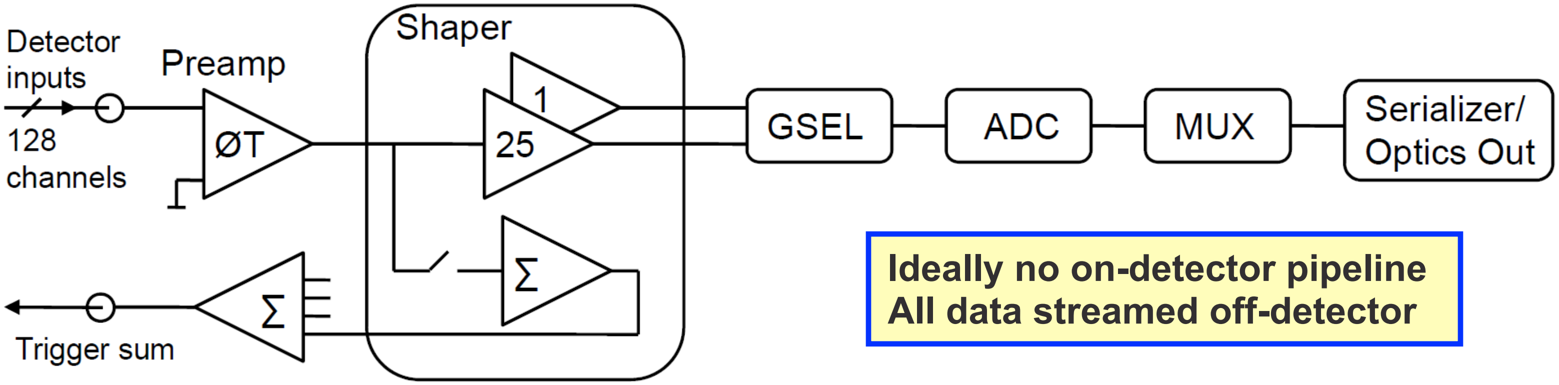
  - **~80W/board, water cooled**
- **Radiation/lifetime issues**
  - **Qualified for 10 years LHC operation**
  - **Limited number of spares (~6%)**
- **Other limitations**
  - **L1 trigger rate <= 100kHz**
  - **L1 trigger latency <= 2.5μs**
  - **Consecutive L1 trigger spaced more than 125ns**
  - **Fixed analog trigger sums**
- **FEB Upgrade**
  - **Component-level replacement impossible**
  - **Full replacement based on current technologies**
  - **No increase of power budget**

Proposed Front-end Architecture



Ideally no on-detector pipeline
All data streamed off-detector

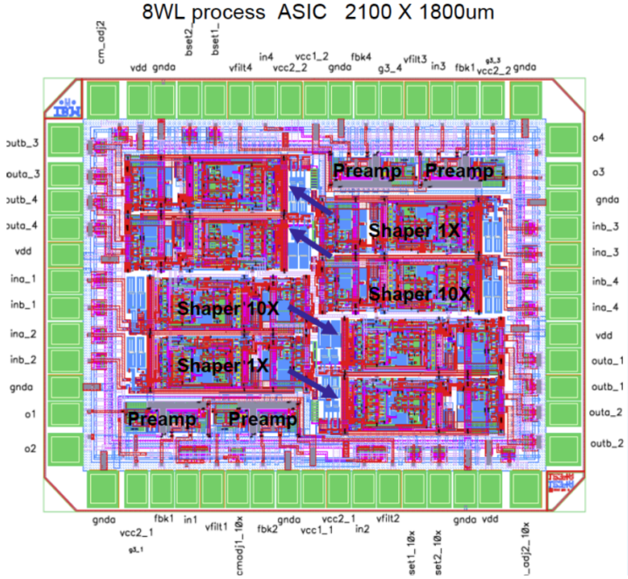
- **Proposed FEB baseline architecture keeps many options open**
  - **Shaping and gain settings**
  - **Analog vs. digital pipeline**
  - **On/off detector pipeline**
  - **Analog vs. digital gain selector**
  - **Possibly provide analog trigger sums to decouple potential trigger upgrade**
  - **Additional information to L1Calo to keep L1 rate below 100kHz**
- **FEB upgrade propagates to other boards**
  - **Digitization at each bunching crossing, data rate is ~100Gbps/board**
  - **Higher speed, higher radiation resistance optical link**
  - **LV power supplies**
  - **Back-end electronics**
  - **Possibly interface to L0Calo/L1Calo digitally**

Analog Front-end: Preamp & Shaper

- **LAPAS ASIC**
  - Quad preamplifier & shaper ASIC in IBM 0.13µm SiGe 8WL
- **Preamplifier**
  - Based on low noise line-terminating preamplifier circuit topology used presently
  - High breakdown devices allow for higher swing to accommodate full 16-bit dynamic range
  - $e_n \sim 0.26 \mathrm{nV}/\sqrt{\mathrm{Hz}}$
  - ENI ~ 73nA RMS (included 2nd stage and for $C_d = 1\mathrm{nF}$)
  - $P_{tot} \sim 42\mathrm{mW}$
- **Shaper**
  - 16-bit dynamic range with two gain settings
  - $e_n \sim 2.4 \mathrm{nV}/\sqrt{\mathrm{Hz}}$
  - ENI ~ 34nA RMS
  - $P_{tot} \sim 130\mathrm{mW}$ (combined 1X, 10X channels)
  - Uniformity: better than 5% across 17 tested ASICs
  - INL: < 0.1% over full scale of 1X and 10X channels
- **LAPAS testing with hand wired prototype**
  - All measurements as expected
  - DC results very close to simulations, shaper peaking time is 37ns as predicted
  - Preamp and shaper transient response is good, no shaper control tuning required
  - Common mode auto-tracking is excellent
  - No significant concerns about first TID results

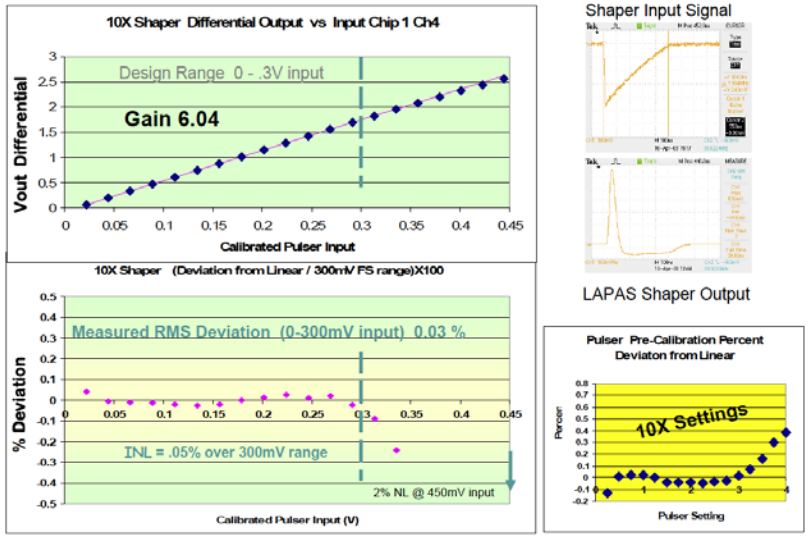
LAPAS: Liquid Argon PreAmplifier Shaper

8WL process ASIC 2100 X 1800um



LAPAS ASIC Automated Linearity Measurement

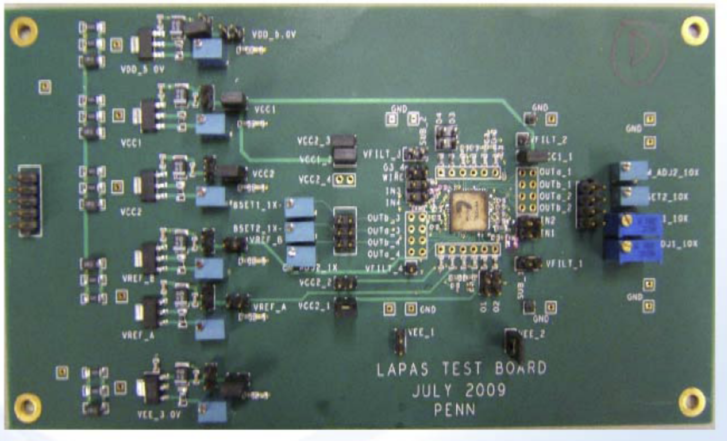
Using AFG3252 & MSO4401

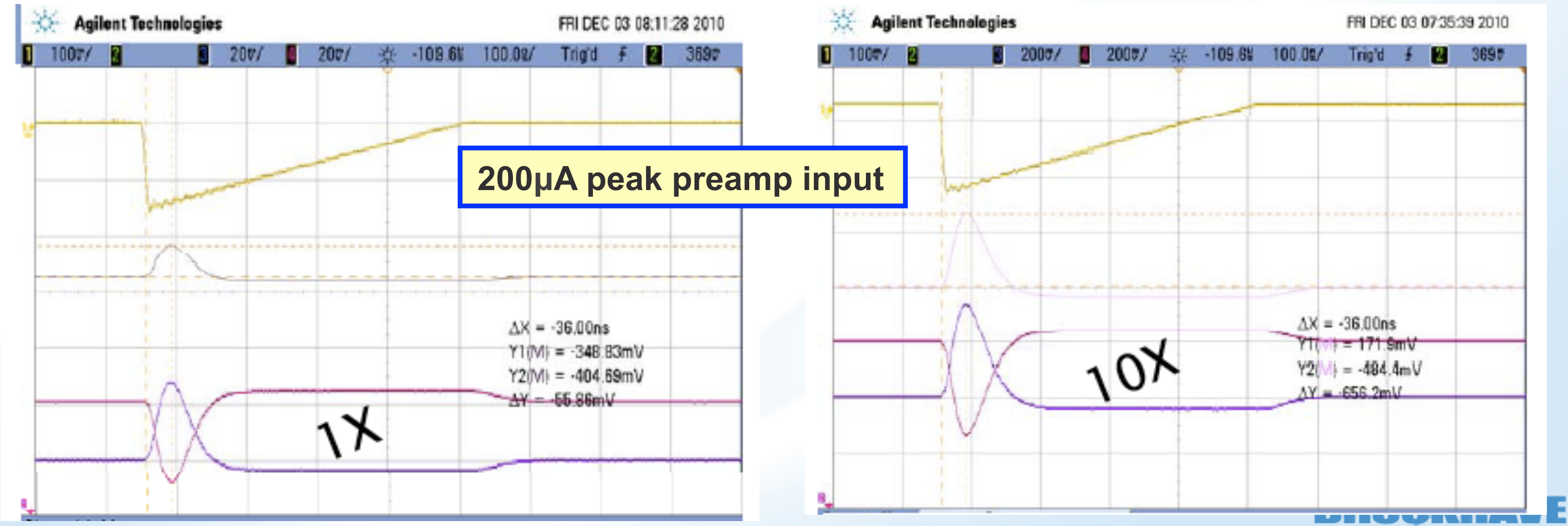


Analog Front-end: Preamp & Shaper

- **LAPAS ASIC Prototype Test Board**
  - **2 – 1X preamp and shaper channels**
  - **2 – 10X preamp and shaper channels**
  - **Reduced and eliminated pickup sensitivity**
  - **Noise measurements on preamp**
    - ENI ~ 85nA for C_d = 1nF
    - Larger than 75nA target value due in part to larger layout resistance and increased FB capacitance
  - **Input impedance measurement**
    - Measured input impedance ~43Ω
    - Larger than 25Ω target value due to additional 0.8Ω resistance in layout
    - Issue resolved by adding resistor in series with feedback
  - **Output drive adjustable**
    - Compatible with gain selector block and differential ADC drive, either 2.34V or 1.2V

Test Printed-Circuit Board

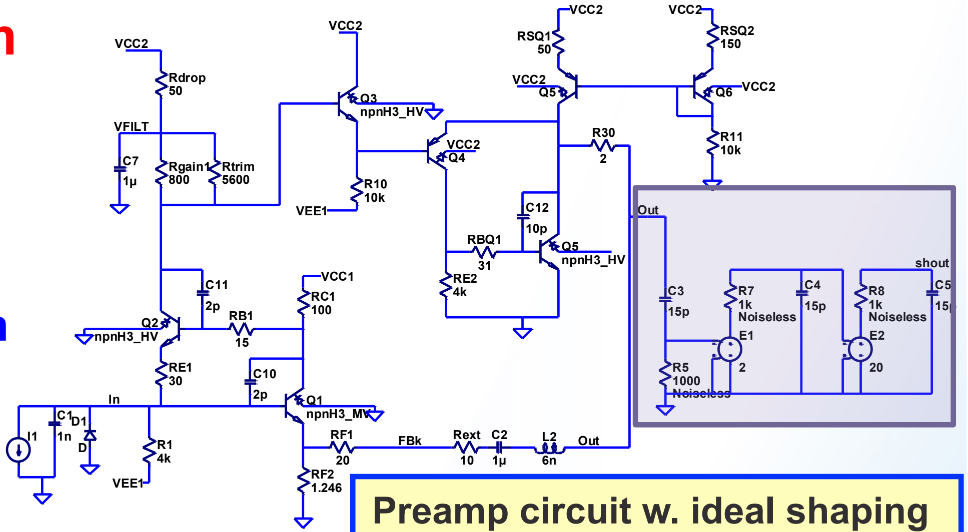




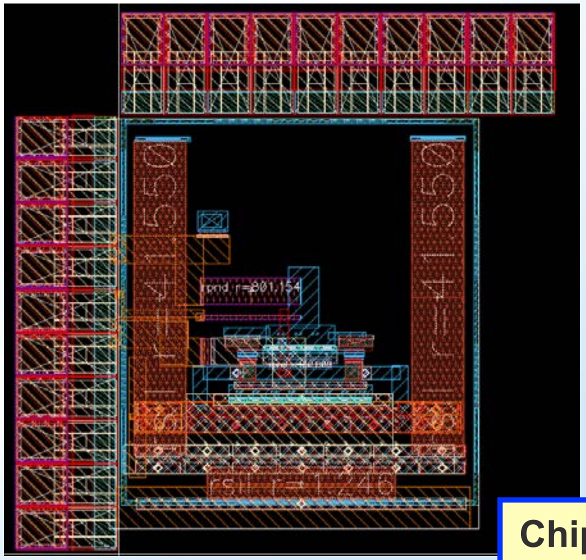
200µA peak preamp input

Analog Front-end: Preamp & Shaper

- **New design based on IHP 0.25µm SiGe SG25H3P BiCMOS process**
  - Schematics design and optimization of preamp
  - Layout preamp and simulation
  - Output driver design consideration
    - PNP: higher effective gain
    - PMOS: higher breakdown voltage
  - Two or four preamps per chip
  - Add test structures in extra space
- **Plans**
  - PNP Vceo of 2.5V vs. operating point of 3.2 to 3.7V is the only potential issue
  - Submit in one or two versions of the preamp July 2011 run to understand this issue
  - Discussion with IHP to collaborate on measurements of the radiation sensitivity of the IHP PNP transistors



Preamp circuit w. ideal shaping elements, P_{tot} ~ 45mW

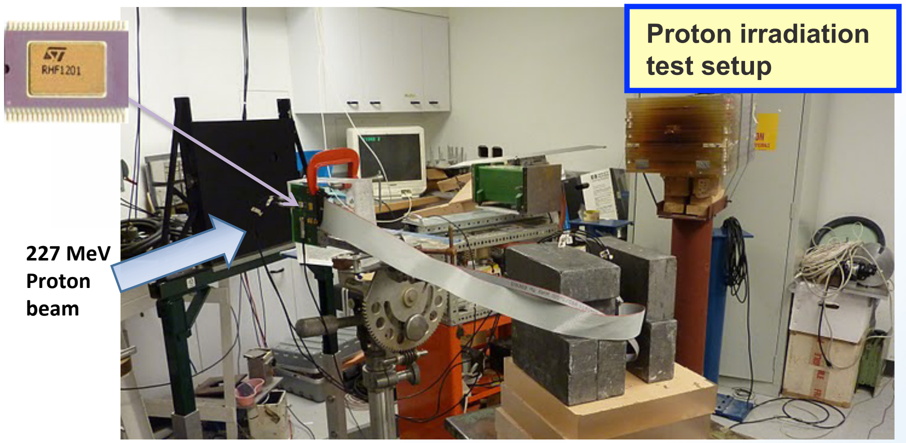


Chip layout

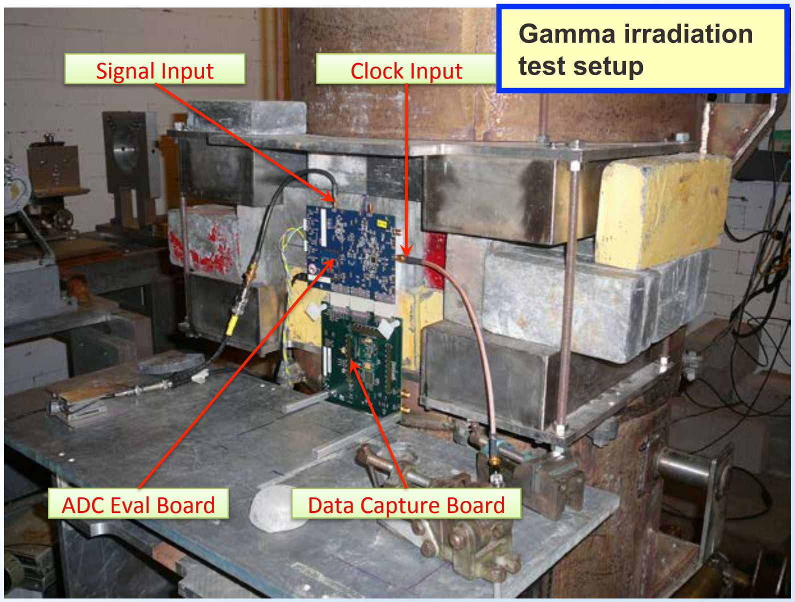
COTS ADC Irradiation Test

- **ADC is the most technologically challenging component in the new architecture**
- **COTS ADC radiation test**
  - **Verify radiation tolerance of commercial ADC**
  - **Proton irradiation test at MGH cyclotron**
    - ST-RHF1201 rad-hard 12-bit 50 MSPS ADC
    - Chip was still functioning after 1.19x10^{12} p/cm^2 at 227MeV (~1.7MRad)
    - Change of properties at 2x10^{12} p/cm^2 (~106kRad)
    - Extreme cost (~$5k list price)
  - **Gamma irradiation test at BNL**
    - Four 16-bit ADCs from Analog Devices, all of them are designed in 0.18µm CMOS technology
    - One 16-bit ADC from Linear Technology designed in 0.35µm CMOS technology
    - ADCs survived 100kRad, but died between 100kRad and 250kRad
- **No commercial ADC has been identified as a solution for the ATLAS LAr electronics upgrade**
  - **Radiation background and safety factor need to be better understood**

	Dynamic Range [bit]	Max Sampling Frequency [MSPS]	Analog Input Span [Vp-p]	Total Power CMOS per Channel at 40MSPS [mW]	Technology	Vendor	TID [kRad]
AD9265-80	16	80	2	210	0.18um CMOS	ADI	~220
AD9268-80	16	80	2	190	0.18um CMOS	ADI	~160
AD9269-40	16	40	2	61	0.18um CMOS	ADI	~120
AD9650-65	16	65	2.7	175	0.18um CMOS	ADI	~170
LTC2204	16	40	2.25	480	0.35um CMOS	Linear Tech.	~180



Proton irradiation test setup

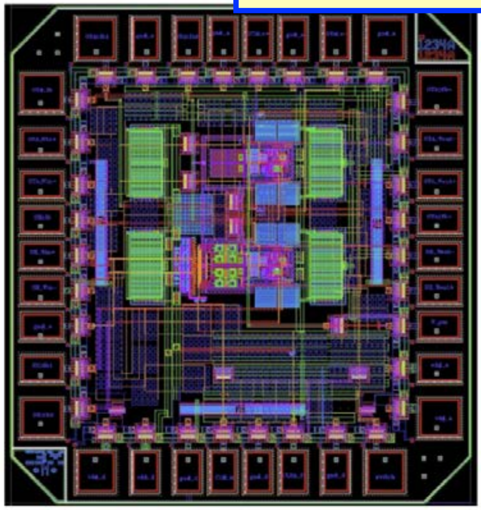


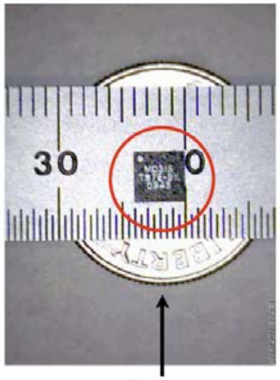
Gamma irradiation test setup

Mixed-signal ASIC: ADC Development

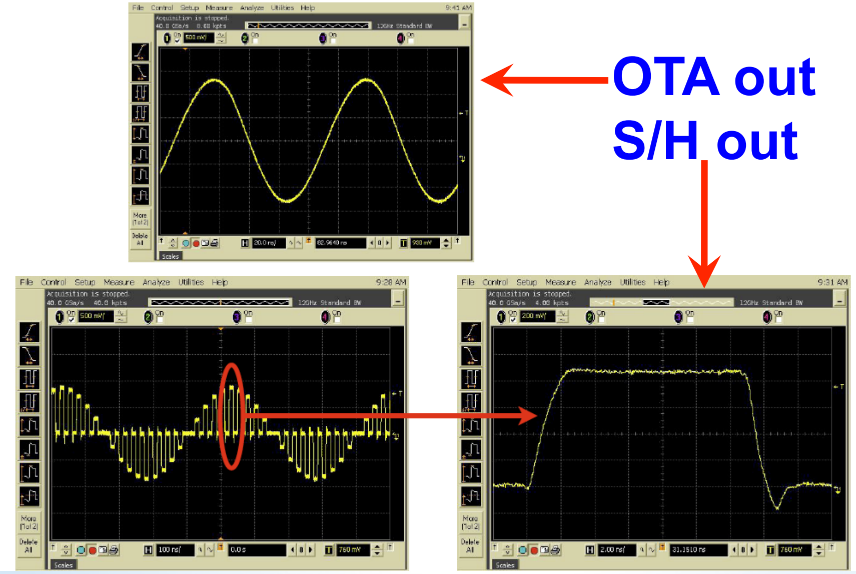
- ADC Development at Nevis
- 12-bit pipeline ADC design
  - 1.5 bits/stage with digital error correction
  - Critical component: amplifier in every stage
- Nevis09 chip
  - 12-bit precision OTA in IBM 0.13µm CMOS 8RF
  - Implemented in chip: OTA + cascade of two T/H to achieve S/H effect for testing
  - Test results: 65dB of OTA is limited by the testing environment
- Nevis10 chip
  - Two 4-stage ADC pipelines, 1.5bits/stage, gain selector structures for each pipeline
  - Delivered in Dec. 2010, test is ongoing

Nevis09 Chip

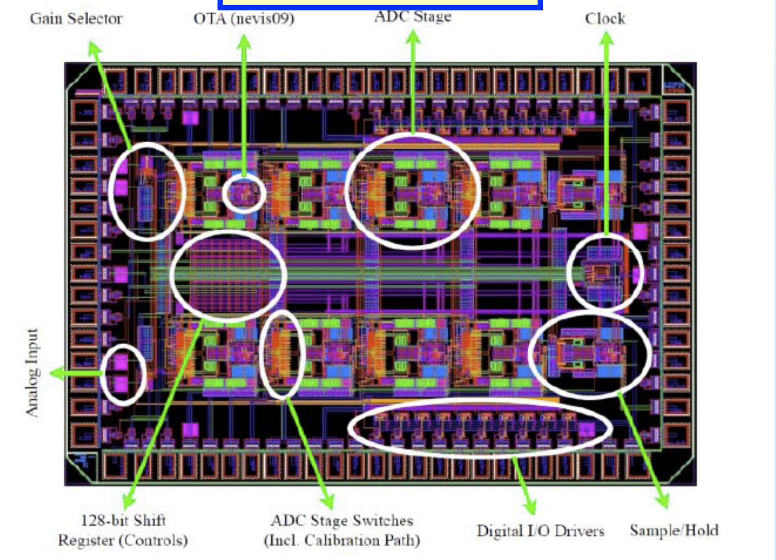




Dime
~2 euro cents
(in size)

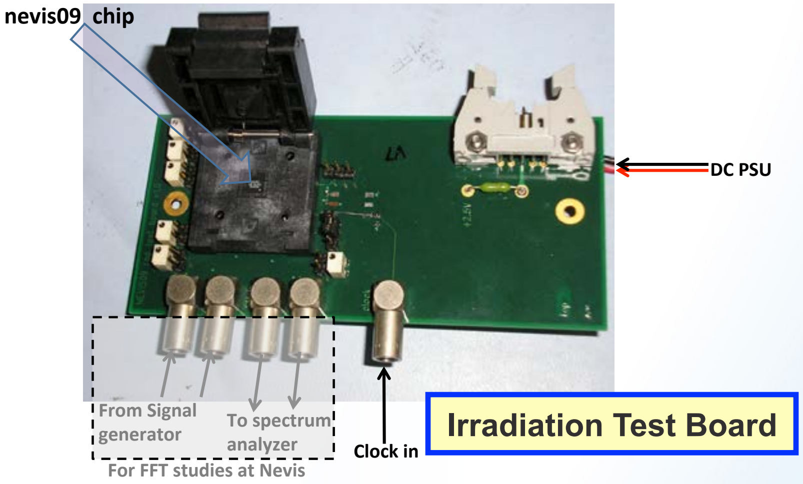


Nevis10 Chip

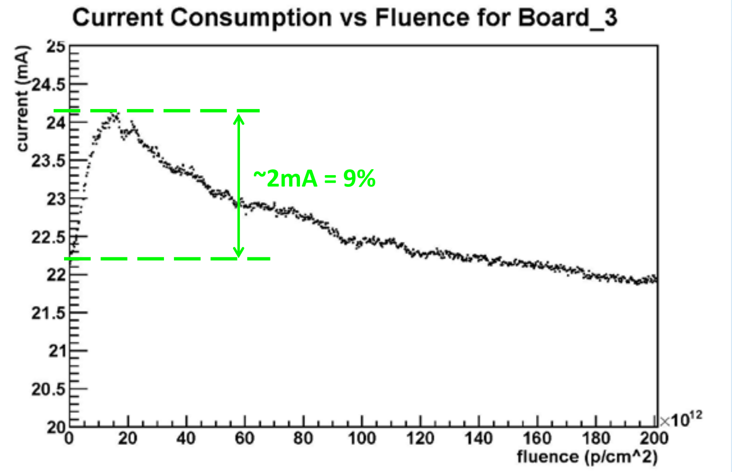


Mixed-signal ASIC: ADC Development

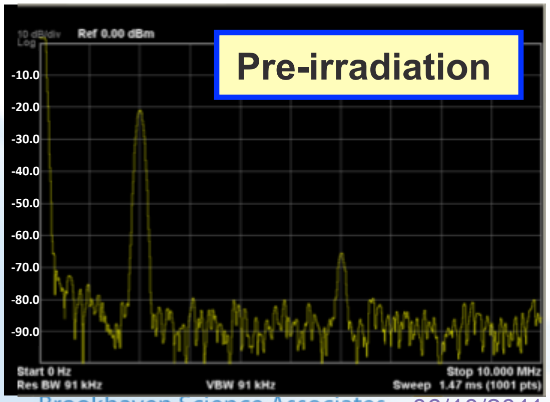
- Irradiation test of Nevis09 chip
  - Test at MGH cyclotron with proton beam
  - 5 irradiation test setups, keep one as spare/ reference
  - 2 or 10MHz sine wave input, tests in 2 input signal amplitudes
  - Pre and post-irradiation tests: FFT, output amplitude and rise/fall time studies
  - Power and clock inputs with current monitoring
  - No noticeable change in spectral analysis
  - Pre-irradiation
    - Vp-p = 1.2561V, Tr = 2.85ns, Tf = 1.73ns
  - Post-irradiation
    - Vp-p = 1.2500V, Tr = 3.40ns, Tf = 1.64ns

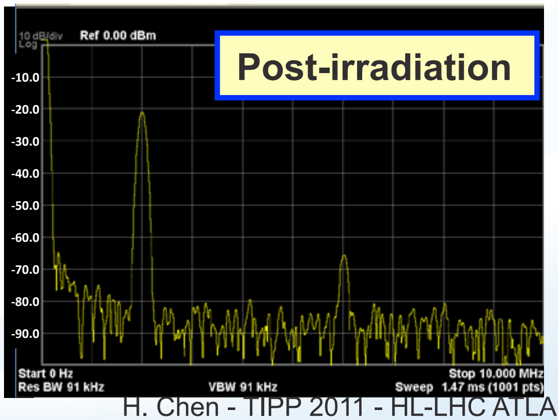


Test board	Approx . Irradiation time (min)	Total fluence delivered x10^{13} protons/cm^2
Board5	12	**2.74**
Board4	18	**5.06**
Board2	37	**10.02**
Board3	69	**20.01**



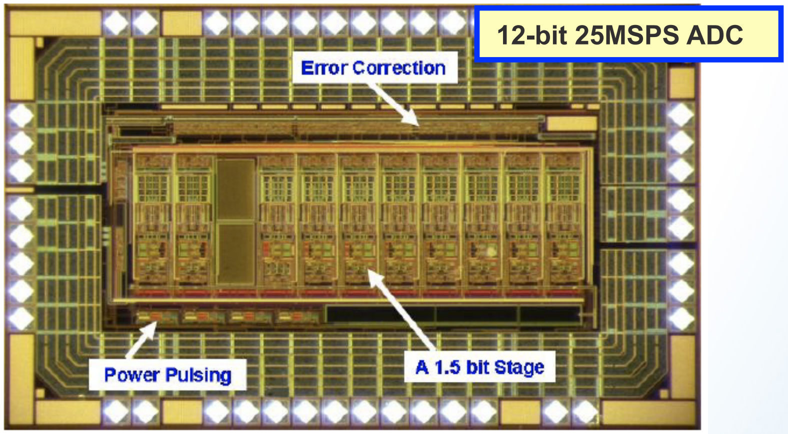
No *noticeable* change

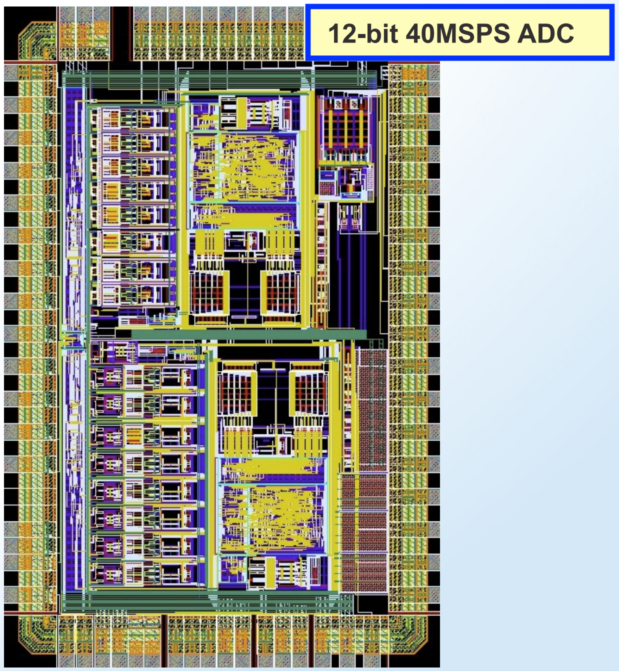


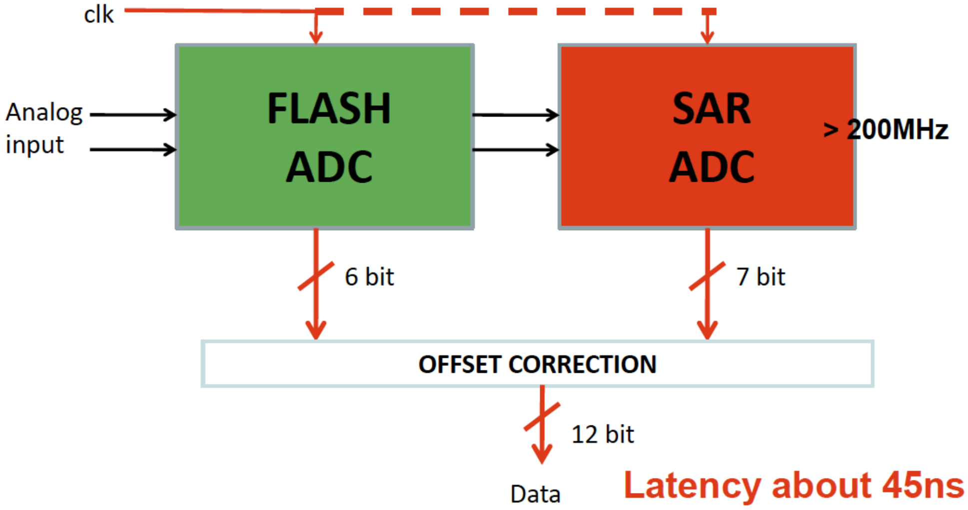


Mixed-signal ASIC: ADC Development

- ADC development at Grenoble (LPSC)
- Past development
  - Full 1.5 bits/stage @ 25MSPS
  - 12-bit pipeline ADC
  - 2-poly 4-metal .35µm CMOS technology
  - Embedded as IP on NECTAR0 chip for CTA collaboration
- Roadmap to pipeline 40MSPS ADC design
  - Increasing the number of bit/stage
  - improve the bandwidth up to 40MHz
  - Use Dynamic Element Matching (for capacitors) for analog linearity correction
  - Research is going on digital correction
  - Reduce C value to ease amplifier design
  - Use more 2.5 bit MDAC stages
  - More bits in the last stage 4 bits (flash)
  - Expected latency 100ns
- To get better latency
  - Pipeline ADC has intrinsic more latency
  - Study new low latency ADC architecture: Flash-SAR ADC



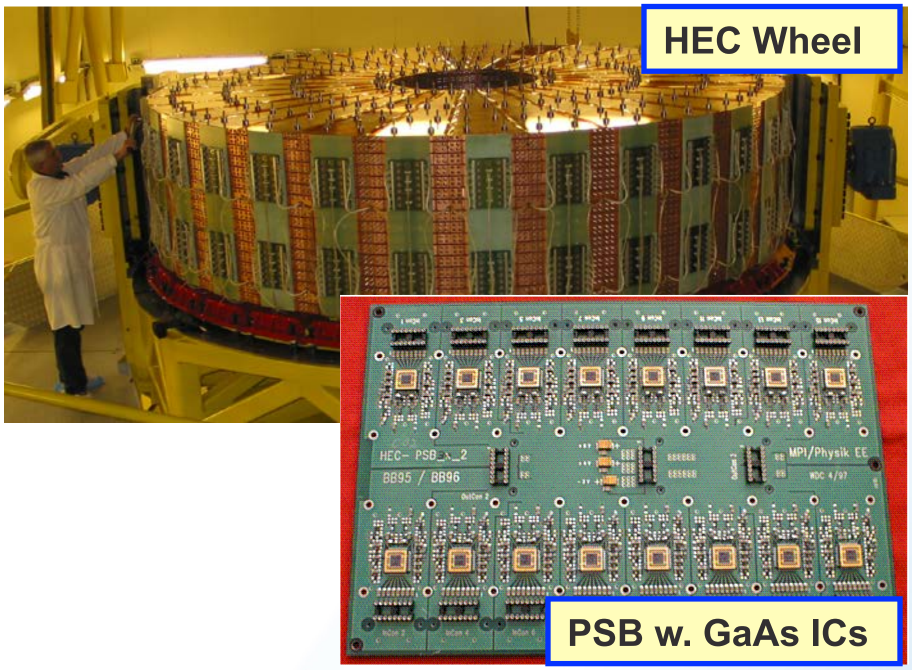




Latency about 45ns

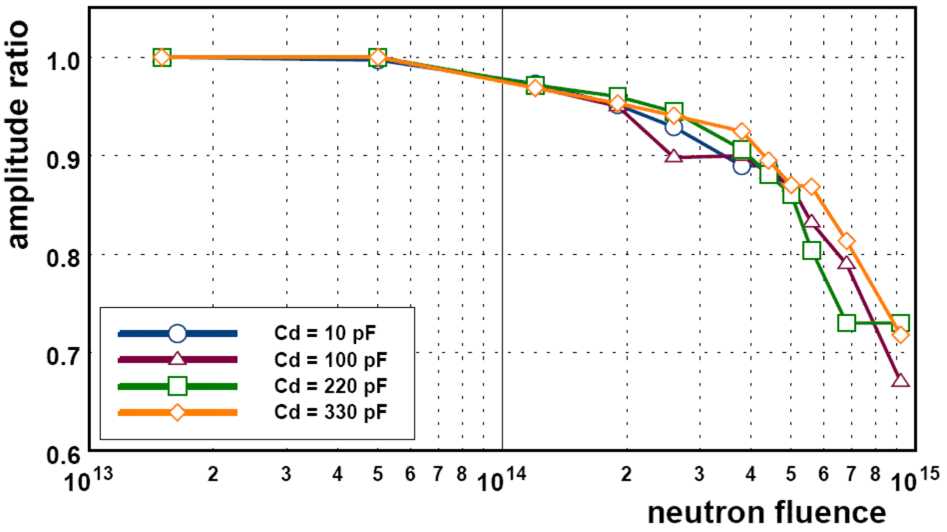
HEC Cold Electronics

- **PSB boards with ICs are mounted at the outer circumference of the HEC wheels**
- **GaAs IC**
  - 8 preamp channels, 2 summing amplifiers, operating in LAr to provide optimal SNR
  - TriQuint QED-A 1μm technology, excellent high frequency performance, stable operation at cryogenic temperatures, radiation hardness
  - Degradation of performance sets in at typically 3x10^{14}n/cm^2 while neutron fluence of 10 years ATLAS operation is 0.2x10^{14}n/cm^2
- **HEC cold electronics R&D plans**
  - New and more radiation hard ICs
  - Radiation hardness up to neutron fluence of few 10^{15} n/cm^2
  - Lower power consumption, < 200mW
  - Low noise, low gain variation, safe with respect to potential HV discharges



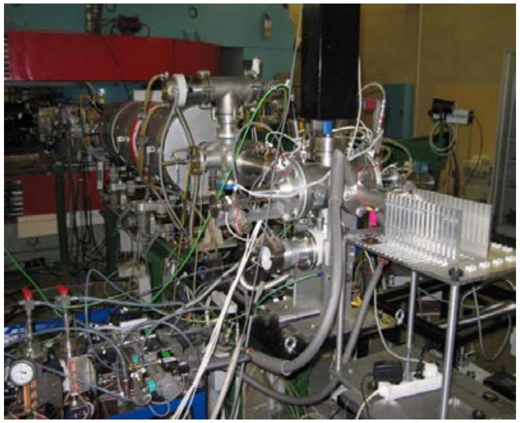
HEC Wheel

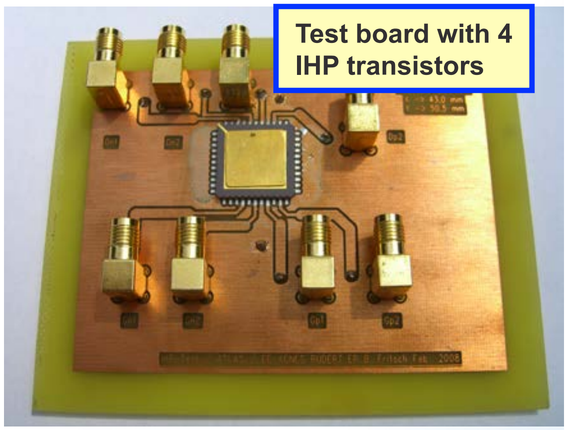
PSB w. GaAs ICs



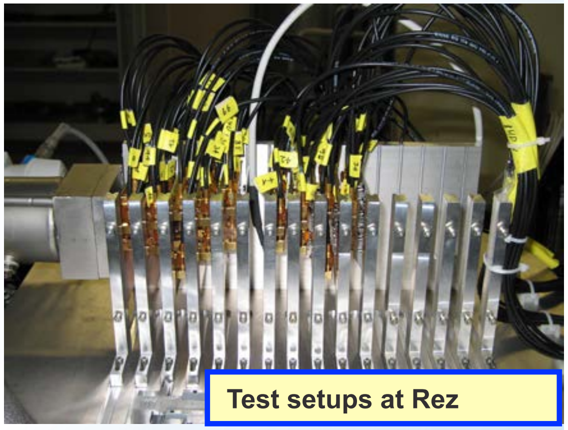
HEC Cold Electronics

- Radiation hardness against neutron irradation has been studied for transistors of SiGe, Si and GaAs technologies
    - Neutron irradiation test at NPI at Rez
    - Measuring DC values and S-parameters
    - Measuring during neutron irradiation
- Technology selection
    - IHP CMOS (better temperature stability) with backup solutions of IHP SiGe Bipolar and IBM SiGe Bipolar
    - Develop simulation models to include radiation and low temperature effects
    - Plan to perform proton irradiation at PSI in Zurich, and gamma irradiation at Rez
    - Design of simple preamp chip (IHP-CMOS) has been done





Test board with 4 IHP transistors



Test setups at Rez

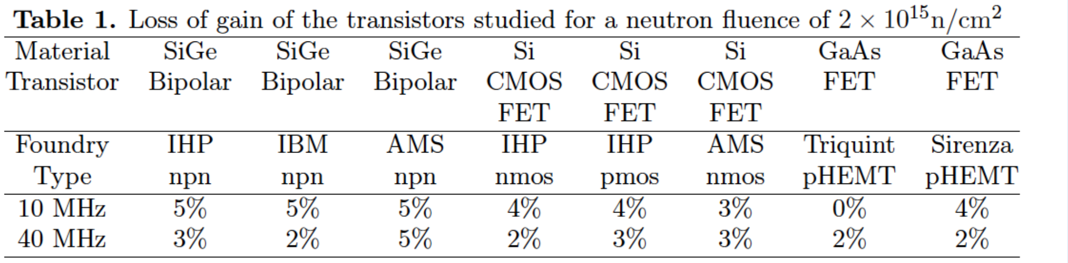
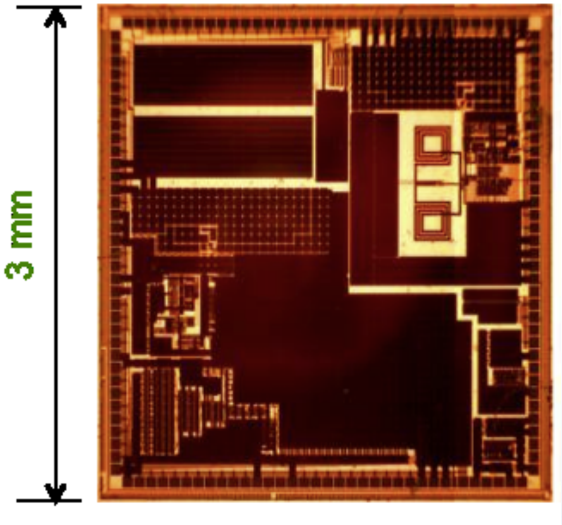


Table 1. Loss of gain of the transistors studied for a neutron fluence of $2 \times 10^{15} n/cm^2$

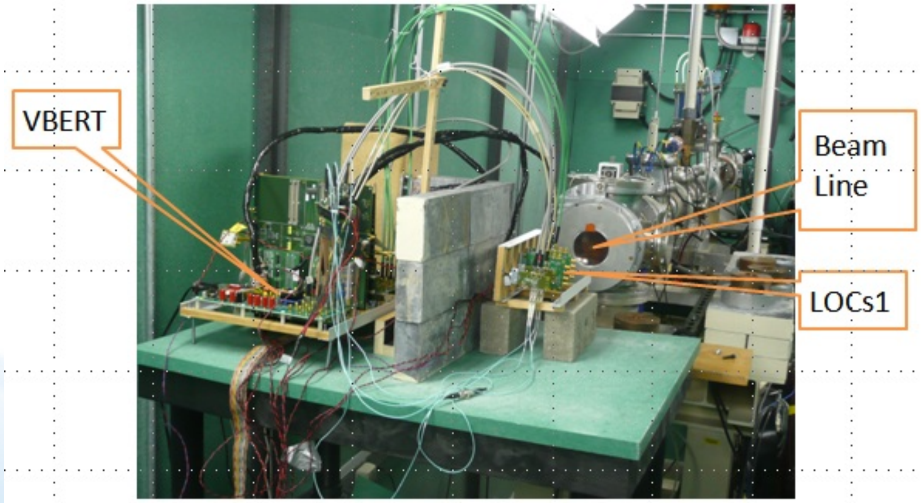
Material Transistor	SiGe Bipolar	SiGe Bipolar	SiGe Bipolar	Si CMOS FET	Si CMOS FET	Si CMOS FET	GaAs FET	GaAs FET
Foundry	IHP	IBM	AMS	IHP	IHP	AMS	Triquint	Sirenza
Type	npn	npn	npn	nmos	pmos	nmos	pHEMT	pHEMT
10 MHz	5%	5%	5%	4%	4%	3%	0%	4%
40 MHz	3%	2%	5%	2%	3%	3%	2%	2%

Radiation Tolerant Optical Link

- **SMU_P1 in 0.25μm Silicon-on-Sapphire consists of the following function blocks**
  - LOCs1, a 5Gbps 16:1 serializer
  - The LCPLL, a 5GHz LC VCO based PLL
  - The CML driver
  - A divide-by-16 circuit
  - A varactor, a voltage controller capacitor
  - An SRAM block
- **LOCs1 test results**
  - T_j ~ 62ps, eye opening ~ 69% UI at 1e-12
  - Jitter tolerance is larger than 1.8 UI when jitter frequency less th 1.56MHz
- **LOCs1 irradiation test at IUCF**
  - 200MeV proton beam at IUCF
  - SEE: the extrapolated BER at HL-LHC LAr is much less than 10^{-12}
  - TID: chips functioning well, no bit error observed, total power current changes less than 6%

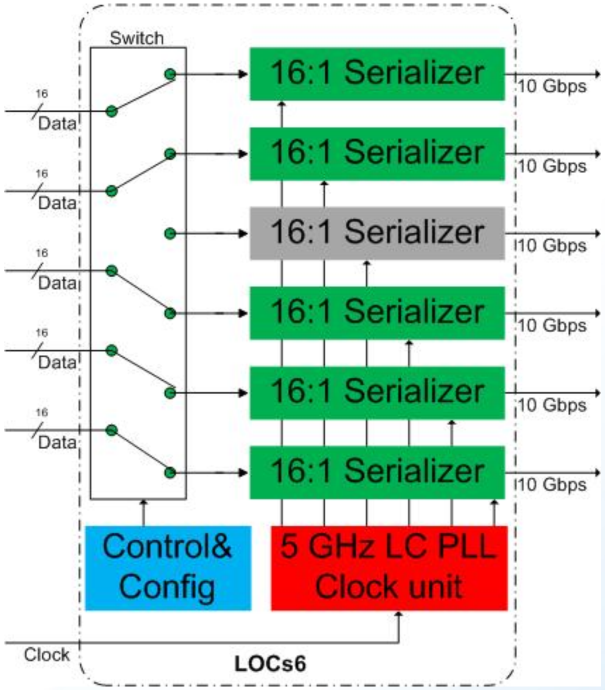


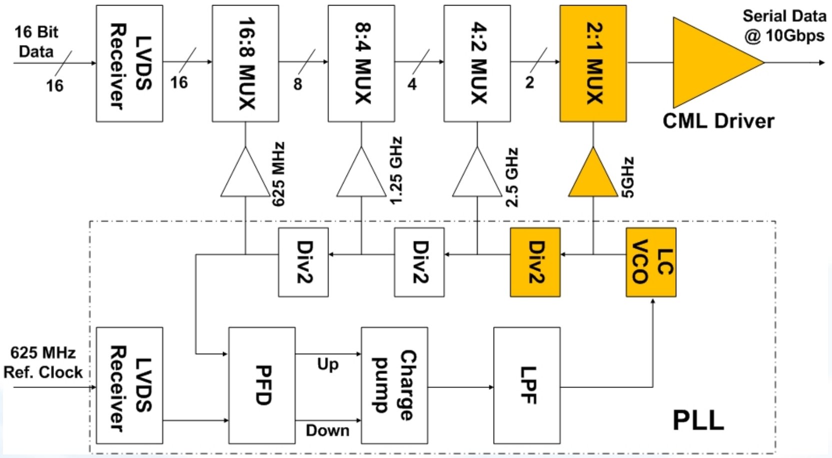
Amplitude (V)	1.16 ±0.03
Rise time (ps)	52.0 ±0.9
Fall time (ps)	51.9 ± 1.0
Total Jitter @ BER 10^{-12} (ps)	61.6 ± 6.9
Random Jitter (ps)	2.6 ±0.6
Total DJ (ps)	33.4 ±6.7
DJ: Periodic (ps)	3.0 ± 2.3
DJ: ISI (ps)	3.0 ± 2.3
DJ: Duty cycle (ps)	15.2 ± 3.8

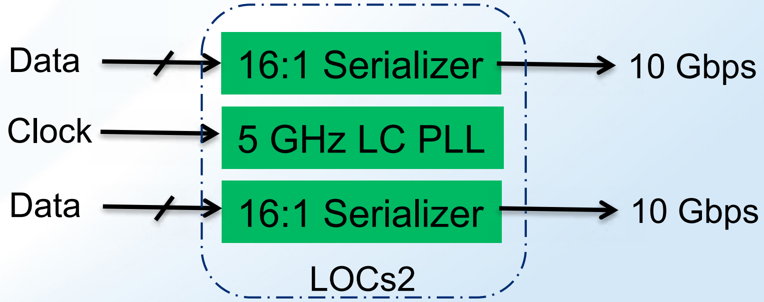


Radiation Tolerant Optical Link

- **Second version LOC design**
  - Initial 6-lane design LOCs6 is not feasible due to difficulties in the 5GHz clock fanout over the whole chip
  - Step back to LOCs2: a 2-lane shared LC PLL serializer array
  - New Silicon-on-Sapphire CMOS process may allow to go back to LOCs6
- **LOCs2 design**
  - Focus on the fast (CML) parts in the design
  - Limitation of 8Gbps on GC process, new 180nm PC process will get it to 10Gbps
  - Design is based on the GC process, will decide on whether prototype GC design or move the PC design



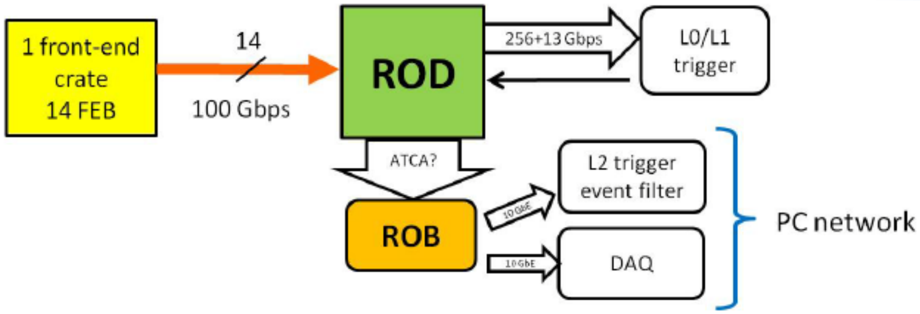


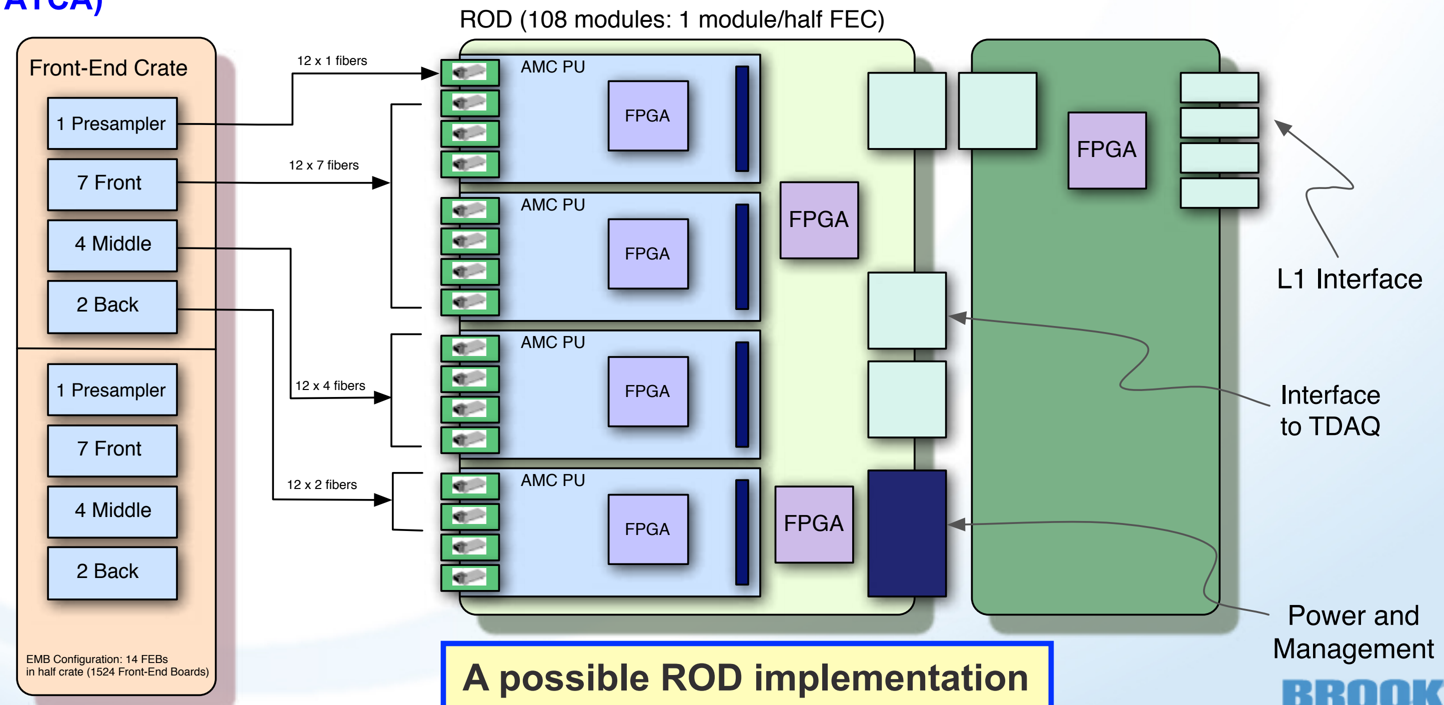


See Tiankuan Liu's TIPP2011 talk for more details

Readout Driver (ROD) Upgrade R&D

- **Data bandwidth of entire LAr w. 1524 FEBs > 150Tbps**
  - **High speed parallel fiber optical transceiver (e.g. 12 fibers @ 10Gbps)**
- **ROD R&D**
  - **Address issues of bandwidth and achievable integration on the ROD**
  - **ROD based on FPGA high speed SERDES and FPGA based DSP to take advantage of parallel data processing**
  - **Perform L0/L1 trigger sum digitally after E-conversio with flexible and finer granularity within a realistic latency budget**
  - **Follow up and explore technology evolution (e.g. FPGA, ATCA)**





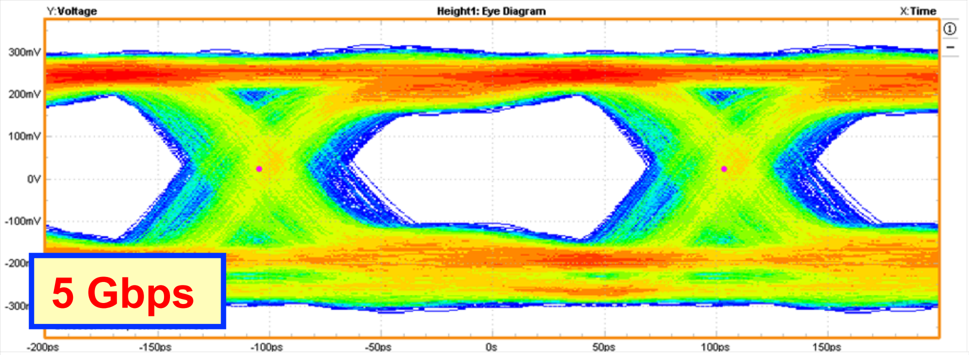
A possible ROD implementation

ATCA Sub-ROD Development

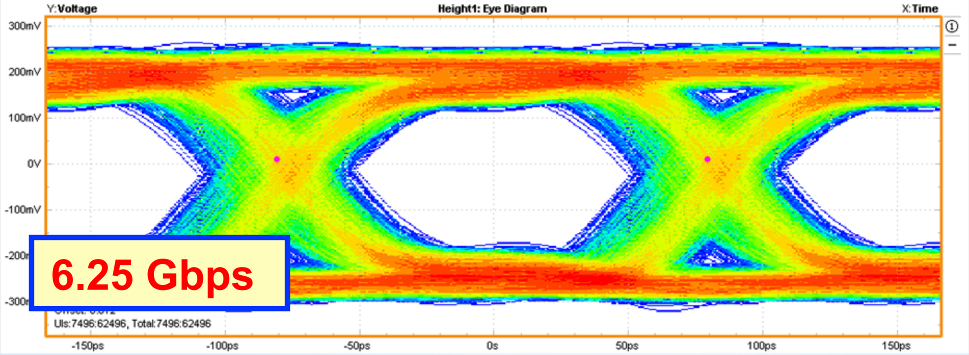
- **Sub-ROD and Injector in US**
  - ATCA form factor
  - 75Gbps parallel fiber optic links
  - FPGA SERDES: Xilinx Virtex 5 FX on Sub-ROD and Altera Statix II GX on Injector
- **Slice integration test**
  - SNAP-12 parallel optical transceiver from Emcore and Reflex Photonics
  - BERT from 2.4 to 6.25Gbps per link
  - Used as test stand for latency study and firmware development for interface to ROS

ATCA Sub-ROD

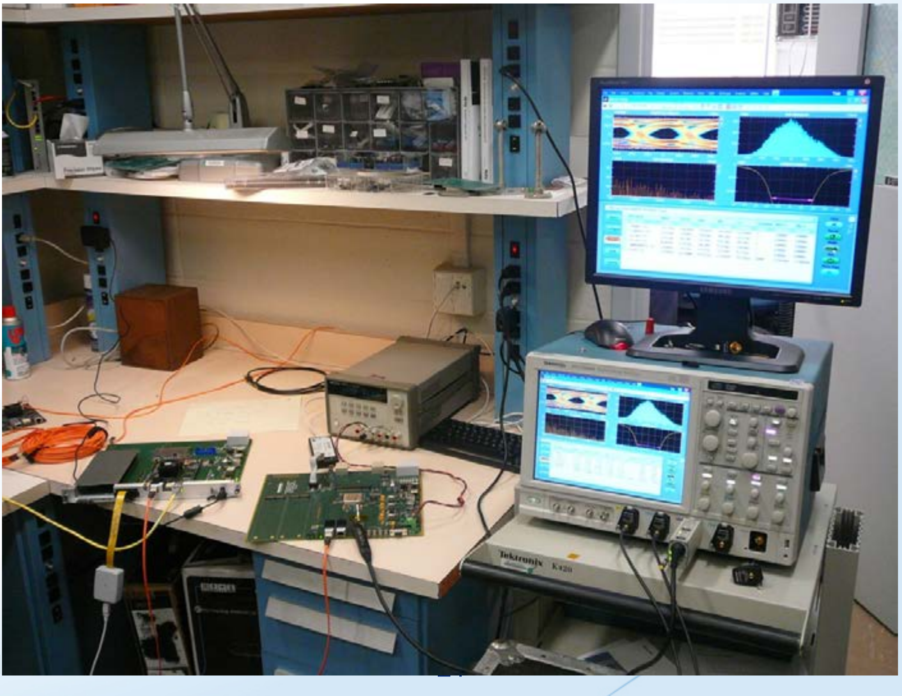
Sub-ROD Injector



5 Gbps

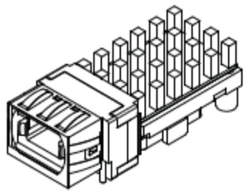


6.25 Gbps

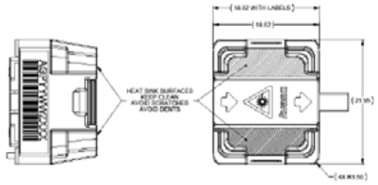


AMC Sub-ROD Development

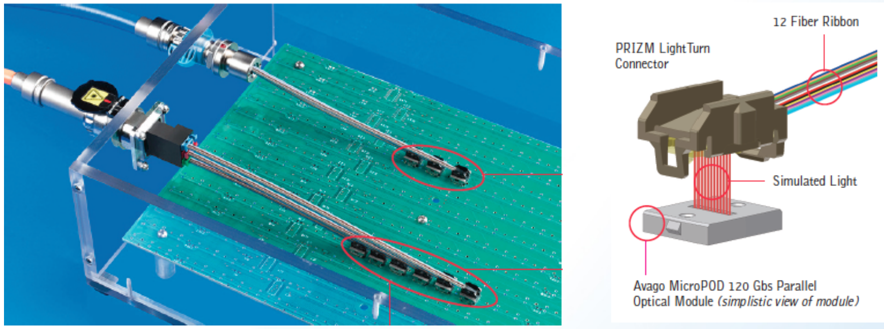
- AMC format Sub-ROD can be tested in a low cost MicroTCA crate or on an ATCA carrier board
- Package of Optical Transceivers
  - Avago SNAP-12: 41.07x17.5mm
  - Avago MiniPod: 18.62x21.95mm
  - Avago MicroPod: 7.8x8.2mm
- AMC Sub-ROD
  - Xilinx Virtex 7 FPGA (XC7VX485T) @ 12.5Gbps
  - MMC (Module Management Controller) is based on ARM processor for IPMI
  - Precision clock circuitry and DC-DC converters for power management
  - Avago MiniPod optics (12x10Gbps)
  - Versatile interface through AMC edge connector
- AMC Sub-ROD Injector
  - Altera Stratix V (5SGXMA5N1F40C2) @ 14.1Gbps
  - 5 power supplies and 1 filter
  - Avago surface mount MicroPod optics(12x10Gbps)
  - Up to 8 Xmit and/or Recv MicroPods



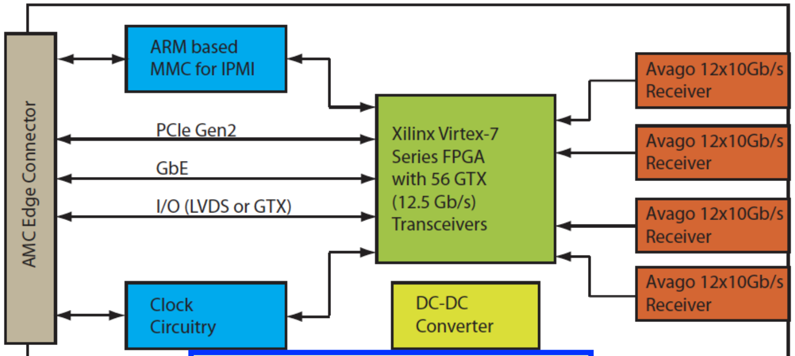
SNAP-12



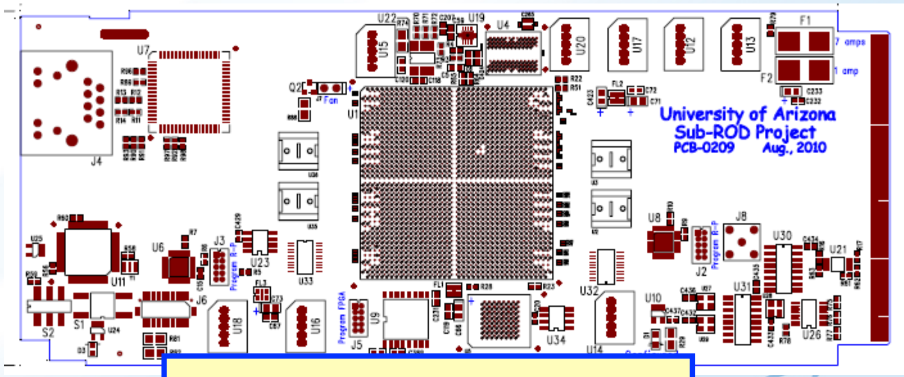
MiniPod



MicroPod w. Molex PRIZM LightTurn cable assemblies



AMC Sub-ROD

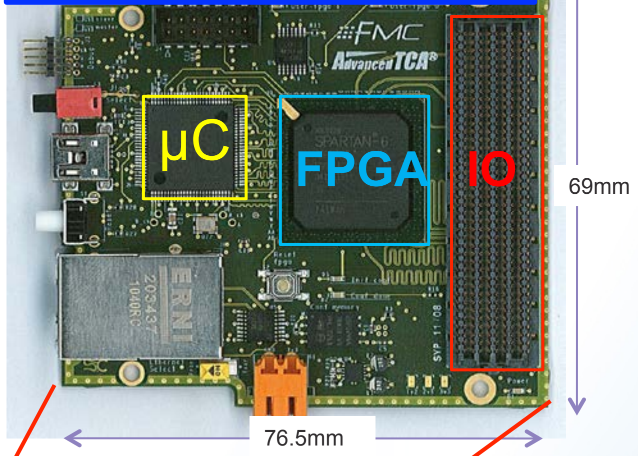


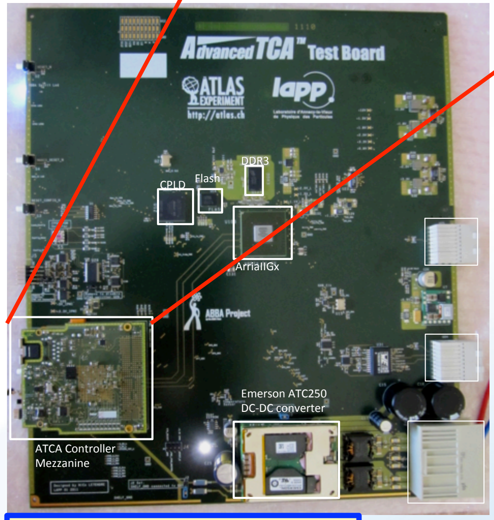
AMC Sub-ROD Injector

ROD R&D in ATCA Platform

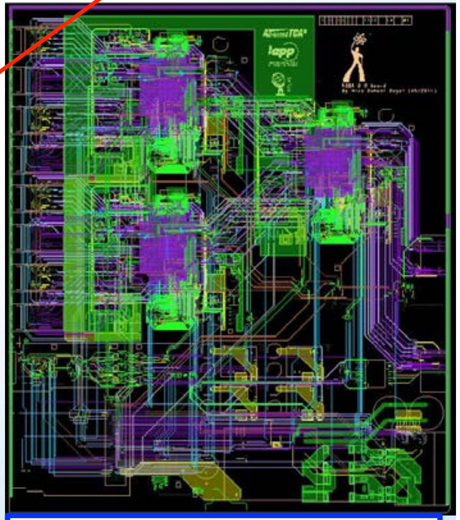
- **ATCA development for the ROD upgrade in LAPP, France**
- **ATCA Controller Mezzanine**
  - IPM controller for communication with shelf manager, hot swap, power management etc.
  - ATCA board management via Ethernet for firmware upgrade, ATCA board monitoring, configuration etc.
  - FMC compliant, low cost
  - Features ARM Cortex M3 processor and Xilinx Spartan 6 FPGA
  - Software development compliant with IPMI 2.0 specification
- **ATCA Test Board**
  - Check board configuration with the ATCA Controller Mezzanine
  - Test ATCA compliant power supplies
  - Check FPGA design for ROD Evaluator (communication with DDR3, Flash, configuration with Flash)
- **ROD Evaluator Board**
  - 3 ALTERA STRATIX IV with 48 transceivers at up to 8.5Gbps
  - 48 injector channels on 4 AVAGO SNAP12 (4 FEBs)
  - 48 receiver channels on 4 AVAGO SNAP12 (4 FEBs)
  - 16 bidirectional on board channels between FPGAs
  - 1 port ATCA update interface and 3 ports ATCA fabric interface
- **Tests with commercial boards**
  - Software framework
  - 10GbE communications between blades
  - Front (via AMC): TCP 5.4Gb/s, UDP 5.6Gb/s
  - Zone 2 (fabric interface): TCP 8Gb/s, UDP 6.8Gb/s

ATCA Controller Mezzanine





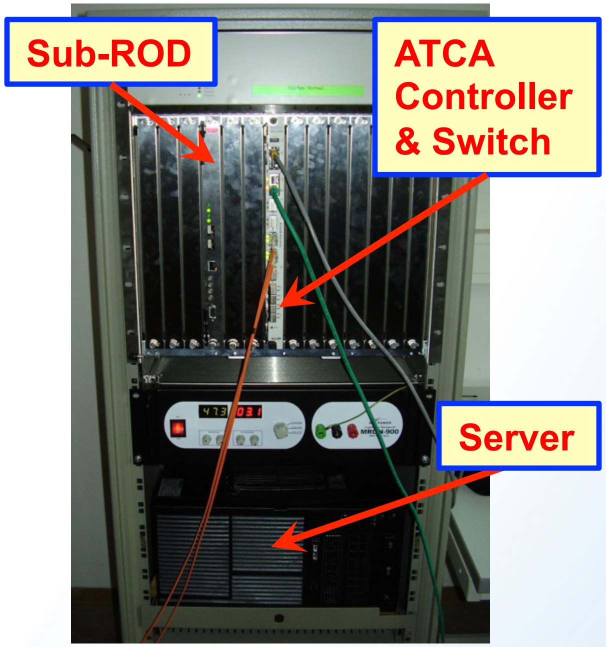
ATCA Test Board



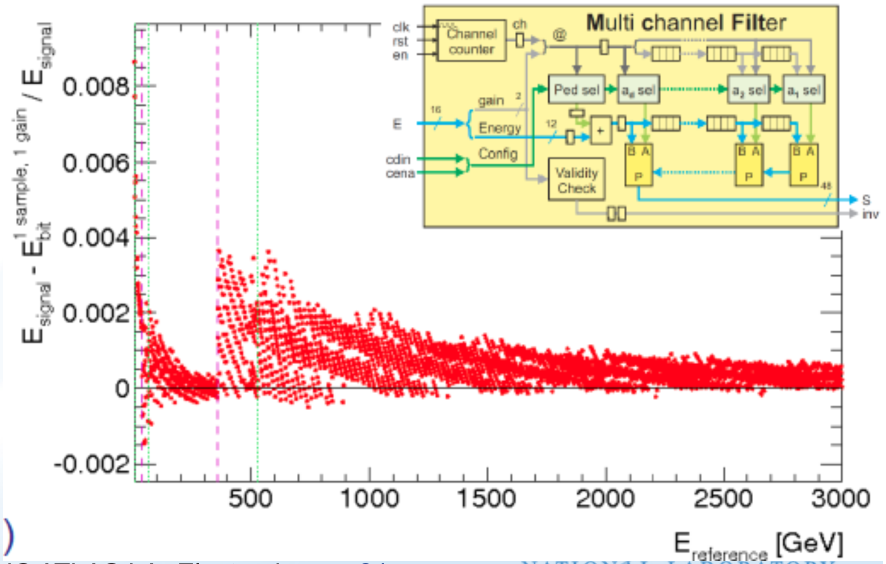
ROD Evaluator Board

ROD R&D in ATCA Platform

- **ATCA ROD test bench in Dresden, Germany**
  - Radisys Promentum ATCA sys-6010 crate with 10GbE and dual star backplane
  - 1 ATCA Sub-ROD from BNL
  - 10GbE Switch with XFP transceiver with 10GbE connection to server PC
  - Installation of ROS software to simulate real data transfer and DAQ system as in ATLAS
  - Fast 10GbE link from ROD to ROB, 10 GbE XAUI interface implemented
  - ROB server with 4 Myricom 10 GbE dual power NICs, performance reached: 79 Gbps @ 30% CPU load

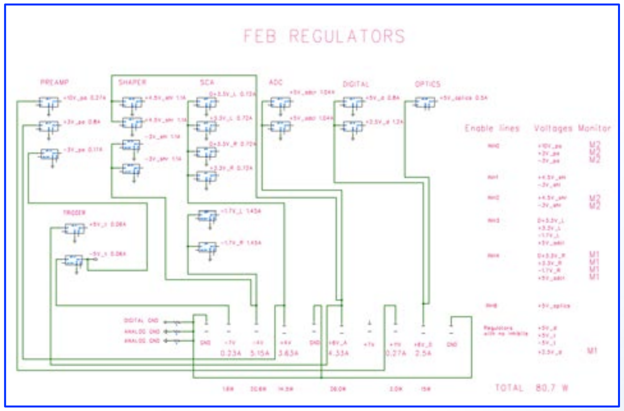


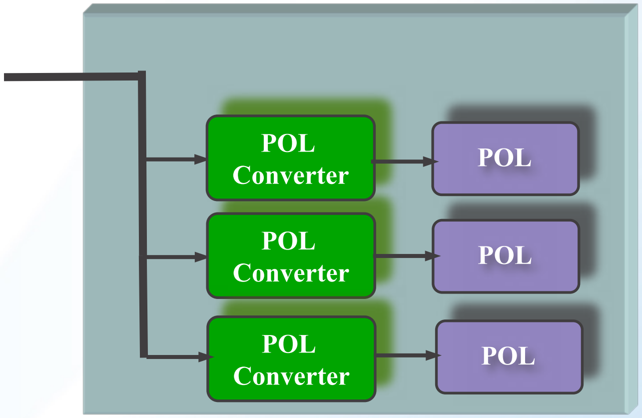
- **FPGA firmware development**
  - Digital signal filter designed with minimal latency (3+2 FPGA clock cycles)
  - Filter operates up to 350MHz in Virtex-5 FPGA
  - Dynamic loading of calibration constants without FPGA firmware update
- **Simulation of free-running readout with software**
  - e.g. different gains for each of samples (noise, pile-up dependent filter coefficients, …)

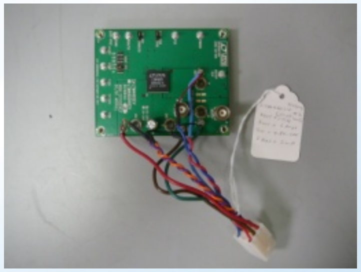


Radiation Hard Front End Power Supply

- **Present power supply scheme**
  - 380 VAC/3 phases → 280 VDC → Rad-tolerant DC-DC converters w. 7 voltages → 19 regulators on FEB
- **Upgraded power supply system**
  - Radiation environment assumed to scale x10
  - Power budget remains approximately the same
  - Rationalization of the number and levels of the voltages
  - Use of point of load converters
- **Two possible architectures**
  - Distributed power architecture: main DC-DC converter + POL converters
  - Intermediate bus architecture: main DC-DC converter + 2nd bus voltage w. POL converter + LDO regulator
- **Two POL converters tested in FEC for noise evaluation**
  - LTM4602: 6A High Efficiency DC/DC μModule
  - IR3841: Integrated 8A Synchronous Buck Regulator
  - Noise shielding necessary if inside FEC
  - Irradiation tests to be done

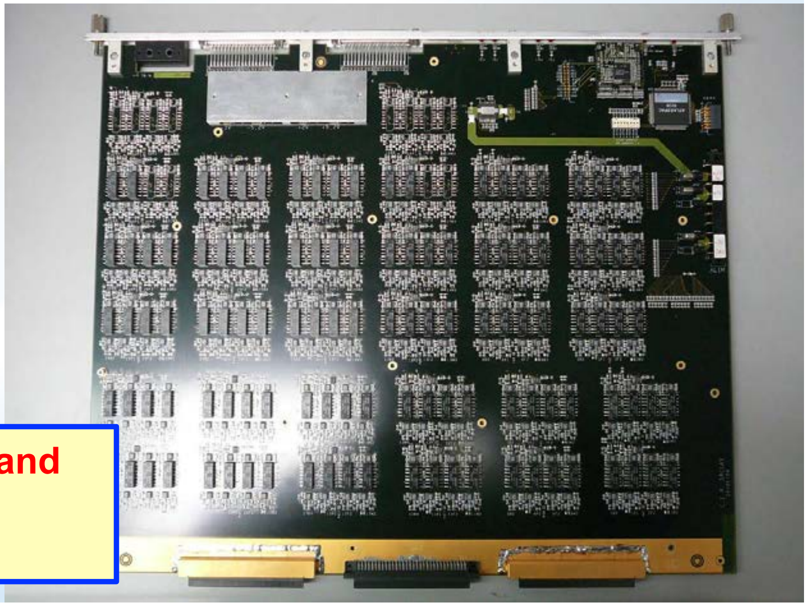






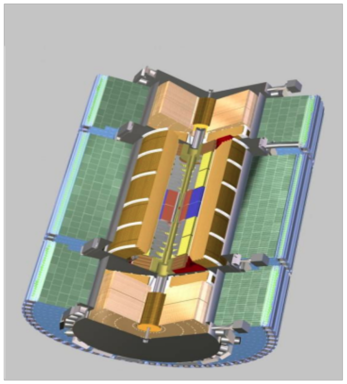
Evolution from Today to HL-LHC

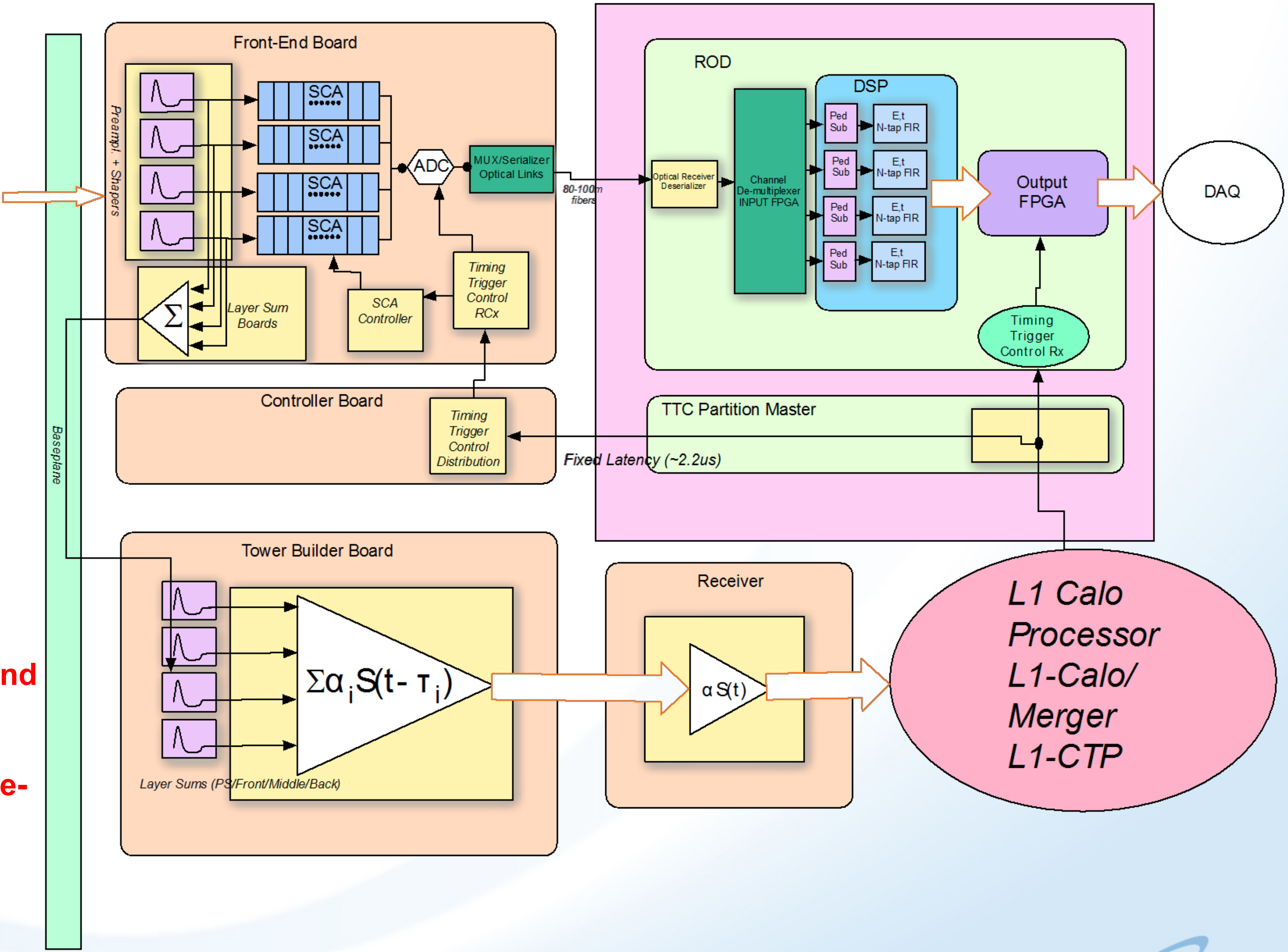
- **Introduction of one or more intermediate upgrade steps before full replacement of LAr readout electronics in HL-LHC**
- **Step1: demonstrator system in 2013/14**
  - **Option 1: replace Tower Builder Board (TBB) with a new, mixed analog/digital version**
    - **Analog signal sums and trigger output identical to today's TBB**
    - **Plus: digitization of sums of the 4 individual LAr layers (layer sums are performed by Layer Sum Board)**
    - **$\Delta\eta \times \Delta\varphi$ segmentation as today, but improved granularity in depth → sent via new ROD to L0/L1Calo demonstrator**
  - **Option 2: equip special FEB boards with new digital electronics**
    - **Sent via new ROD to L0/L1Calo demonstrator**
- **Step 2: potential extended system in phase-1 upgrade**
  - **TBB replacement in a larger detector area**
  - **Possibility of implementing global object searches through the full calorimeter in the early trigger phases**



Tower Builder Board (TBB) sums and reshapes layer sums, includes programmable delay line

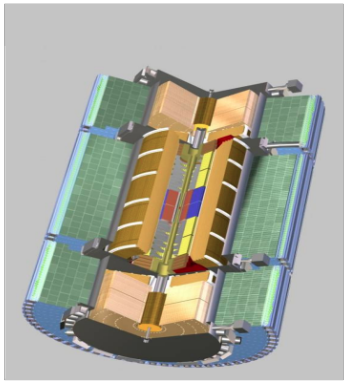
Current Architecture

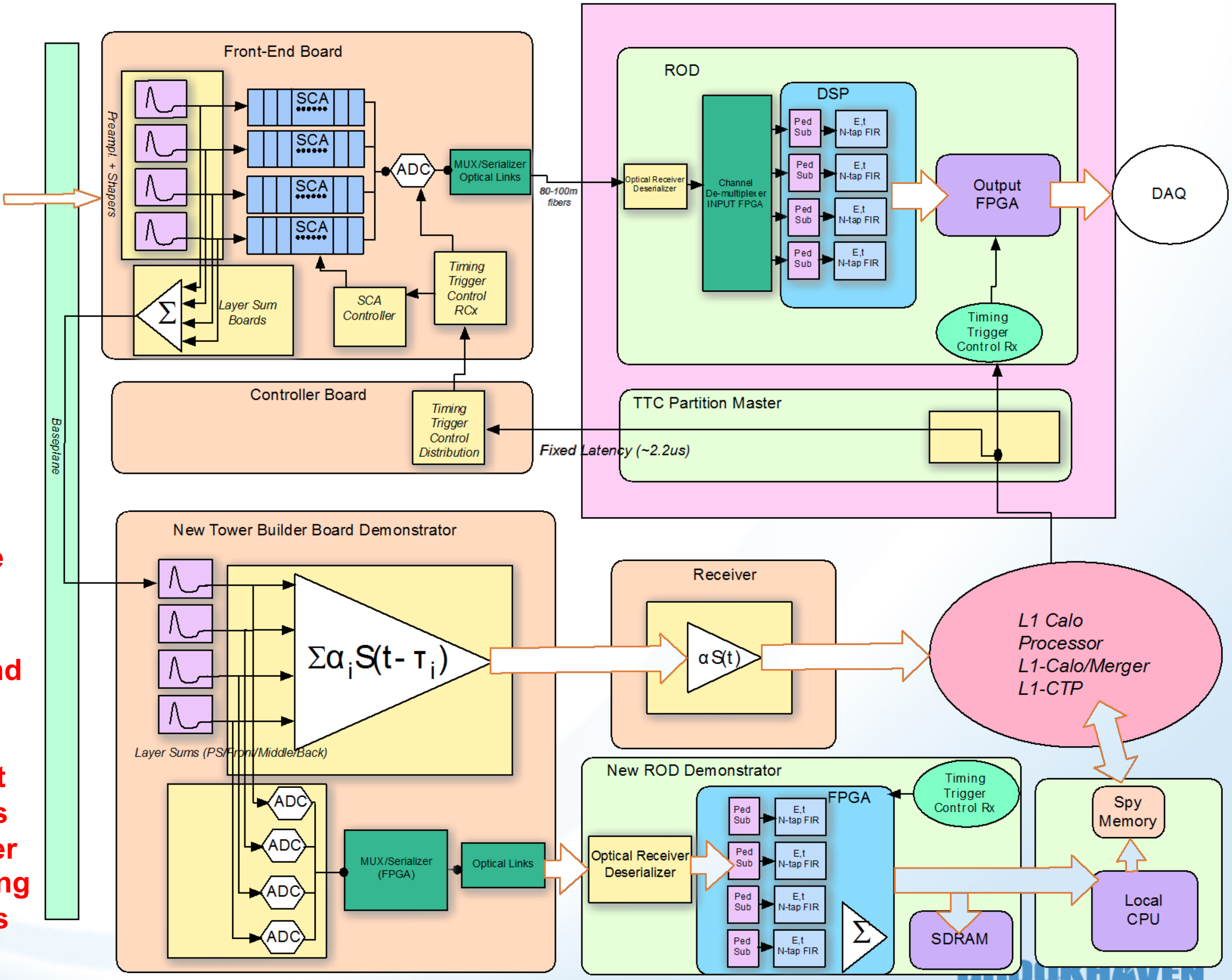




- **Analog trigger tower signals sent to L1Calo through TBB and Receiver, digitization happens on Pre-processor**

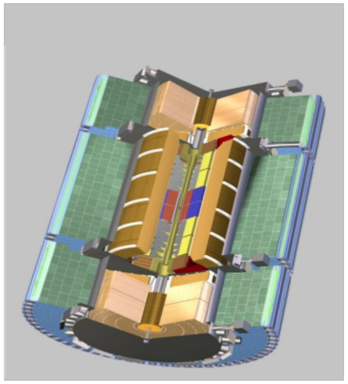
Idea for Demonstrator System

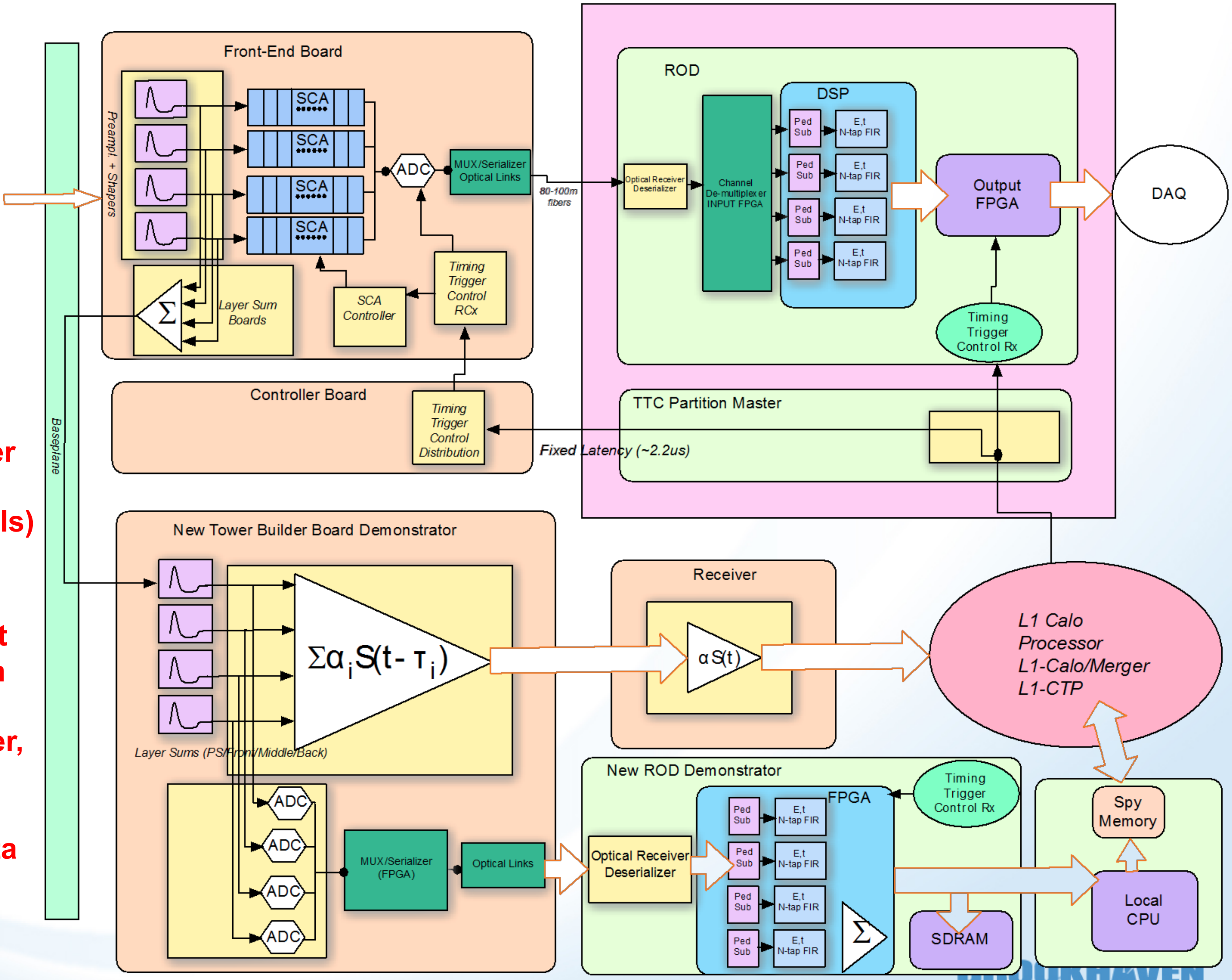




- **Phase 0: ~3k channels max, 0.4x0.4 are on one side of the barrel calorimeter**
- **Phase-1: extend to the full calorimeter trigger readout (~20k channels max), L1 trigger potentially using digitized layers**

Possible Extension of Architecture at HL-LHC

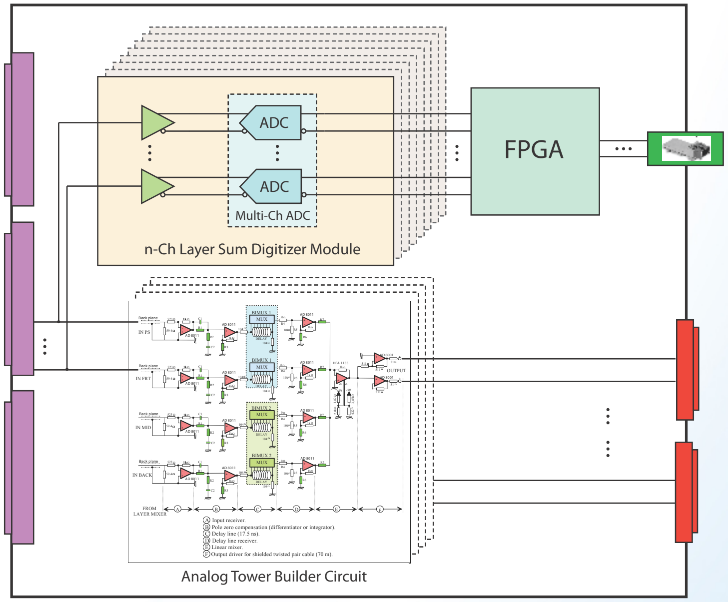


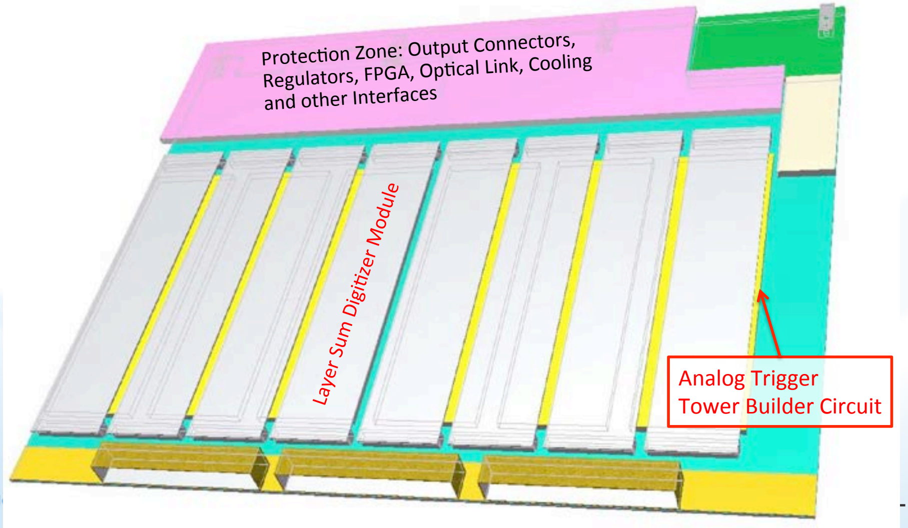


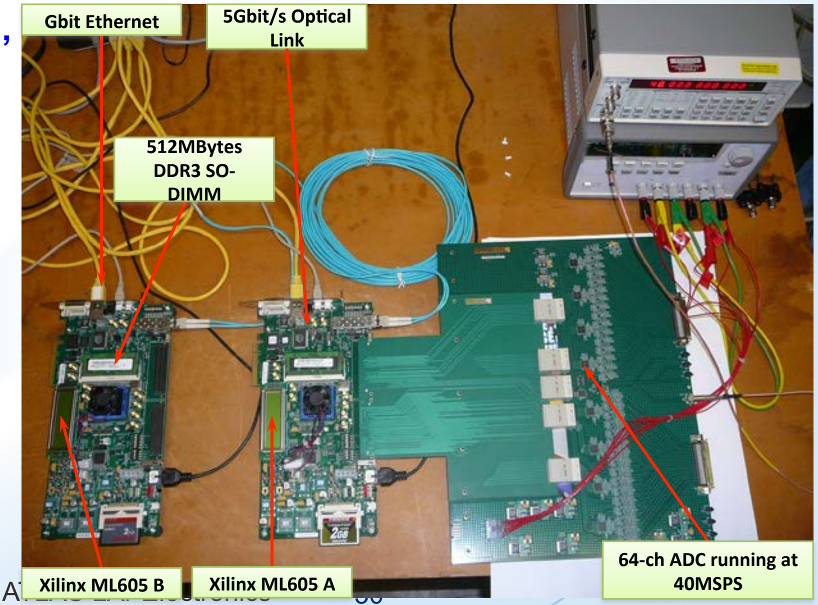
- **Full calorimeter digital readout (~200k channels)**
- **Calorimeter trigger may evolve in a fast L0 trigger from digitized layer and a L1 trigger, which uses higher granularity data**

Digital Tower Builder Board

- **Digital TBB**
  - **Preserve full analog TBB functions and mechanical/ electrical interfaces**
  - **Take analog input signals from input connectors to minimize interference to analog trigger tower builder chain**
  - **Digital output is sent to USA15 through fiber optical link**
  - **Digital layer sum preparation, modular design is preferred**
- **Electrical Studies**
  - **Data from 4 ADC channels transferred over 5Gbit/s optical link to second Xilinx ML605 board, and stored in DDR3 memory, then transfer to PC over the Gigabit Ethernet**
  - **ADC board with ML605 “A” demonstrates the digital TBB, while ML605 “B” demonstrates the TBB ROD**
  - **Data flow test with optical link has been done**
- **Mechanical Studies**
  - **Modular design of Layer Sum Digitizer mezzanine card, and FPGA/optical link mezzanine card**





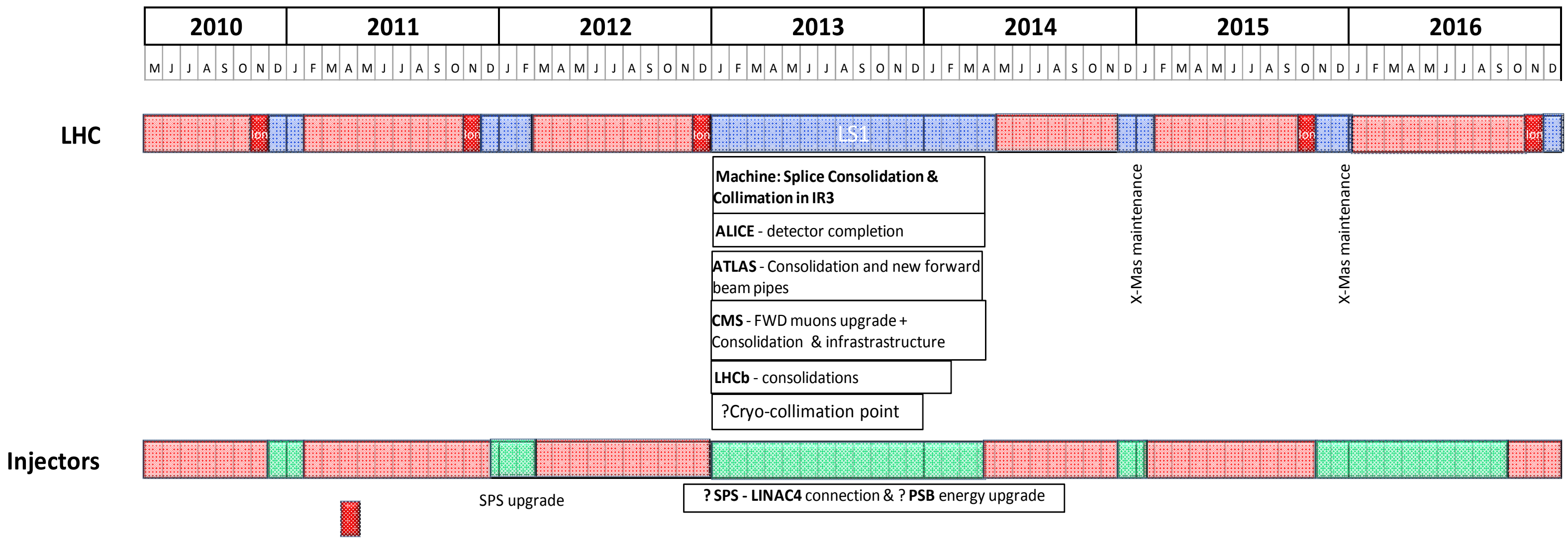


Summary

- Radiation tolerance, natural aging of the electronics and higher selectivity of the L1 calorimeter trigger to keep L1 rate below 100kHz are the driving motivations for an upgrade of the front-end electronics
- Opportunity to apply modern technology and revise architecture
  - Continuous data streaming off-detector
  - Fully digital L0/L1 trigger information with flexible granularity, while interface to trigger system will be guided by physics and MC simulation
- Major challenges
  - Modern technology requires lower voltages, difficult to maintain the required large dynamic range and stringent noise performance
  - Critical radiation hard components (analog front-end, ADC, optical link and power supply)
  - Extremely large bandwidth off-detector readout
  - High performance data handling with very strict latency budget
- Evolutionary scenario towards a digital calorimeter readout at HL-LHC
  - A staged upgrade is being considered with hybrid demonstrators with both analog and digital trigger readout as an intermediate step
  - A well proven demonstrator could be included in ATLAS on a semi-permanent basis
  - Provides information on reliabilities as well as it provides digital trigger data that can be used for HL-LHC L1Calo development

Backup Slides

LHC Upgrade Schedule after Chamonix 2011



Machine: Splice Consolidation & Collimation in IR3

ALICE - detector completion

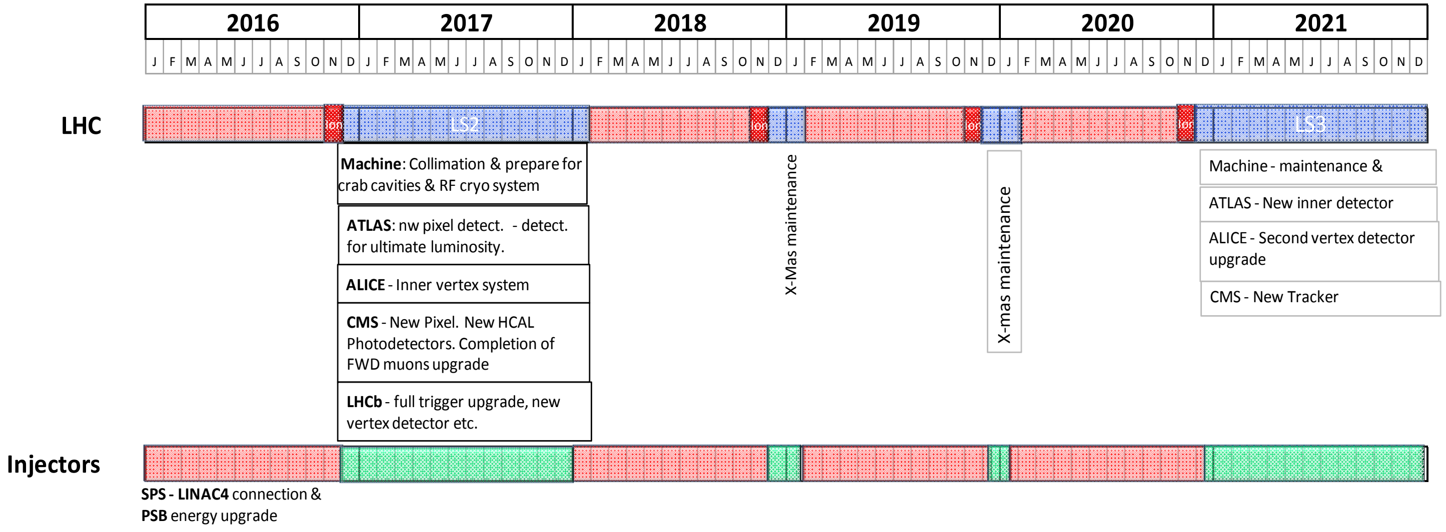
ATLAS - Consolidation and new forward beam pipes

CMS - FWD muons upgrade + Consolidation & infrastructure

LHCb - consolidations

?Cryo-collimation point

? SPS - LINAC4 connection & ? **PSB** energy upgrade



Machine: Collimation & prepare for crab cavities & RF cryo system

ATLAS: nw pixel detect. - detect. for ultimate luminosity.

ALICE - Inner vertex system

CMS - New Pixel. New HCAL Photodetectors. Completion of FWD muons upgrade

LHCb - full trigger upgrade, new vertex detector etc.

Machine - maintenance &

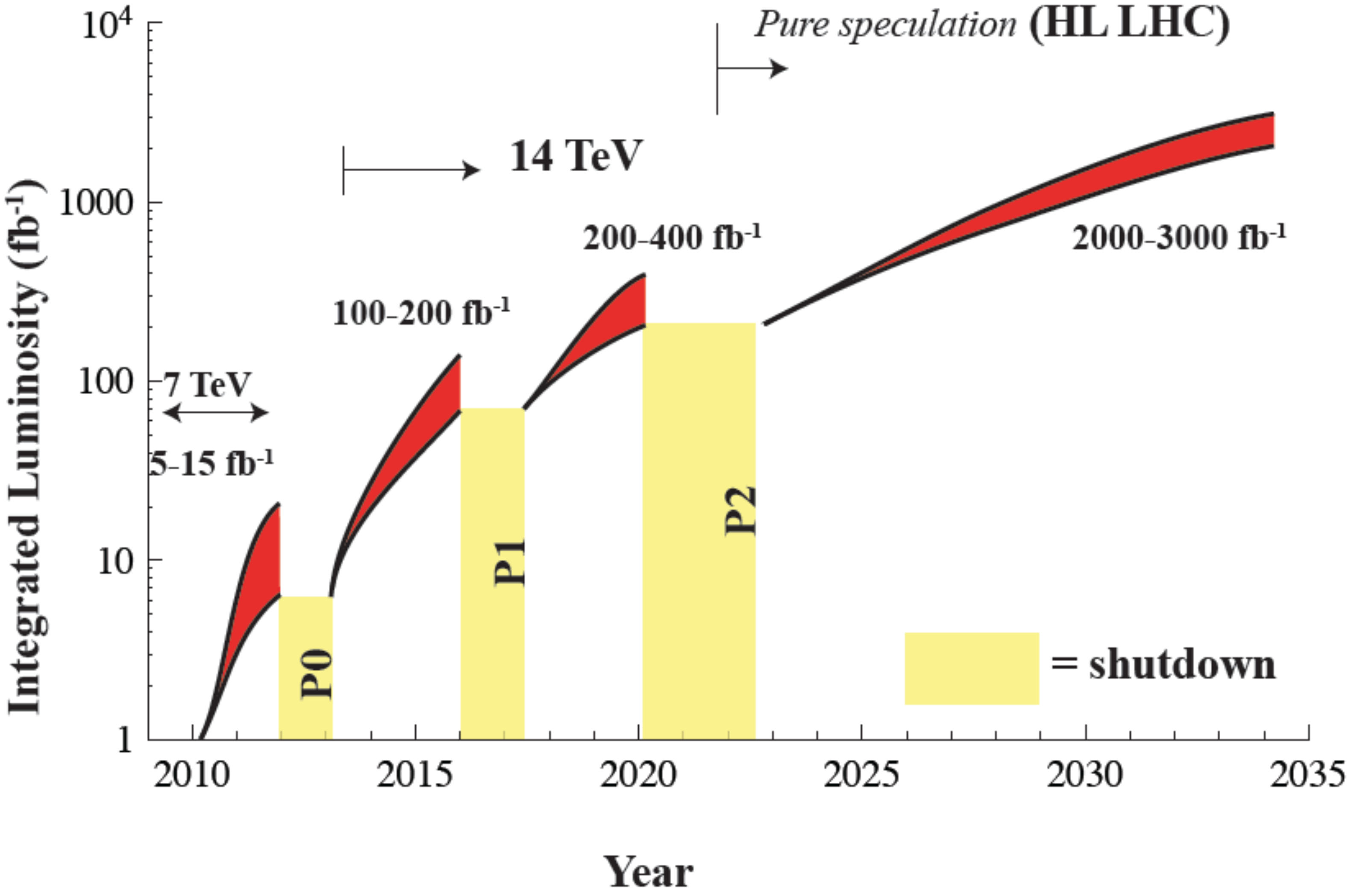
ATLAS - New inner detector

ALICE - Second vertex detector upgrade

CMS - New Tracker

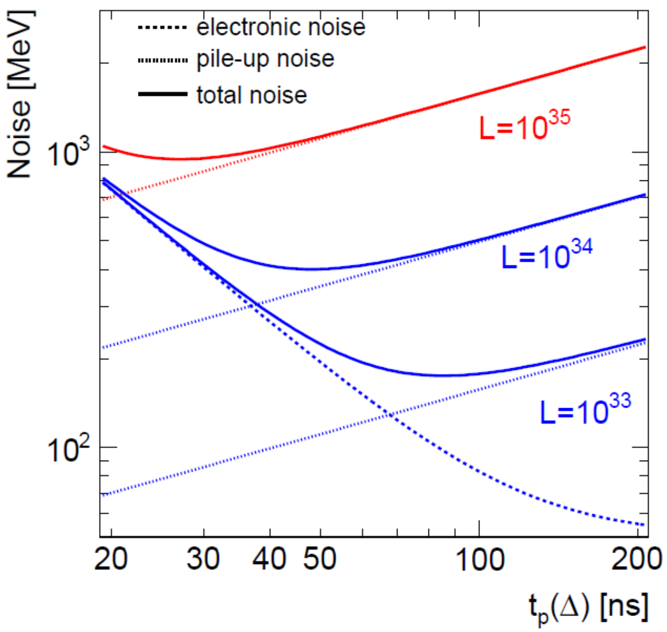
SPS - LINAC4 connection &
PSB energy upgrade

Luminosity Evolution

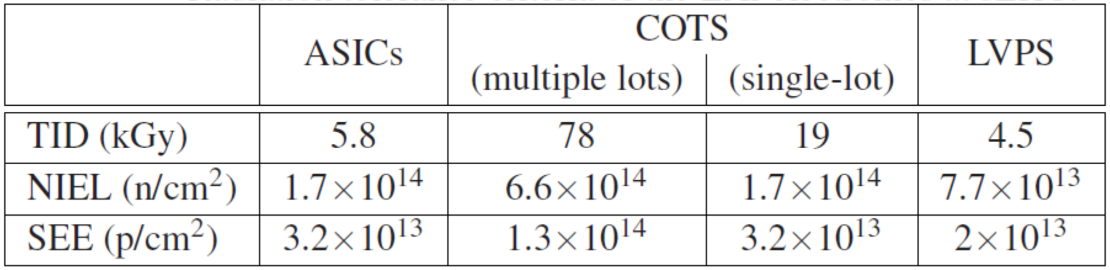


New Readout Challenges at HL-LHC

- Radiation hardness: 10 times more radiation
- Dynamic Range
  - EM: from 50 MeV to 3 TeV (10 mA): 16 bits
  - HEC: up to 1 TeV (0.3 mA)
- Relative energy resolution: $\sigma_E/E \sim 10\%/\sqrt{E} \oplus 0.7\%$
- Electronic calibration: < 0.25%
- Fast shaping to optimize signal/noise ratio
  - Up to 20 times more pile-up events
  - Optimal hardware shaping time scales as $L^{-1/4}$, $t_p(D) \sim$ 28ns @10^{35}
- Digital filtering signal reconstruction: To adapt to changing LHC luminosity
- Minimal coherent pickup noise: < 5% of incoherent noise
- Data to be used for both DAQ and L0/L1 trigger
- Same power consumption



Radiation tolerance criteria of the LAr electronics at sLHC.



	ASICs	COTS (multiple lots)	COTS (single-lot)	LVPS
TID (kGy)	5.8	78	19	4.5
NIEL (n/cm^2)	1.7×10^{14}	6.6×10^{14}	1.7×10^{14}	7.7×10^{13}
SEE (p/cm^2)	3.2×10^{13}	1.3×10^{14}	3.2×10^{13}	2×10^{13}