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# Prototype Real-time ATCA-based LLRF Control System

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***Abstract*—The linear accelerators employed to drive Free Electron Lasers (FELs), such as the X-ray Free Electron Laser (XFEL) currently being built in Hamburg, require sophisticated control systems. The Low Level Radio Frequency (LLRF) control system should stabilize the phase and amplitude of the electromagnetic field in accelerating modules with tolerances below 0.02 % for amplitude and 0.01 degree for phase to produce ultra-stable electron beam that meets the conditions required for Self-Amplified Spontaneous Emission (SASE). The LLRF control system of 32-cavity accelerating module of the XFEL accelerator requires acquisition of more than 100 analogue signals sampled with frequency around 100 MHz. Data processing in real-time loop should complete within a few hundreds of nanoseconds. Moreover, the LLRF control system should be reliable, upgradable and serviceable. The Advanced Telecommunications Computing Architecture (ATCA) standard, developed for telecommunication applications, can fulfil all of the above mentioned requirements.**

**The paper presents the architecture of a prototype LLRF control system developed for the XFEL accelerator. The control system composed of ATCA carrier boards with Rear Transition Modules (RTM) is able to supervise 32 cavities. The crucial submodules, like DAQ, Vector Modulator or Timing Module, are designed according to AMC specification. The paper discusses results of the LLRF control system tests that were performed at the FLASH accelerator (DESY, Hamburg) during machine studies.**

## I. Introduction

Modern linear accelerators require a powerful digital Low Level Radio Frequency (LLRF) system that will stabilise the electromagnetic field in accelerating cavities with tolerances as low as 0.02 % for amplitude and 0.01 degree for phase [1]. To obtain such a good stability, a digital controller with fast feedback and adaptive feed-forward is required [2]. The LLRF system measures the probe signals in accelerating cavities and digitises them [3]. The digital signal, in form of a Vector Sum (VS), is delivered to the real-time controller. The processed in-phase and quadrature componnets (I and Q) are connected to the Vector Modulator (VM) that modifies the phase and amplitude of the reference signal. The modulated signal is amplified and delivered to the accelerating cavities as presented in Fig. 1. The system composed of 32 cavities, LLRF hardware and a single klystron is called an RF station [4].

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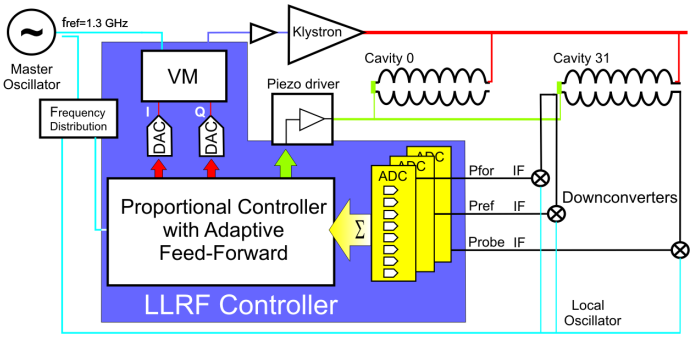


Fig. 1. A block diagram of an LLRF control system. Cavity probe signals converted from the cavity frequency (f=1.3 GHz) to the intermediate frequency (e.g. f=54 MHz) by downconverters are digitized and delivered to a digital real-time controller. The digital controller generates I and Q components that modulate the amplitude and phase of the Master Oscillator signal. The signal amplified by the preamplifier and the klystron is supplied to cavities.

The forward and reflected power signals can be used instead of the probe signal when it is not available in emergency situations, to maintain the operation of the accelerator. Moreover, the reflected power signals can be used to calculate cavity detuning caused by Lorentz force and to compensate the detuning using piezo actuators.

The distributed LLRF control system of X-ray Free Electron Laser (XFEL) will consists of 20 RF stations supervising 640 cavities.

High reliability, availability and modular design of the LLRF system are as crucial as operational demands [5]. Modern telecommunication standards, adopted recently for High Energy Physics applications, like ATCA or AMC could fulfil the above mentioned requirements [6]–[9]. The standard offers native redundancy of the most critical elements, like power supply, communication interfaces and useful features, such as hot-swapping or shelf management and monitoring [6]–[8], [10]–[13].

The designed system, dedicated for XFEL accelerator, was built with the application of ATCA standard. Most of the functionality of the LLRF system is implemented in AMC modules. The application of pluggable AMC modules allows for easy upgrade of the system in the future.

The authors propose the architecture for the LLRF system of a single RF station. The demonstration of the ATCA-based LLRF system was performed at the FLASH accelerator at DESY.

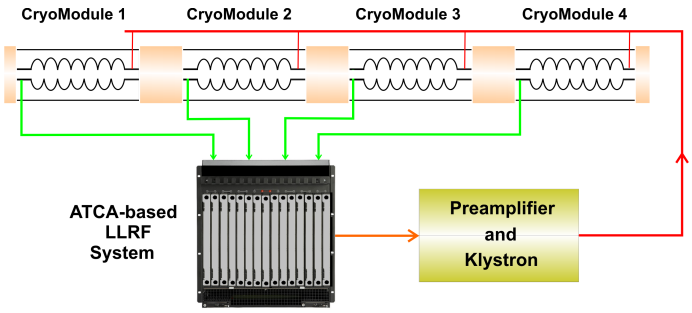


Fig. 2. Centralised LLRF Control System

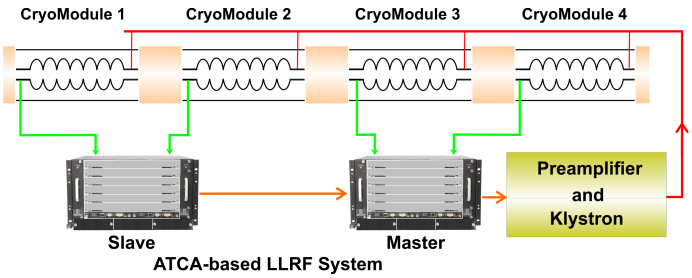


Fig. 3. Semi-distributed LLRF Control System

### A. *Centralized versus Distributed LLRF System*

The LLRF system consists of several ATCA carrier boards with three AMC slots each. An ATCA carrier board supplies the main processing power (FPGA and DSP) and all the functionality required for AMC modules, whereas these modules provide various functionality of the LLRF system. The ATCA-based LLRF control system requires the following AMC devices:

- 8-channel data acquisition module,
- Vector Modulator (VM),
- Trigger and timing module,
- IO module with digital and analogue signals,
- Radiation Monitoring Module (RMM),
- Optional controller for Lorentz force detuning compensation.

Moreover, an additional processing module equipped with a DSP processor or FPGA can be installed in one of the available AMC bays. Analogue RF signals are connected to extension cards defined in the ATCA standard, called Rear Transition Modules (RTMs). Up to four downconverters can be installed on a single RTM. The RTMs are directly connected with DAQ AMC modules via connectivity provided by Carrier Boards.

A single RF station of the XFEL LLRF control system installed in the accelerator tunnel should supervise 32 superconducting accelerating cavities supplied from a single klystron. Groups of eight cavities form four cryomodules (#1 - #4) [14]. Therefore, each RF station should be connected with cavities using 96 RF cables (probe, forward and reflected power signals). The length of the RF cables should be minimized in order to improve temperature drifts of the cables, signal crosstalk and attenuation. Therefore two different architectures of the LLRF system were taken into consideration:

- centralised system,
- distributed system.

The centralised system is composed of a single 14- or 16-slot vertical ATCA shelf [15] delivering infrastructure required by the ATCA standard, e.g. cooling, redundant power supply and Shelf Management (ShM). ATCA carrier boards with various AMC modules and RTMs are installed in the ATCA shelf. The shelf is placed in the central position, next to cryomodules as presented in Fig. 2. The length of the cables is acceptable in such a case, however significant amount of space is required for the ATCA shelf.

On the other hand, the LLRF system of a single RF Station can be split into a few subsystems, each supervising a single cryomodule. The distributed system could be designed with application of four ATCA shelves. In such a case, 5- or 6-slot ATCA horizontal shelves [16] can be used. The dimensions of the shelves give an opportunity to install them just above the cryomodules in the nearest proximity of the accelerating cavities. This solution allows to use short RF cables. However, application of four ATCA shelves with redundant equipment required by the standard will unacceptably increase the cost of the whole accelerator LLRF system. The remedy for this problem could be a semi-distributed system composed of two horizontal shelves installed above the cryomodules #1–#2 and #3–#4 respectively. The concept of a semi-distributed LLRF system is depicted in Fig. 3. In such a case, Master and Slave systems can be distinguished. The Slave system collects all the data from cryomodules #1 and #2 (cavity probes, reflected and forward power, etc.), digitises them and sends to the Master system. The main LLRF controller located in the Master shelf collects data from cryomodules #3 and #4 and receives data from the Slave system. The processed data are provided to the Vector Modulator module and forwarded to the preamplifier and finally to the klystron supplying the cavities. Therefore, low latency connectivity between Master and Slave subsystems is required. The connectivity can be realised using optical fibre and Multi-Gigabit Transceivers (MGTs) available in Xilinx Virtex chips. The control data can be sent using both PCI Express or Gb Ethernet standards. More detailed discussion concerning data requirements and transmission in the LLRF system based on the ATCA standard can be found in [17]. In case of the distributed system, redundancy of main interfaces could be required [18].

The analysis of the system has shown that the horizontal ATCA shelves with 5 or 6 slots can provide the required functionality of the system (including Lorentz force detuning system). The space available above the cryomodules is large enough to house two standard horizontal ATCA shelves [19].

The electronic equipment of the distributed LLRF system installed above the cryomodules will be exposed to higher gamma and neutron radiation doses than in case of the centralised system. Therefore, it is recommended to monitor gamma and neutron fluence in the nearest proximity of the ATCA and AMC equipment.

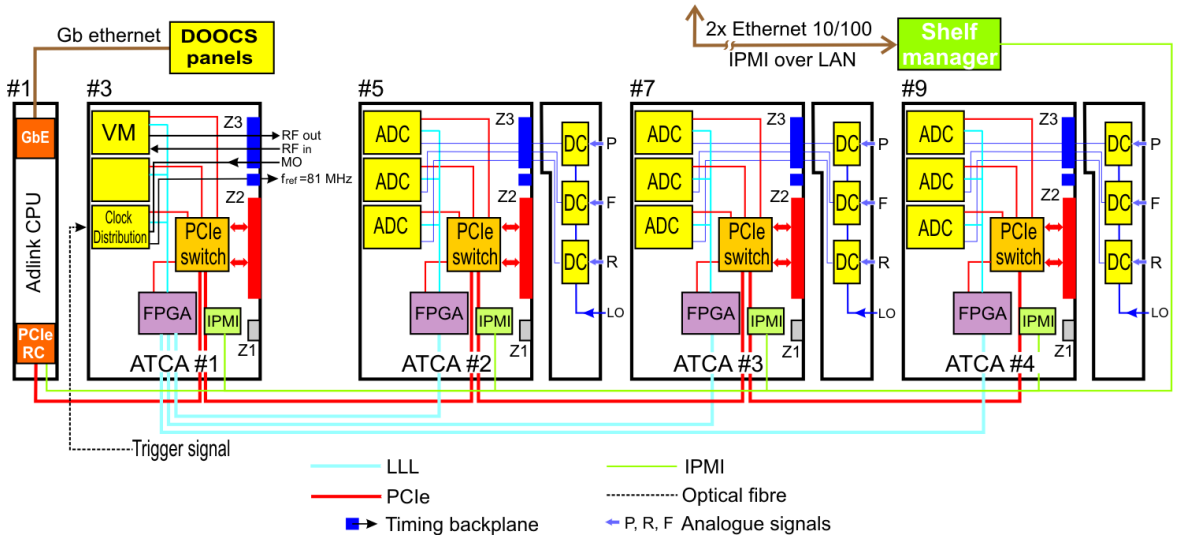


Fig. 4. Block diagram of the test setup of the centralised ATCA-based LLRF system used during demonstration. Adlink CPU is installed in slot #1, other carrier boards are installed in every second slot in order to leave some space for diagnostics instrumentation

## II. ATCA-BASED LLRF CONTROL SYSTEM

Since the FLASH accelerator is an experimental facility and most of its hardware is installed in an experimental hall outside the tunnel, the centralised system was chosen. Only three accelerating modules, namely ACC4, 5, 6, were available for the demonstration. Therefore, the hardware used during the demonstration consists of four in-house developed carrier boards. Three of them are used for data acquisition and one for reference timing and RF signal modulation. The data acquisition modules, Vector Modulator (VM) and Timing module are implemented as AMC modules installed on carrier boards. The block diagram of the LLRF control system with various links emphasised is presented in Fig. 4.

The system is managed using an ATCA computation blade Adlink 6900 with PCIe interface available on the backplane (zone 2). The CPU working under Debian Linux operating system is used as a Root Complex required for PCIe. The DOOCS server running on Adlink CPU was responsible for the configuration of the submodules of the LLRF system. The LLRF system is controlled from DESY control room via Gb Ethernet. Analogue RF signals with frequencies f=1.3 GHz from 32 cavities (probe signals, forward and reflected powers) are connected to downconverters installed on RTM modules. A Local Oscillator (LO) signal with frequency f=1.354 MHz allows to obtain signals with intermediate frequency f=54 MHz that is digitised using commercially available AMC modules TAMC900. The vector sum signals, partially calculated in FPGA devices available on TAM900s, are sent to the main FPGA present on the carrier board installed in the slot #3. The data transmission uses a custom Low Latency protocol based on the LVDS standard. The measured latency is less than 120 ns. The main Feed-Forward controller implemented in the FPGA chip available on the carrier blade in the slot #3 generates the I-Q signal that is connected to the VM. It is responsible for modulating the RF signal used to drive a preamplifier and a 10 MW klystron. The timing module is responsible for generating clock and trigger signals required in the LLRF system. The hardware used during demonstration with Ethernet cables and Xilinx programmers is depicted in Fig. 5 (only two carrier boards are installed in the shelf).

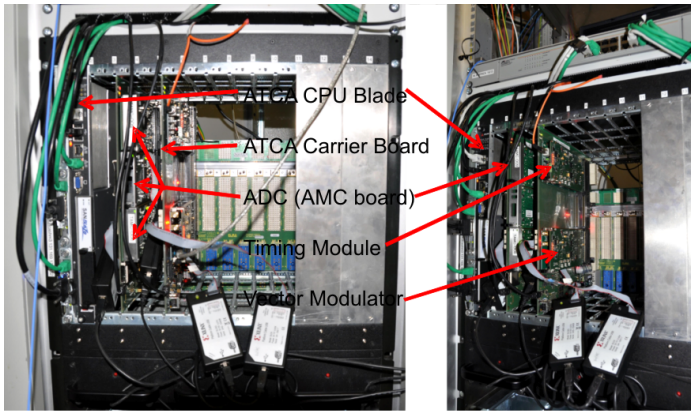


Fig. 5. A photograph illustrating the ATCA shelf with hardware used during the demonstration. From the left hand side: Adlink computing blade, two Carrier Boards fitted with five AMC modules (3x DAQ, VM and Timing)

*1) ATCA Carrier Board:* The ATCA carrier designed for LLRF system is equipped with three AMC bays. The board provides low latency computation for Real-Time (RT) controller loop (Xilinx Virtex 5 FPGA) and floating point Digital Signal Processor for more complex applications required for system diagnostics. The photograph of the carrier board with an RTM module and three AMC modules is presented in Fig. 6.

The carrier board provides all the necessary interfaces for the RT controller, system management and diagnostics required by the ATCA standard. A more detailed discussion of various links can be found in [17]. The FPGA device is connected using Low Latency Links (LLL) with all three AMC modules. The main carrier board with the VM has low latency connectivity to all other carrier boards, see Fig. 4. Each carrier board has a built-in, eight channel PCIe x1

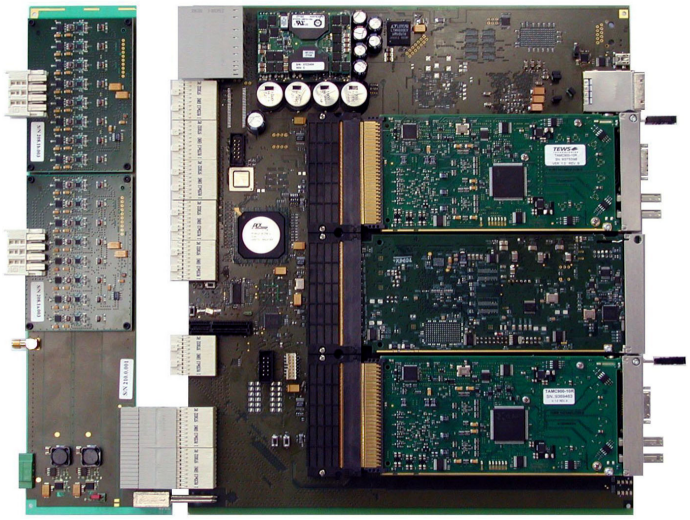

Fig. 6. Photograph of Carrier Board filled with three AMC modules and RTM with downconverters

switch connected to the AMC modules, the FPGA on the carrier board and two channels on the backplane (zone 2). The PCIe chain link between the carrier boards is created during activation using Intelligent Platform Management Interface (IPMI) mechanisms, see Fig. 4.

The reference timing signal is generated by the Timing module (f=81 MHz) from the Master Oscillator (MO) and distributed together with trigger signals using a custom timing backplane.

All analogue signals are transmitted from the RTM module using Erni connectors (zone 3).

*2) AMC Modules:* Most of the functionality of the LLRF system, required for its basic operation, was implemented using hot-swappable AMC modules:

- 8 channel data acquisition module,
- Vector Modulator,
- Trigger and timing generation module.

The DAQ TAMC900 module was manufactured by TEWS company, whereas the VM and timing modules were developed in-house. The AMC modules consist of two parts: a digital AMC_B board including all the digital hardware required by the AMC standard and FPGA processing power, and an AMC_A module fitted with all the hardware required for subsystem functionality, e.g. VM or timing hardware [20].

*a) Local Timing Generation and Distribution:* The LLRF control system requires synchronization of devices within the ATCA crate by means of timing signals. Two types of timing signals are distributed locally within the ATCA shelf: the trigger and the clock signals. Both signal types are generated by the AMC Timing Receiver card (called AMC_TM). The trigger signals are derived from a fiber-optic receiver part of the AMC_TM. Three different CMOS-level trigger signals are decoded in the FPGA and sent to the AMC connector of the Timing Receiver. Three independent clocks are also generated by the AMC_TM. The clock frequency can be flexibly programmed in the range from 10 MHz to 100 MHz. Clocks are synchronized to the RF phase reference signal delivered to the ATCA shelf from the Master Oscillator [21] system. The required jitter value for the clock is less than 5 ps. The jitter demonstrated at the output of the AMC_TM in laboratory conditions varies between 1 ps and 1.3 ps depending on the clock frequency [22], [23].

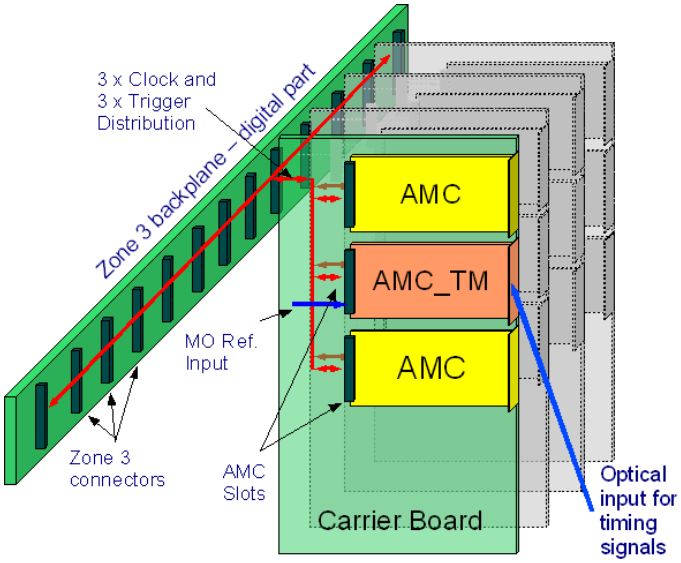


Fig. 7. Timing signal distribution inside the ATCA shelf

The timing distribution scheme is shown in Fig. 7. The AMC_TM can be located in any AMC bay on the carrier. The timing signals are distributed over the carrier to the remaining AMC bays. There is also a bidirectional connection between the ATCA carrier board and the custom Zone 3 Backplane (Z3B). The Z3B allows for distribution of the trigger and clock signals to other carrier boards inside the ATCA shelf. This architecture allows for distribution of the timing signals from any AMC bay on any carrier to all other boards within the shelf. The redundancy is also supported by a possibility of switching between two AMC_TM cards in case of failure of one of the modules.

*b) Vector Modulator:* The AMC Vector Modulator module (AMC_VM) is used as an actuator device delivering an RF output signal of the LLRF control system. The AMC_VM output signal drives the klystron input. The Vector Modulator card contains an I-Q modulator circuit [24] that can change the amplitude and phase of the MO phase reference signal. The modulator I and Q inputs are driven by high-speed DACs. The DAC control signals are transmitted to the module via the low-latency link from the ATCA carrier. The AMC_VM module also contains DC offset conditioning circuits, RF power amplifier, programmable attenuator, RF-gate and diagnostic circuits. The attenuator allows for implementation of automatic output power level control. The RF-gate protects the AMC_VM output from high level signals coming from the klystron input and it also can be used for fast shutting down of the klystron drive signal in case of interlock or any fault detection. A detailed AMC_VM card description is given in [25].

*c) Data Acquisition Module:* The TAMC900 single width, mid-height AMC has been selected for data acquisition.

It consists of eight LTC2254 14-bit, 105 MS/s ADCs, two modules of 250 MHz 18-bit x 1 Mword QDR-II SRAM at two independent channels and the XC5VLX30T Virtex-5 FPGA. Data from ADCs can be transmitted to the CPU by up to x8 PCIe link. The configuration of the on-board peripherals is maintained by XC95144XL CPLD. The TAMC900 provides three clock inputs and three trigger inputs. The three external clock inputs and the PCIe reference clock are routed to a flexible clocking scheme that allows independent clocking of the ADCs in two groups. The trigger inputs are routed directly to the FPGA. The inputs to ADCs are connected via the AMC connector and the carrier board to the downconverters on the RTM. The module also features a set of LVDS connections [26], used as a low-latency link to the remaining parts of the controller.

*d) Radiation Monitoring Module:* The Radiation Monitoring Module (RMM) is designed as an AMC module [27]. The module is not indispensable for operation of the LLRF control system, however it could be helpful when the system will be installed in the tunnel and exposed to radiation. The module equipped with gamma and neutron radiation detectors allows to estimate doses absorbed by the LLRF hardware. A RadFET detector is used for gamma dosimetry, whereas a Static Random Access Memory (SRAM) chip is applied as a reference error counter or neutron fluence detector when it is calibrated [28], [29].

Since the LLRF control system was installed outside the accelerator tunnel and it was not exposed to radiation during tests, the RMM module was not tested.

*3) Lorentz Force Detuning System:* In the XFEL the piezoelectric actuators are to be used to compensate the changes in the cavity resonant frequency caused by Lorenz forces deforming the cavities during the RF pulse. This system requires generation of control signals at the level of hundreds of volts, uncommon to the ATCA-based system. This part has not yet been fully implemented and tested. Two possibilities are considered:

- a separate crate connected to the ATCA system via an optical cable,
- a special, custom-made ATCA board.

### A. Distributed LLRF Controller

The LLRF controller calculates appropriate control signals for the RF field source based on the measurements of the RF field in individual cavities to achieve the required RF field stability.

The simplified block diagram of the algorithm is presented in Fig. 8. The first stage of the algorithm is I-Q demodulation of the signals for individual measurement channels. After an arbitrary calibration of each detected vector, they are summed together to create the Vector Sum (VS) of the fields in the whole accelerating module. This sum is compared with a user-provided Set Point (SP) value and the resulting error signal is processed by a P-Controller in a feedback loop. To create the final control signal, multiple corrections are applied and the resulting I-Q vector is provided to the output.

The presented architecture of the hardware platform requires special considerations for the firmware design. To ensure efficient usage of resources, the control algorithm blocks have been distributed among several FPGA chips connected with each other using Low Latency Links.

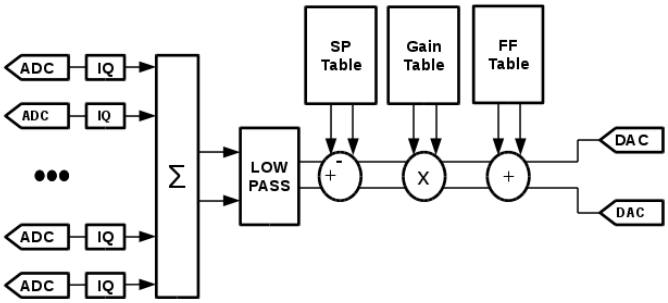


Fig. 8. The structure of the algorithm executed by the LLRF controller.

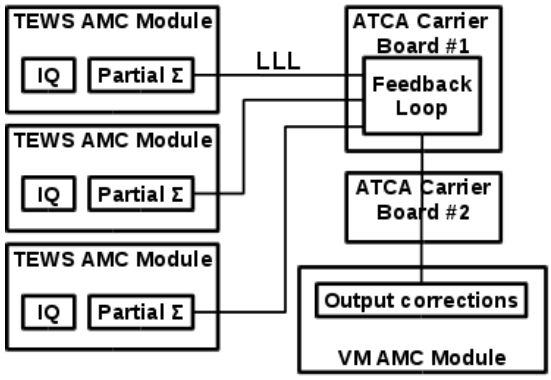


Fig. 9. The distribution of the LLRF Controller firmware blocks.

As presented in Fig. 9, the blocks related to field component detection are moved directly to FPGAs on the TEWS AMC modules. Each module calculates a partial Vector Sum. The final VS calculation and the main part of the feedback algorithm is executed on the carrier board installed in slot #3, see Fig. 4. The intermediate control signal is transmitted to the Vector Modulator board where the final corrections are applied and the control signal is provided to the output.

Such distribution algorithms require several interconnections between FPGAs on several boards. The communication links were implemented as differential lines using the LVDS standard. In the presented application, the latency of the whole algorithm is important - excessive latency reduces the maximum feedback loop gain possible to achieve. To minimise the latency and number of used lines, Double Data Rate (DDR) serial transmission protocol is used. The achieved latency of a single link is below 100 ns.

### B. Diagnostics and Control Software

DOOCS [30] is a distributed object oriented control system designed to secure a reliable software platform for high energy experiments conducted in the DESY research center. It allows to provide functionality starting from the device server level up to the operator console [31]. DOOCS server

for ATCA-based LLRF control system was installed on the ADLink carrier board working under control of the DESY distribution of Linux operating system. Therefore it was able to perform direct communication with each system component through the PCIe bus. The main task of the server was to process input calibration coefficients taken from the operator control panels presented in Fig 10 , interpret it, recalculate the control parameters and send it back to the appropriate hardware subsystems. The server was synchronized with the

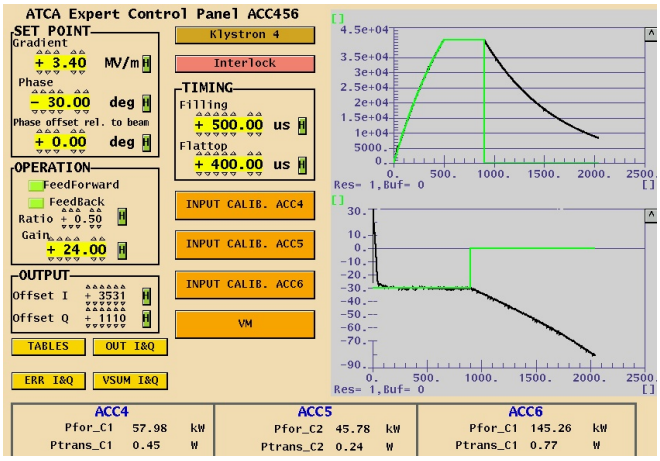


Fig. 10. Control system panel with input calibration coefficients for ACC4.

hardware system through the USR1 signal generated by the PCIe device driver in response to the MSI interrupt from the LLRF controller. Therefore, after every operation phase of the accelerator, it updates current information about the system activities. Consequently, the operators can monitor the status of the machine in real time and react quickly to detected anomalies.

### C. Intelligent Platform Management Interface

The Intelligent Platform Management Controller (IPMC) is a vital part of every intelligent Field Replaceable Unit (FRU) in ATCA. It is responsible for communication with the redundant Shelf Managers (ShMs) as well as Advanced Mezzanine Cards (AMCs) in case of ATCA carrier boards. The entirety of management communication concerning any given FRU is governed by the IPMC. The states of various sensors, including voltage, current and temperature, need to be monitored by it in order to be able to detect and possibly prevent any failures. They must at least inform the System Manager about such occurrences.

Moreover, IPMC has to deal with Electronic Keying (EK) that is linking the devices in an ATCA shelf according to the interfaces they are able to support. This removes the need for manual cable manipulation at the front panel since all the connections have been moved to the backplane. In case of the Carrier Board (CB) for LLRF Control System the PCI Express (PCIe) protocol has been used for sending the configuration parameters to the LLRF controller. Each CB stores information about the possible connections in a non-volatile EEPROM. This data is presented to the ShM during activation to which the ShM responds with requests to activate certain links. The IPMC, knowing the relative position of its CB in the shelf as well as the states of other CBs, enables only these connections which are necessary to create the PCIe chain as presented in Fig. 4. This procedure is repeated every time a board is activated or deactivated in the shelf and the IPMC is responsible for maintaining the proper links. This is done automatically, with no help of the user, thanks to dedicated algorithms implemented in the IPMC.

## III. Initial Tests of the System in FLASH Tunnel

The main goal of the tests of the prototype ATCA system at FLASH was to demonstrate that this standard fulfils many technical aspects required for XFEL. The performed demonstration was only an initial test of the system performed in two steps: running in the laboratory and controlling with feedback an accelerating field in 24 cavities of the FLASH accelerator.

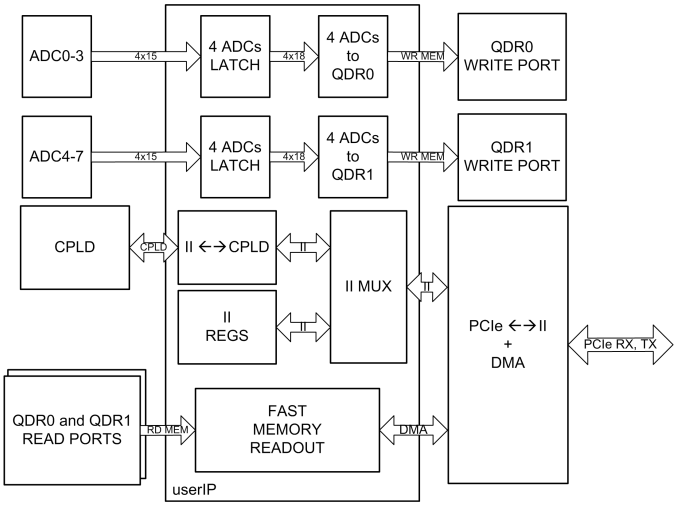


Fig. 11. Block diagram of TAMC900 diagnostics and readout firmware

### A. DAQ - Diagnostics and Readout

For diagnostic purposes the data from all the TAMC900 channels can be stored in QDR memory during the RF pulse and transferred via the PCI Express interface between the pulses. The block diagram of the firmware is presented in Fig. 11. The Integral Interface [32] is used to communicate with the firmware control registers. For the transfer of the ADC samples DMA has been implemented, allowing to achieve the data rate of 140 MB/s for x1 link and 400 MB/s for x4 link.

### B. Tests in Laboratory

The goal of the tests in the laboratory was to put all analogue and digital components in one ATCA shelf, connect the test signals, install software and make it all run together. The tested system comprised four carrier blades equipped with nine TAMC900 ADC modules, one AMC vector modulator and one AMC timing module. All the boards were managed by an ATCA CPU-6900 blade located in slot 1. The configuration is presented in Fig. 12a. The three ATCA blades with ADC

modules were coupled with RTM modules where analogue signals were connected - 24 probes, 24 forward and 24 reflected power signals from 24 cavities. The RTM modules are visible in Fig. 12b.

a) b)

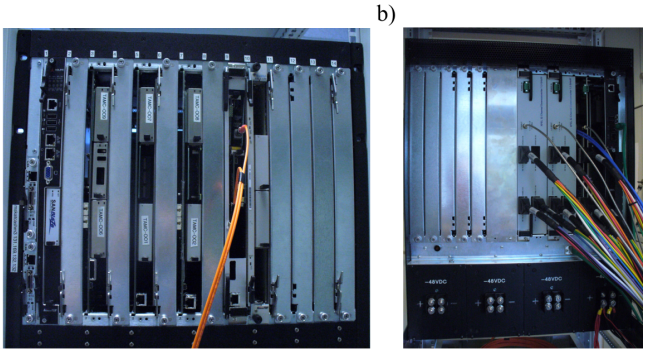

Fig. 12. The photograph of the ATCA shelf used during the demonstration of the prototype ATCA system, a) the front panel and b) back panel.

During the tests, the software installed on the CPU was controlling other modules over the backplane using PCIe protocol. The software controlled 15 FPGA chips with firmware doing cavity field detection, timing configuration and distribution, analogue vector modulator control and data acquisition. The laboratory test also helped to improve software for IPMI running on every module in the shelf.

### C. Tests of the 24 Cavity System

An RF station for XFEL will consist of 32 cavities in 4 accelerating modules driven by one klystron. The FLASH accelerator was an excellent place for testing the system. In 2009 the modules ACC4/5/6 (24 cavities in total) were driven by one klystron. This is very similar to the XFEL setup. The system was installed in the experimental hall and real signals of the FLASH accelerator were connected. The system was running in feedback mode controlling field in 24 cavities and driving a 10 MW klystron. The performance of the system was measured in the so-called gain scan experiment. The gain of the feedback loop was changed from 0 to 60 and the stability of the vector sum of 24 cavities was measured by calculation of amplitude and phase stability for a given feedback gains. Fig. 13 and 14 present the results from the experiment where the red dashed line is the minimum value. The optimal point was achieved for gain equal to 35 and the corresponding stability was $(\Delta A/A)_{rms}$ = 0.945e-3 for amplitude and $(\Delta\phi)_{rms}$ = 0.1589 deg. The achieved stability fulfils the requirements for field stability in the linac section of the XFEL accelerator.

## IV. Summary

During the tests in the FLASH accelerator the centralized version of the system has been used. The whole system, apart from the TAMC900 DAQ boards has been custom-made. The custom components, never tested before, included the carrier boards, the AMC_B modules, the Vector Modulator, the Timing module, the Timing backplane and the Intelligent

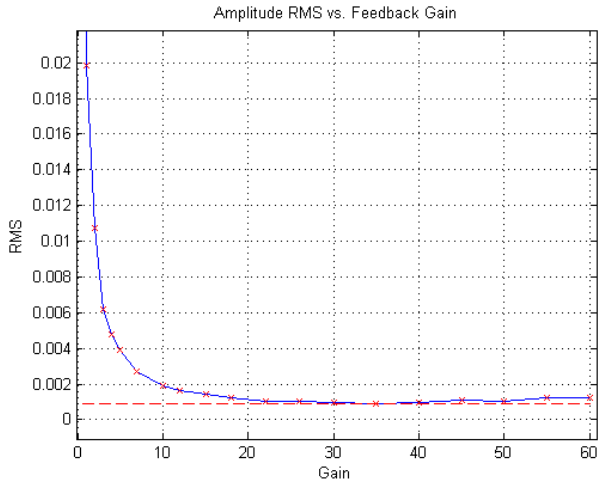


Fig. 13. Amplitude stability measurement for varying feedback gain

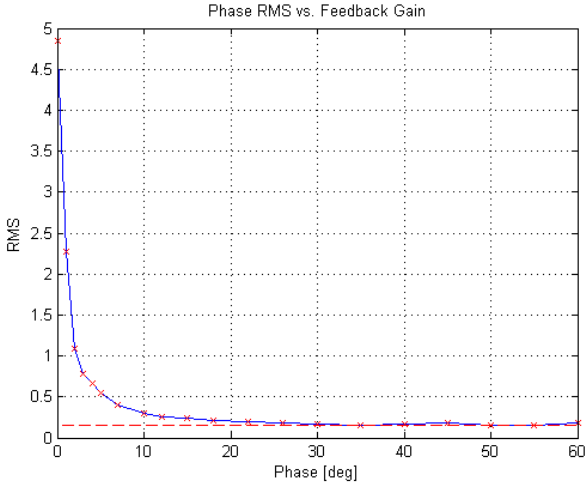


Fig. 14. Phase stability measurement for varying feedback gain

Platform Management/Module Management Controllers. The components integrated together operated very well, fulfilling all the expectations.

The PCI Express bus has turned out to be a very efficient solution. The possibility of application of DMA makes it particularly convenient to transfer data to the PC. It is very well suited for a system occupying only one shelf. For the distributed solution, the PCIe-over-cable or PCIe-over-fibre are needed. The latency of round-trip over the PCIe connection is very low – it amounts to a few microseconds – due to the application of cut-through switches. The external control of the system must be performed using Gigabit Ethernet. The switches in this technology usually apply the store-and-forward technique, making the latency dependent on the packet size – at least 16 ns per byte. The cut-through switches are hard to find. As PCIe or Gigabit Ethernet are used only for data acquisition and slow control, this is not a limiting factor. Building a system based purely on Ethernet eliminates the necessity of application of GbE-PCIe bridges, making the

system simpler and eliminating additional protocol translation latency. Making the redundant system based on GbE is also easier than the PCIe-based one - a VLAN-enabled switch is enough for this purpose. The low-latency direct links using the LVDS connections allow to achieve latency of order of several nanoseconds. They have been functioning very well during the tests, allowing to realize a distributed controller based on 4 carrier boards.

There were some problems with the clock jitter – the current bus clock distribution architecture is not optimal, additional signal splitters on the carrier boards are necessary. This has been corrected in the second revision of the carrier boards.

The system has very large computational power - multiple digital signal processors and FPGAs makes the system easily upgradable. The implementation of remote firmware upgrade via the IPMI protocol based on the HPM.1 standard is under development.

Estimation of the reliability of the system requires much more time and it is not known at the moment. Plenty of design errors have been detected and fixed in the next revision. New version of the boards is being manufactured and new tests are planned. Many questions are still unanswered, however the demonstration at FLASH has proven that the ATCA standard can be used for instrumentation purposes where many channels of small signal levels must be processed with low noise and low latencies of a few hundred nanoseconds.

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