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VISIT TO NEVIS LABORATORIES, COLUMBIA UNIVERSITY

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ABSTRACT

Columbia University is preparing an experiment in which proportional multiwire chambers will be used on a large scale. Since the apparatus used for it is similar to the one we want to use at CERN, we were interested in the progress the group at Columbia University has made in developing the amplifiers and read-out logic for the chambers. This report gives the present state of the art of their work.

Another point of interest is the "Sippach Logic". A brief description is given of this electronic system, used in almost all the Columbia experiments.

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1. AMPLIFIERS AND READ-OUT LOGIC FOR CHARPAK CHAMBERS

1.1 Amplifiers

For a reliable amplifier design, one must first understand the operation of the chambers. Therefore a definite amplifier has not yet been developed.

In order to measure the performance of different chambers and gases an amplifier with an adjustable bias and an adjustable threshold control is used. This amplifier uses a Motorola MC 1Ø35 integrated circuit as amplifier, followed by a MC 1Ø2Ø as threshold.

The main parameters which have to be known for the definite amplifier design are:

1) jitter time distributions;
2) time relation between pulses on two adjacent wires;
3) performance of the image pulse on the adjacent wires;
4) rise-time and shape of the pulses;
5) gas amplification factor;
6) capacitance of the wires;
7) properties of signal propagation in long wires.

With an experimental set-up using a chamber with a wire spacing of 3 mm, a wire thickness of 30 µm, and filled with argon +5% methane, the following preliminary results were obtained:

1.1.1 Jitter time or arrival time

In principle a jitter-time distribution is a curve which represents the time in which enough electrons of the ion track are amplified by the gas to pass the threshold of the amplifier discriminator system. This means: the greater the gas amplification and the lower the threshold of the amplifier, the more the curve tends to become a distribution of the time which is necessary for the nearest electron, or cloud of electrons, of the ion track to move to the wire.

Figure 1 shows a typical time distribution measured with a low threshold of the amplifier and a high gas amplification. It appears that in this system one single cloud of charges can be detected, since the shape of the curve stays the same over a reasonable range of the gas

amplification. At much lower gas amplification the distribution is smoothed, because more single clouds of charges have to be gathered in order to pass the threshold. These smoothed curves are similar to the ones measured previously at CERN.

Further, it has been demonstrated that pulses occurring in the regions A and C of Fig. 1 correspond with the nearest single cloud of charges to the wire being in the regions A and C respectively of Fig. 2. Region B is a boundary case and corresponds to single clouds of charges between two wires. Probably this region extends over the entire border between the regions A and C.

If one is able to develop a chamber-amplifier system operating under the above described conditions it must be possible to decrease the thickness of the chamber to about twice the wire separation. This gives many advantages. Since there is an indication that each track will lose enough charge in region A, the decrease of thickness will not affect the efficiency of the chamber. Some chambers of different thickness will be made to test this.

1.1.2 Time relation between pulses on adjacent wires

Particles which pass through the chamber, at certain angles, can generate charges in region A of one wire (Fig. 2) and in region C of an adjacent wire. Measurements prove this.

A proper opening time of the gate in the system, just covering regions A and B, will give a minimum number of double wire events, without producing a dead-gap between the wires.

Within the geometrical limits there is not any indication that triple wire events occur.

1.1.3 Image pulse

An image pulse always occurs on wires adjacent to the wire closest to the ion track. The shape and timing of this pulse are roughly the same as those of a pulse generated by the charges in region A (Fig. 1, Fig. 2). In the present test chamber the amplitude was about 15% of the amplitude of a primary pulse. Suppression of this pulse by means of compensation

methods failed since there remains a considerable amount of signal with a high-frequency structure.

Thus in order to avoid double or triple wire triggering, the amplifiers and triggers should be insensitive to input signals of the opposite polarity during the opening time of the gate in the system.

1.2 Read-out logic

In the proposed read-out system the wires of a chamber are split up into main groups of 128 wires. Each main group of 128 wires is again split up into 16 subgroups of 8 wires.

When an event is stored in the flip-flops of the wires and the gates are closed, the main groups of all chambers are simultaneously read-out in their appropriate buffers. Only the subgroups containing one or more set flip-flops are read-out, which is expected to be done in about 70 nsec + 30 nsec per subgroup. Into these buffers the 8 wire flip-flops of a group are transferred in parallel and the address of this subgroup is transferred in binary code. Each buffer can consist of one or more subgroups.

During this fast read-out the wire flip-flops are reset which means that the chambers are again ready for a new event, while a central logic unit can find out whether the stored event is of interest or not for read-out on tape.

With this read-out system one has a reasonably short dead-time (expected smaller than 250 nsec) while all the relevant data of an event are, in an economic way and without ambiguity still available for further examination.

Besides the large redundance of the system allows a flexible examination of the stored event.

The data of an event will be written on tape in binary form. The address of a chamber is determined by the sequence of read-out in the tape format. Optionally a double event in one or more chambers can be written on tape in a special coded form at the end of one event block. Also the possibility to read-out all data on tape will be available.

The entire system will make use of the Motorola MECL II integrated circuits. A pair of printed circuits, consisting of the read-out logic of one group, up to the buffers, has already been developed. On this board space is available for the amplifiers. One proposes to plug these cards into a busbar system which is placed along the edge of the chamber. The buffers will be placed at the end of this busbar system.

2. "SIPPACH LOGIC"

In hodoscope counter experiments many decisions are made by electronic equipment in order to separate the information of the desired events from the background and events of no interest. Many of the decisions made are simultaneous logic and timing decisions. The difficulties for the timing decisions due to jitter and delay times increase with the complexity of these systems. The "Sippach logic", however, separates the logic and timing decisions in order to avoid these problems. Especially in experiments where a great flexibility of the logic is required, this system is very useful.

2.1 Basic principle

Figure 3 shows the principal block diagram of the system.

Each counter of the experiment is connected to a gated fast register. The gates of all registers are opened only when a possible good event may occur, as determined by the signals of one or more counters in the experiment or for instance by a signal coming from counters upstream. The delay times of all counters are equalized by means of cables in such a way that all signals arrive at the same time, with respect to the gate signal, in the fast registers. The opening time of the gates is equal to the jitter time in the system. Since all the relevant information of an event is stored in the fast registers during the gate time, no further timing considerations are necessary.

The outputs of the fast registers are fed into the "d.c. logic". In this logic the operator can select the logical requirements for a good event. A fixed time after the end of the gate pulse, longer than the maximum propagation time of the d.c. logic, a pulse strobes the outputs of the logic. The output on which a signal appears determines how to deal with the information of the event caught. For instance, an event of

interest can be written on tape, and an event of no interest rejected.

The entire system is under the control of a master logic, which generates the gate, strobe and reset pulses for the registers, and interacts with the computer, tape units, etc. Less significant decisions of the d.c. logic are always strobed into scalars.

With an additional set of registers a feature of measuring the accidentals can be created. Therefore, the gates of the fast registers are opened twice. The first opening is in time with the possible event. The second opening is after a fixed delay, thus out of time with the possible event. Before this second opening of the gates the content of the fast registers is duplicated in a slow register. This register then contains the information of the "first time slice". After the second gate opening the fast registers contain the sum of the information entered during "the first and the second time slice" as these registers are not cleared before the second gate opening. If one of the time slices contains accidental information the slow and the fast registers contain different information. The d.c. logic finds out whether this is the case or not.

2.2 Modules

Nevis Laboratories has a stock of standard units for this system. Most of the units are already a few years old. Therefore these units still use transistors and discrete components. A new generation with improved specifications, using only MECL II and MECL III integrated circuits will be made in the future. Some of the circuits are already developed. At the same time another arrangement of the inputs and outputs of the modules will be made which allows a more flexible interconnection of the logic signals of the several units. Since at present the reliability and the specifications are good enough for the current measurements, the production of the new generation has not yet been started.

The frequently used modules are listed below.

i) Fast register

This module contains 8 fast registers and their input gates which can be opened simultaneously by a gate pulse.

ii) Threshold summing logic

Out of up to 16 levels of fast register outputs this unit gives outputs when either 1, 2, > 2 and > 3 input levels are present.

iii) Switch logic

Into this system 16 outputs of the threshold summing logic can be fed. With switches, any logical combination of these 16 signals can be selected. The selected combination can be strobed. A busbar system allows a multiple use of these 16 inputs. The system consists of two different units: a busbar driver unit which powers the busbars with the original and the complementary levels; the second unit is the unit with the switches.

iv) Matrix (coincidence)

This unit contains an 8 × 8 matrix into which outputs of fast registers are fed. The logical "AND" combinations are made by placing transistors in the appropriate crossings of the matrix.

v) Scalar strobe gates

vi) Read-out modules for the computer

This is a special unit for a specific computer.

vii) Fan out

These units are used to fan out the gate pulse to all fast registers.

2.3 Performance

In a system like this, when compared with a conventional system, the complexity of the logic requests does not affect the timing performance at all. In a conventional system for instance, an antisignal must always overlap the signal which has to be vetoed, often giving problems due to different dead-times of these signals. The "Sippach logic" allows, therefore, an optimized time performance. All the counters including anti-counters have the same dead-time. In addition, the counting rate of the counters can be high.

Acknowledgements

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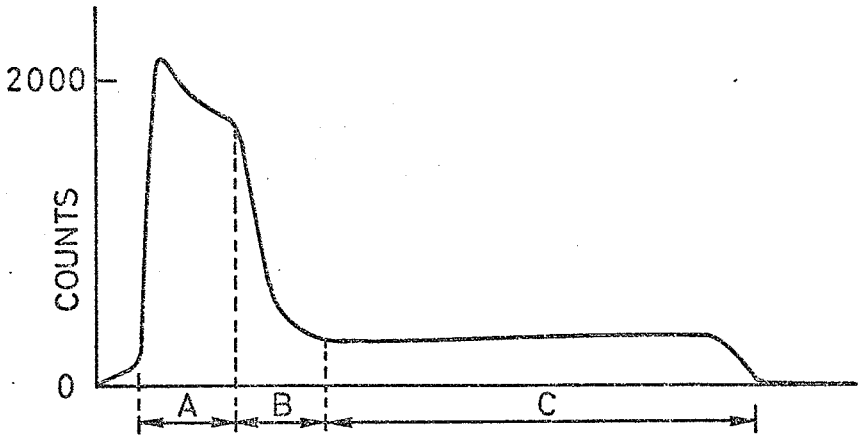
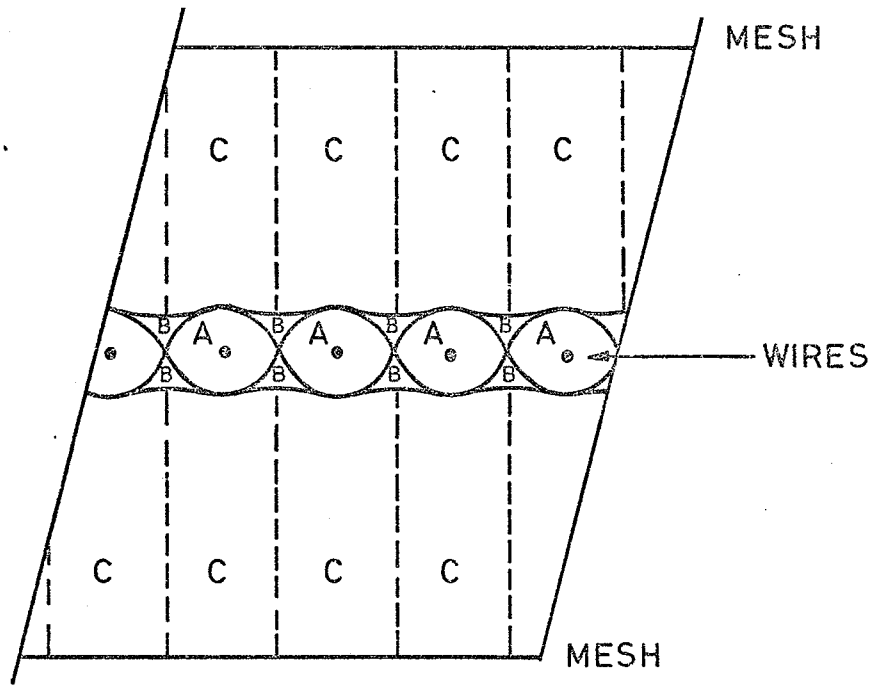


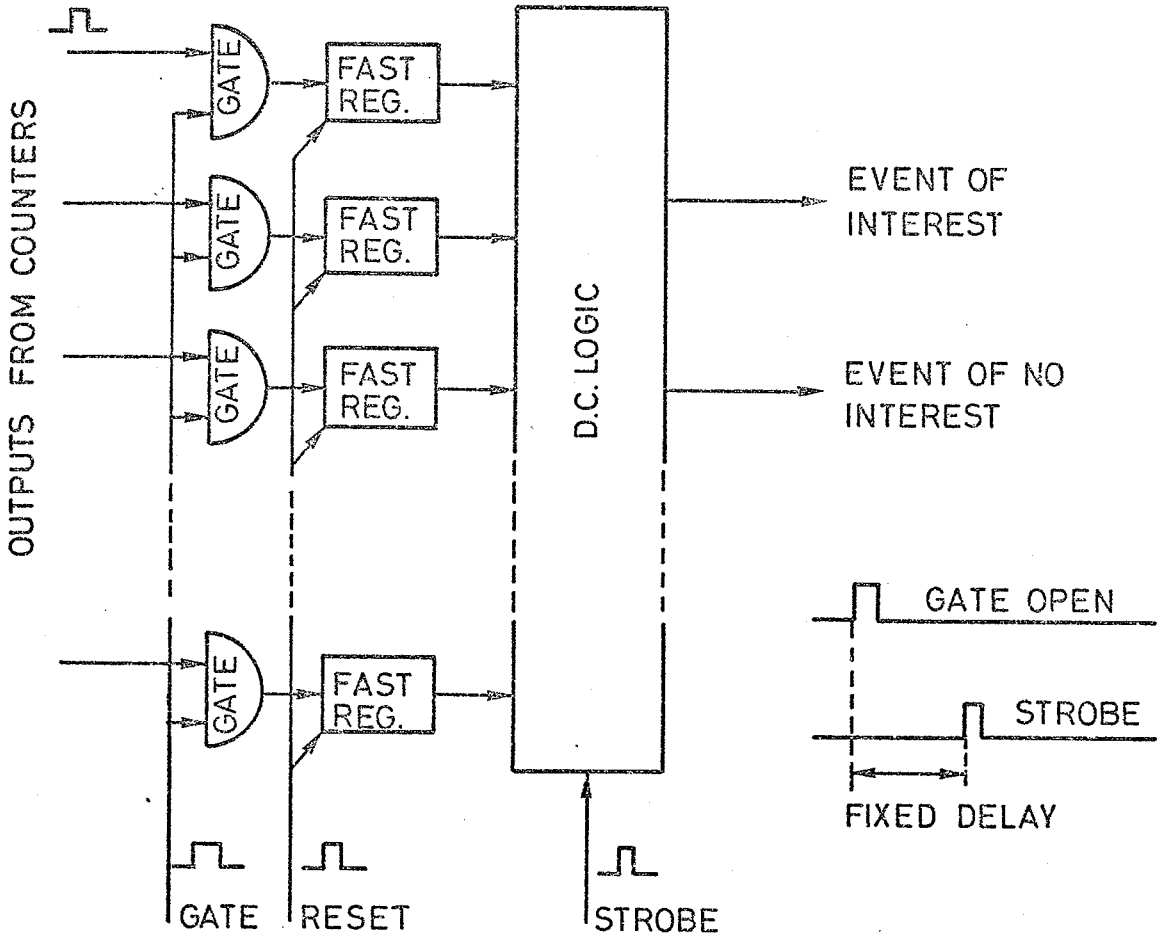
TIME DELAY BETWEEN TRAVERSAL OF β RAY AND THE OUTPUT OF THE DISCRIMINATOR

FIG.1



MULTIWIRE PROPORTIONAL CHAMBER CROSS-SECTION WITH THE TIME REGIONS

FIG. 2



PRINCIPAL OF "SIPPACH LOGIC"

FIG.3