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SPECS: a Serial Protocol for the Experiment Control System of LHCb

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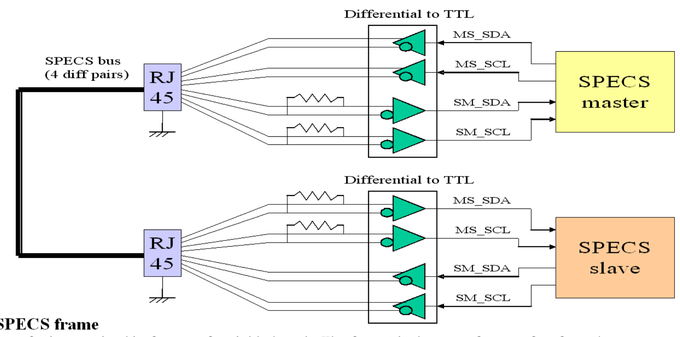
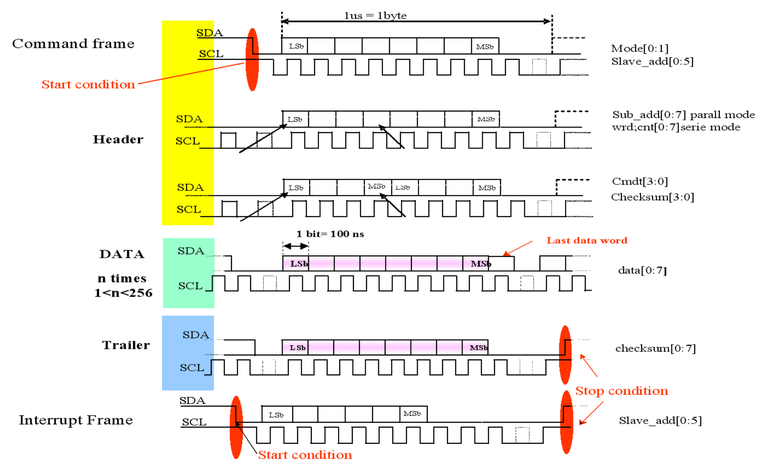
SPECS protocole

The SPECS is a single master, multi slave serial bus. It communicates between an unique master and up to 32 slaves (limit fixed by the address range), at a 10 MHz rate, thanks to 4 different unidirectional lines. These lines called MS_SDA, MS_SCL, SM_SDA, and SM_SCL are the data and clock lines, from master to slave, and from slave to master respectively. They can be implemented in differential mode (8 wires) or in unipolar mode (4 wires).



The SPECS frame

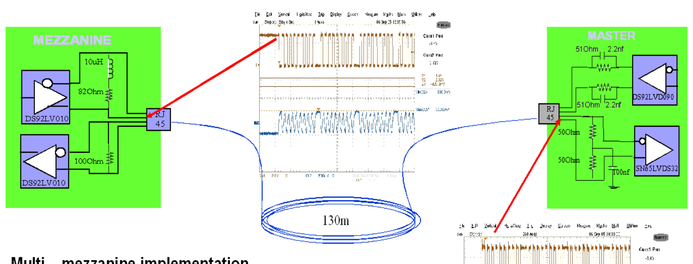
Data transfer is organized in frames of variable length. The format is the same for transfers from the master to the slaves or in the other direction, except for the interrupt commands which have a specific frame. The frames start and stop with a specific transition of the data line when the clock line is at a high level ("1"). These transitions are called 'start condition' and 'stop condition', and are identical to the ones used in I2C.
The clock lines are active only during a data transfer and remain quiet during an idle phase. A frame is composed of a variable number of words, the latter being separated from each other by a 'missing clock cycle'. This makes the debugging by oscilloscope very easy, since the packets are clearly identified. The words have a fixed length of 9 bits and, due to the missing clock cycle, a word needs 10 cycles to be transferred. Therefore, with the 10 MHz clock frequency, the data transfer rate is 1 MB/s.



SPECS implementation

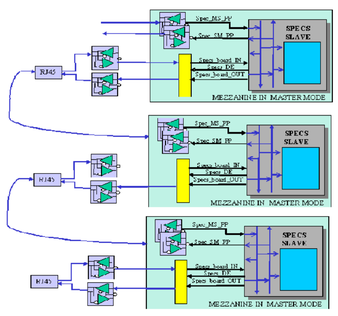
Mezzanine implementation

On the SPECS mezzanine, 2 SPECS interfaces are provided: one point to point for long distance interconnection and one for local bus connection. Thanks to this feature, we can handle several mezzanines on the same SPECS bus. Mezzanine can be chained using cable. We use Ethernet CAT6 cable with RJ45 connector. To allow length up to 130m and patch panel, pole zero cancellation have implemented on both master and slave.



Multi – mezzanine implementation

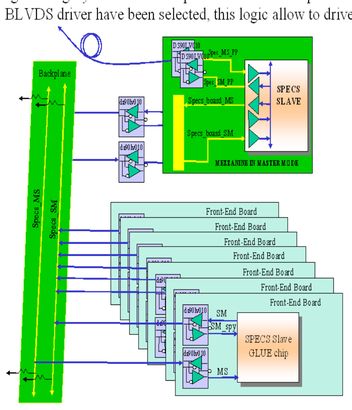
Long distance implementation



For chaining SPECS mezzanine slave, several solutions are available. To respect signal integrity rules extra drivers receiver and RJ45 connector are mandatory. In this configuration we can chain up to 32 mezzanines with length up to 30 meter between slaves.

Backplane implementation

The SPECS protocol is mono-master multi-slave. This permits the implementation of many slaves on the same bus.
For the Calorimeter electronics, the SPECS bus will actually be distributed on the remote crate backplane. Simulation with signal integrity tool have been performed to select specific logic (plot. result on fig 1 et fig 2)
BLVDS driver have been selected, this logic allow to drive 21 slot with a good noise margin.



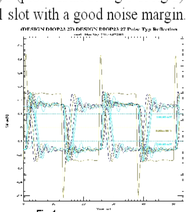


Fig 1: plot of the 21 slot
Fig 2: plot of the nearest neigbour receiver, slot 9 & 11
Fig 3: Signal on the 11th slot with differential probe

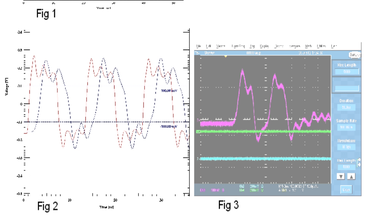
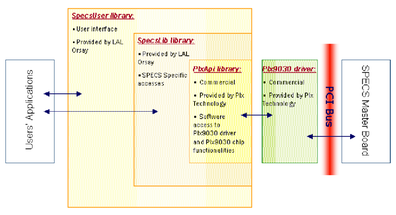


Fig 1 Fig 2 Fig 3

The SPECS software

Software Layers



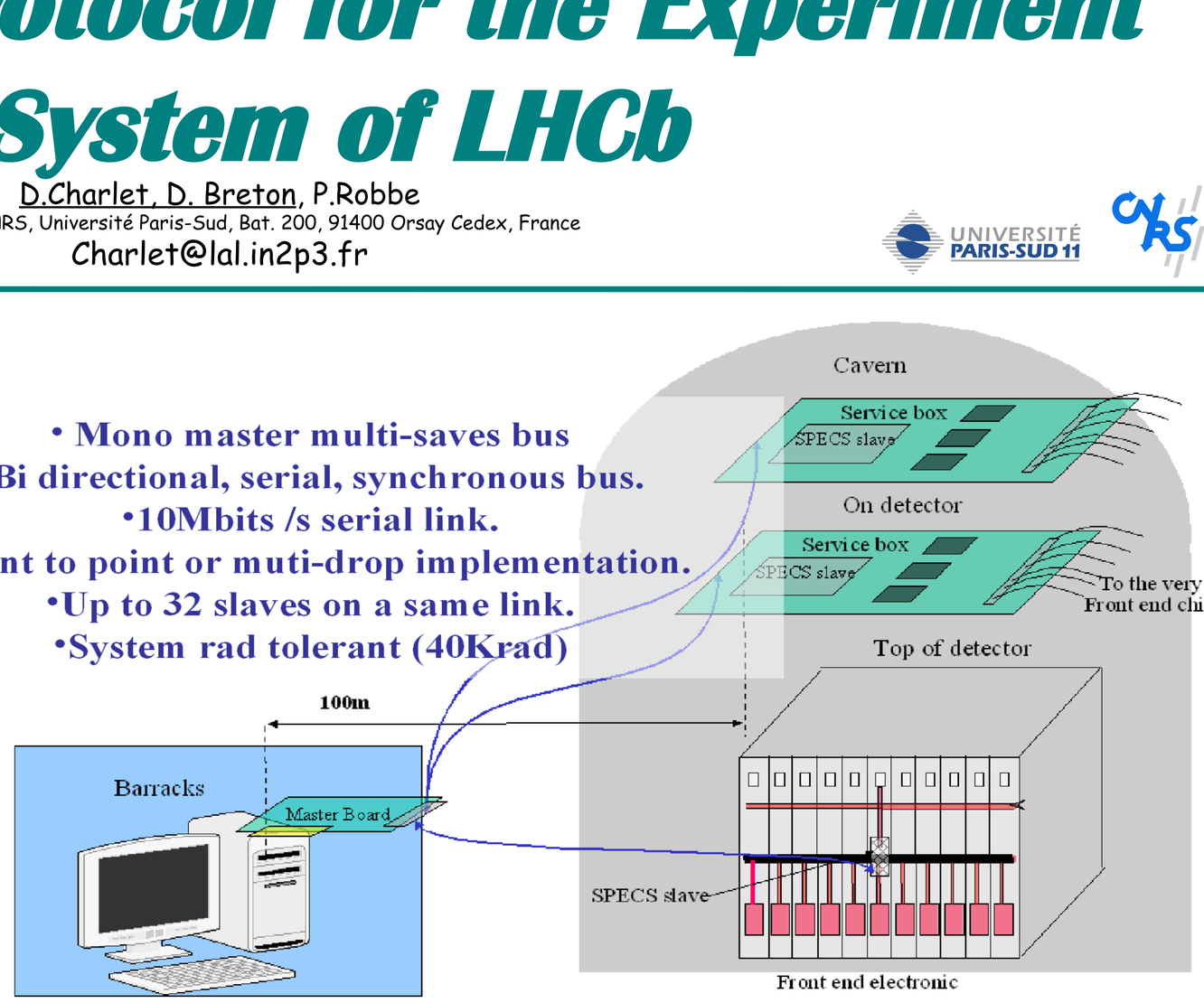
The control of the SPECS system is achieved using specific libraries that allow access to all the available functionalities.
The libraries are available for both Windows and Linux environment and are written in C language.
In order to maintain low CPU occupancies, accesses to the Master buffers are managed by PCI interrupts instead of polling status registers. The libraries also provide protection mechanisms to allow several applications or users to use the same board at the same time.

Software Functionalities

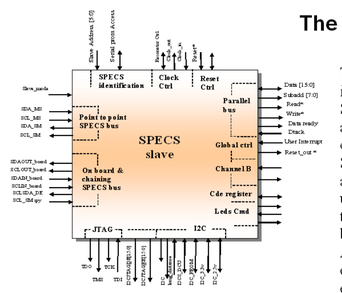
The Software libraries give access to all SPECS functionalities:

1. *I2C Accesses:*
   - **Read:** with or without sub-address (ie first word after address word), with selection of I2C bus
   - **Write:** with or without sub-address, or using general I2C calls.
   - **Error reports:** when the I2C slave address does not exist (SPECS interrupt associated to no I2C acknowledge).
2. *Parallel Bus Accesses:*
   - **Read:** automatic selection of DMA access when the size of data to send is larger than 1 (x 16 bits)
   - **Write.**
3. *JTAG Accesses:*
   - **Reset,**
   - **Idle,**
   - **Irscan,**
   - **Drscan.**
4. *Register Accesses:*
   - **Read:** to any Slave register (I/O pins, Clock Selection, ...)
   - **Write.**
5. *Management Functions:*
   - **Initialization:** initialization, termination, or reset of communications with Masters or Slaves
   - **Identification:** of Master location and serial number.
   - **Control:** selection of SPECS Master clock frequency, reset of Emitter and Receiver FIFOs
   - **Error Report:** when problem in data transfers (timeout, checksum error)
6. *Combined Accesses:*
   - **On-board DCU Functionalities:** initialization, reset, selection of input mode, and acquisition of input channels
   - **On-board EEPROM Functionalities:** read to all 65 kbits of the EEPROM (identification and User space), write to the User space.

- **Mono master multi-saves bus**
- **Bi directional, serial, synchronous bus.**
- **10Mbits /s serial link.**
- **Point to point or muti-drop implementation.**
- **Up to 32 slaves on a same link.**
- **System rad tolerant (40Krad)**

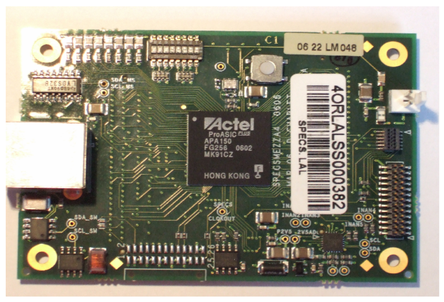


The SPECS slave



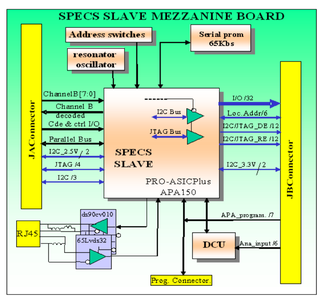
SPECS slave chip

The slave is designed as a portable VERILOG code and is physically integrated inside an ACTEL flash PGA. With this technology, the slave is SEL immune, and is also SEU immune, because the internal registers are appropriately protected by triple voting techniques, and state machines use one-hot state. Moreover, to ensure a high reliability of the decoding of the SPECS commands, there are no state machine in the SPECS receiver part. In addition, all commands (and in particular all resets) are generated without using any local clock but only the SPECS lines. This may for instance allow the user to reset the TTCrx through SPECS if necessary. The chip will also be reasonably radiation tolerant, up to 10 krad (with some safety margin, the ACTEL chip having been tested up to 40 krads) over the lifetime of the experiment. It can then be placed at most locations where we foresee to have electronics, except in or near the Vertex Locator tank. The chip is an ACTEL APA150.



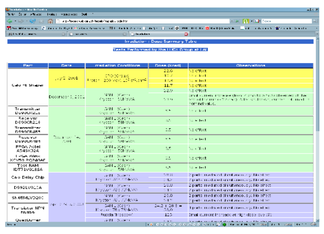
SPECS slave mezzanine general description

A mezzanine daughter-board has been developed to house the SPECS slave, and to provide all the described functionalities of the SPECS Slave chip through 2 SMC connectors. The mezzanine board also provides most of the necessary service functions for the sub-detector front-end electronics. The goal is to avoid putting unnecessary electronics in the radiation sensitive area.
The mezzanine can be configured in master mode or in slave mode. In master mode, the mezzanine can deal with 2 SPECS busses:
One point to point long distance bus. This bus is implemented with RJ45 connectors on the mezzanine, which permits a direct connection, without any additional component, to the master through an Ethernet cable.



List of the main features of the mezzanine board:

- One long distance point to point differential SPECS interface (coming from the SPECS master).
- One unipolar SPECS local interface for multi-load bus applications.
- Three serial bus: 1) local I2C 2) long distance I2C 3) JTAG bus.
- 16 JTAG or 15 I2C chip-select control bits and direction control bits for external drivers.
- One parallel bus offering 16 data bits and 8 address bits.
- One decoder for the channel B of the TTCrx, decoding: A) L0 front-end reset, B) Calibration pulse type 0, which can be delayed with a programmable counter.
- One 32-bit static register to control or read back the local environment. The bits [31..0] can be individually configured either in output or in input mode.
- One reset signal. This output can be triggered without the need of any clock on the board.
- One local 40MHz oscillator. It is also provided as an output of the mezzanine and can be enabled by the software.
- One PROM which will allow the ECS system to obtain some information about the front-end element housing the mezzanine. It will be mounted on a socket.
- One DCU chip with 6 ADC channels of 12-bit resolution.

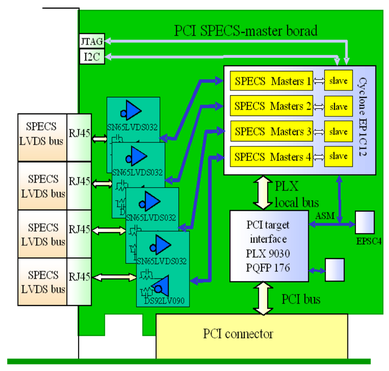


Radiation environment

For radiation zones, hardness to the single event latch-ups (SEL), single event upsets (SEU), and single event transients (SET) are required. This point has to be considered carefully, and the design of the slave chip ensures that the registers and state machines are protected by appropriate redundancy. The single event latch-up sensitivity however depends on the technology used. For this reason we have tested and chosen some specific ones. All the components have thus been tested either by us or by other laboratories up to 30kRads

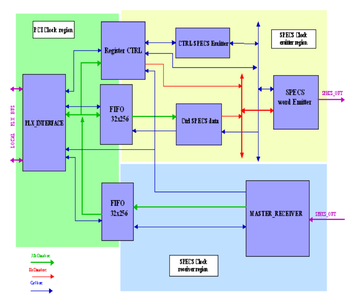
The SPECS master

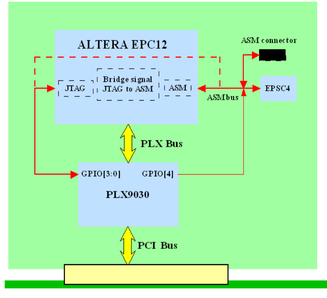
The SPECS master board hosts 4 SPECS masters. The SPECS master is implemented on a standard 32-bit 33 MHz PCI board, which can be plugged into a PC. In order to offer an easy setup for the test benches, the board also includes an internal SPECS slave, which allows the user to benefit from both JTAG and I2C local output capability. The heart of the system is integrated within an ALTERA CYCLONE FPGA and the PCI interface is performed by a PLX9030 chip, each of them having its own configuration EEPROM. For the driver part, we use the DS92LV090 driver with the voltage RC pole-zero cancellation. For the receiver part, due to the long distance link, we use receivers with high common mode input voltage range (-2 to 4.4V), and low differential input thresholds (< 50mv), SN-5LVDS032 from TI



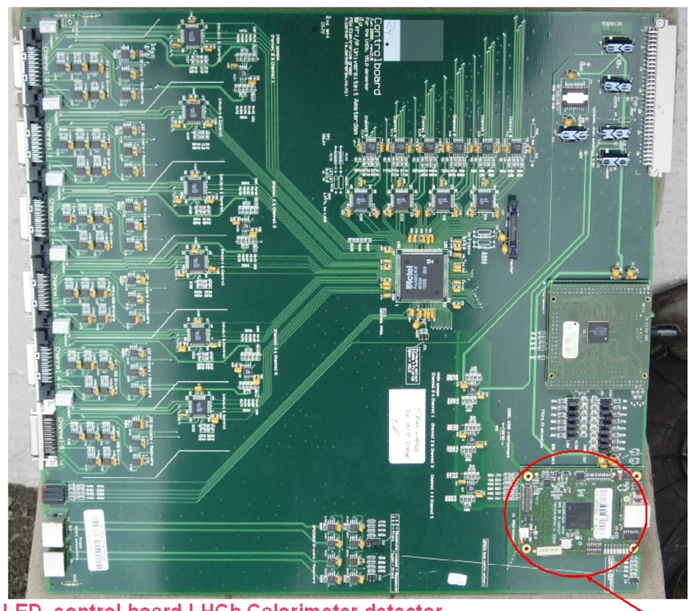
The loading of the FPGA via the PCI bus. To do this, the general purpose I/O of the PLX 9030 and the JTAG of the FPGA are used. The GPIO are configured and connected to the JTAG. The download file contains firmware which takes control of the active serial bus of the FPGA, this one is used to load the EEPROM and to configure the FPGA, and also transform the FPGA into a bridge between the 2 buses. After with the INIT command we download the firmware contains in the EEPROM which replaces the specific one. The JAMPLAYER software is delivered by ALTERA and allows, after modification, to control the GPIO, the GPIO emulate a JTAG bus.

The firmware have been developed in portable verilog code.
One of the main characteristic is the 3 different clock domains.
This require specific logic like anti-metastability system or "rendez vous" system.

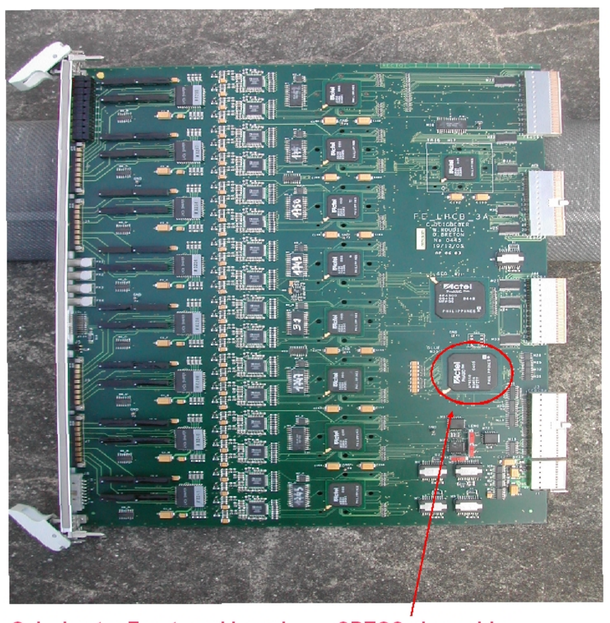




CROC Calorimeter control board



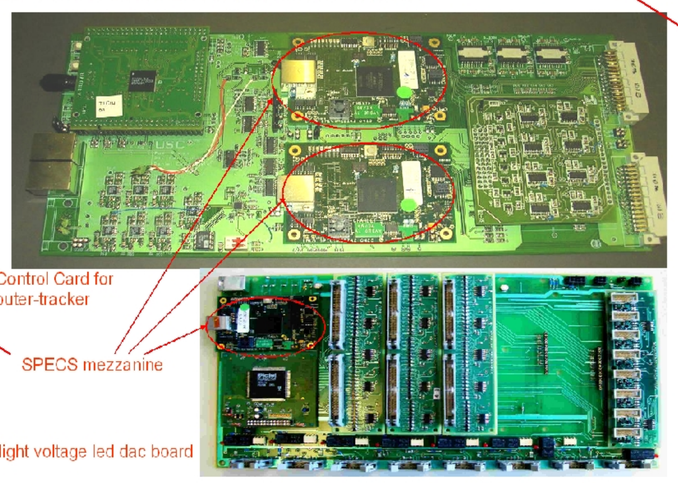
LED control board LHCb Calorimeter detector



Calorimeter Front_end board

SPECS slave chip

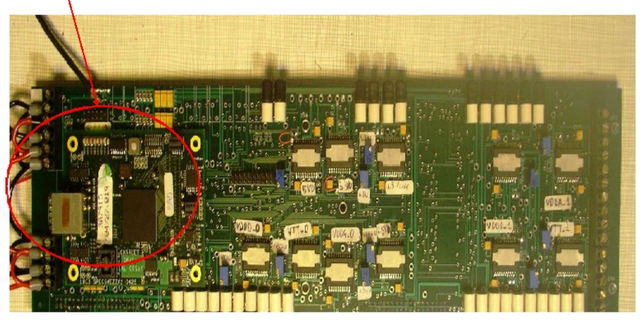
SPECS mezzanine



Control Card for outer-tracker

SPECS mezzanine

Hight voltage led dac board



HPD module control board LHCb RICH detector

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