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1. Introduction

The UA1 experiment is a large multi-purpose particle physics detector system. It was designed to provide full solid-angle coverage around the LSS5 intersection region of the CERN proton-antiproton collider operating at a centre of mass energy of 540 Gev. The experiment has been operational since November 1981 and the next data-taking period is scheduled for September 1984. At present an upgrade program (4) involving the installation of new detectors and the improvement of the data acquisition system is in progress.

This paper describes the current upgrade of the data readout and online data handling facilities by means of a multicrate and multiprocessor system based on the industrial standard VME/VMX bus (1) and the M68000 microprocessor family.

The various parts of the detector and the data acquisition system have already been described elsewhere (2,3). In short, the apparatus consists of a central detector built of drift chambers with image readout to provide particle tracking, surrounded by a variety of complementary electromagnetic and hadronic calorimeters in both the transverse and longitudinal directions of the beam. A dipole magnetic field provides momentum analysis, and the whole detector is surrounded by an iron shield, which is being instrumented with multiple planes of Iarocci tubes, and a matrix of muon chambers (2). Additional drift chambers, in the forward and backward directions, complete the detector's 4π coverage. It is planned to insert a high resolution cylindrical drift chamber in the beam pipe in order to improve track reconstruction around the collision point.

The data digitization and formatting are performed by about 200 Camac crates grouped in 28 Remus branches (5). These are read in parallel into a multievent buffer system. A variety of specialized processors such as ROP (6) , FAMP (7), 168/E (8), Super Caviar (9) and NORD computers, share the tasks of event data compression, digital trigger, readout control and mass storage. The number of channels and the amount of data generated by the digitizing electronics for each event are given in Table 1. In Table 2 are listed the main components of the UA1 data acquisition system.

2. Trigger Levels and Data Acquisition Phases

At the design luminosity of the SPS proton-antiproton collider ($10^{30}/cm^2$ sec) the collision rate is of the order of 50 kHz, with a beam crossing every 3.8 μsec. The average luminosity obtained during the last data-taking period, in 1983, was $3\ 10^{28}/cm^2$ sec, and an increase by a factor of 10 is expected for the next data-taking period starting in September 1984. This corresponds to a collision rate of about 15 kHz.

The maximum event readout rate is limited by the magnetic tape speed to about 4-5 Hz . In order to reduce the trigger frequency from several KHz to a few Hz, and maintain the overall system efficiency above 90%, the data acquisition operates in separate phases. Distinct levels of triggering take place before and during the data digitization, the data reduction, and the data readout phases.

A pre-trigger selects beam-beam interactions using standard NIM logic to demand a coincidence between hodoscopes in the proton and antiproton directions to within ± 20 ns. A first-level decision is then made between beam crossings, using a purpose-built processor system to fast identify energy distributions and prompt muon signals from the muon chambers. At this moment the data are in the phase of digitization and the data reduction and reformatting are enabled.

A second-level trigger decision can be activated only if a muon candidate is identified in the first-level, using M68000 microprocessors (7) to attempt to establish whether the muon candidate comes from the interaction region. At the same time data are formatted in parallel by a set of specialized processors and read into a multi-event buffer system. The system dead-time is determined mainly by the central detector data processing time (of the order of 35ms) . However, the future incorporation of a hardware double buffer into each digitizer channel of the central detector readout will limit this dead-time to the ADC conversion time of 3ms. In order to reduce this dead time, further, to a few microseconds, the addition of an analogue double buffer to the calorimeter channels is also being studied.

Finally more refined decisions are made, based on the analysis of the event data by 168/E processors. These processors re-check the trigger condition matched in the preceding levels with greater precision and execute more sophisticated selection algorithms. This event filter is used either to flag or to reject an event. The maximum input rate to this phase of readout is about 30 Hz while the output rate, depending on the mass storage speed, is 4-5Hz.

3. Data Readout Structure

Figure 1 indicates the general structure of the data readout. Two systems

run concurrently during data acquisition: the parallel readout and the event data builder. They are controlled by two independent processor units: the readout supervisor and the event manager.

The Parallel Readout system consists of a set of detector busses autonomously driven by independent bus drivers associated with dual port memory units . These dual port memories are able to store several events, with a common port for data sorting. Data processing for reformatting and trigger selection can be executed in parallel by each driver unit accessing the data via a private bus. The readout supervisor handles the first level trigger signals, initializing the drivers for data readout, allocating the available memory for event buffering and controlling all the phases of data input. In addition this processor accomplishes the task of controlling and testing the digitizing electronics.

The Event Data Builder system accesses the parallel readout buffers and a set of event units, which are able to accept full event data for data acquisition and data sampling tasks. The event filter is part of this system. The event manager supervises the event building process, serving any event request coming from an event builder unit, initializing a multi-DMA transfer from the parallel readout buffers into the event unit memory, and starting and monitoring the event process. After the completion of an event transfer, for data acquisition, the event manager enables the corresponding multievent buffers for further trigger data input.

Such a structure was implemented from the beginning of the experiment in 1981, using Camac crates and Remus readout modules, with hardware FIFO memories for the parallel readout. The readout control processor was made of hardwired standard NIM logic. A Super CAVIAR microcomputer performed the task of event manager, controlling a stack of five 168/Es acting as an event builder unit. Other data sampling tasks were executed by a HP21MX and two NORD 100/500 computers, spying the data during acquisition. This solution was satisfactory in the previous data-taking periods with a trigger rate of the order of a few Hz, at first level trigger, and an overall system efficency of 90%. Its main limitations were the speed of the event readout at the third trigger level, at maximum 3 Mbytes/sec, and the difficulty of extending the system performance by including additional processing and control units. In order to cope with the higher rates expected in subsequent data-taking periods, and to allow for the modular expansion of the system in order to extend the second level trigger and the event data handling facilities, a hardware double buffer is being added to all the digitizer electronics channels that most affect the data reformatting dead time (namely the central dectector charge to time digitizers CTD (20)) . In addition the data readout system is being partially rebuilt with the use of the general-purpose multiprocessor VME/VMX bus.

4. VME-VMX Bus

The VME bus is a 32-bit data and 32-bit address asynchronous multi-processor bus (20MHz bandwidth) introduced by industry (Mostek, Motorola, Signetics) in 1982 and now IEEE standard.

It is based on double size Eurocard mechanics. A large variety of general-purpose modules for processing, control, communication and display are commercially available. In addition, in order to improve the performance in applications where local data access and private memory extension are needed, a 32-bit data and 24-bit address local bus VMX is specified. Since the UA1 data acquisition improvement essentially involves the data readout part, and not the digitizer electronics system itself, the VME/VMX solution appears more attractive and suitable for this stage of the data acquisition system than a solution based on the high energy physics standard Fastbus. This does not exclude the use of Fastbus crates for digitizing and fast data compression in the front end of the data acquisition system.

The development of CAMAC-based equipment for UA1, and the monitoring and control of the experiment, made extensive use of CAVIAR microcomputers. With the introduction of the VME system, a successor to CAVIAR is being developed based on Apple Macintosh personal computers. This new system, called MacVEE (Microcomputer Applied to the Control of VME Electronic Equipment) allows up to eight VME crates and eight CAMAC crates to be directly memory-mapped into Macintosh address space.

The logical structure of the full readout system is shown in figure 9. It comprises the following four functional busses:

4.1.1) The Detector Bus links the digitizing electronics crates to a controller unit, the bus driver. It is a 16-bit data bus with a few control functions and sequential data access, its implementation depending on the standard of the digitizer electronics. For the old equipment of the UA1 experiment, the detector bus is a Remus vertical branch. For the upgraded detector program non-standard solutions have been chosen; these are the Iarocci STAR system readout (10) with an 8-bit data and 8-bit address special bus, and the microvertex detector LeCroy 1879 TDC readout, where a Fastbus crate with a VME/VMX interface is planned.

4.1.2) The Readout Control Bus is a general-purpose bus hosting all the detector bus driver units and the readout supervisor processor. The bus is used for readout initialization, calibration procedures and multi-processor control.

4.1.3) The Event Builder Bus performs the high speed data transfer between the multievent buffers and a requesting event builder unit memory, under the control of the event manager processor. Both the readout control and the event builder system are based on the VME bus. Physically they consist of several VME crates linked together with a crate interconnect system (figure 7).

4.1.4) The Local Bus is used for private data access between the driver unit, and the corresponding multievent buffer memory and the event builder processor, and its memory. The local bus is implemented by a VMX segment.

The system is composed of the following two modular elements:

4.2.1) The VME Parallel Readout Unit (VPRU) (figure 2) is the basic element of the parallel readout. It consists of a detector bus driver (DBD), a control processor unit CPU and a VME/VMX dual port memory (DPRX) of 128Kb size. This is suitable for storing several event data blocks coming from the associated detector electronics. The DBD and the CPU are connected via the VME port to the readout control bus and operate under the control of the readout supervisor processor.

The dual port memory VME port is connected to the event builder bus. The VMX port shares a VMX segment with the CPU and the DBD that act, respectively, as VMX primary and secondary master. An event unit may not have an associated CPU; in that case all the readout control is performed by the readout supervisor processor. During data acquisition each event unit takes care of the detector data readout and buffering. Data reformatting and/or second level trigger selection are executed at the end of readout by the CPU unit accessing data via its local VMX bus segment. The CPU is also responsible for the monitoring, calibration and system test tasks.

The detector bus driver can be a single VME module, such as the VME Remus branch driver used to read the old system, or it can have a substructure as in the case of the Iarocci STAR readout (figure 3) where an entire VME crate perfoms the function of the input driver. The full parallel readout system consists of 28 event units with VME Remus branch driver, a VME crate for the Iarocci detector and a LeCroy 1879 Fastbus VME/VMX Driver. Figure 7 indicates the physical layout of the VME crates.

4.2.2) The VME Event Builder Unit (VEBU) (figure 4) has a structure symmetric to the event unit. The event unit accomplishes the task of full event data analysis. It consists of a dual port memory accessible from the event builder VME system and from a VMX segment hosting a CPU. Optionally it can be accessed by an output driver unit for data communication. The dual port memory has a size of 256Kb, suitable for storing two full event records for double buffer operations. The CPU and output driver VME ports reside in an independent VME segment bus in order to avoid the event builder bus overloading during the event building data transfer. The task of an event builder is either to process a full event data record for data sampling, executing statistics, histogramming and display applications, or for data communication with the third level trigger and the mass storage. In general, a single event unit is associated with each task and several such units can be modularly inserted into the system without affecting the overall speed performance.

A special event unit is dedicated to the data acquisition and the third level trigger. In this case an output driver module acting as secondary master on the VMX bus accomplishes the data transfer (at 6 Mbyte/sec) between the dual port memory and the 168/E emulator stack. The latter is interfaced to a Camac system via an auxiliary crate controller (PAX) (8) (see figure 5). This represents a temporary solution to the event filter problem.

In the final configuration the 3081/E emulator (11) will be integrated into the system as a VME event unit processor (figure 6). Such a system can also be used for offline data analysis. Additionally new mass storage devices, such as digital video disk, can be included directly into the VME system when commercially available.

5. VME Components

Owing to the specialized functions of some of the units and to the recent introduction of the VMX local bus specification, not all of the VME modules needed for the implementation of this project were commercially available at the start of the data readout improvement program, in October 1983. Consequently an important development program has had to be pursued, partly within the UA1 collaboration and partly by commissioning specified projects to commercial firms. The module specification was finalised in December 1983 (12) and all the prototype modules where developed during the first half of 1984. At the time of writing production and installation are in progress.

The following modules were developed for the UA1 VME readout system:

5.1) Control Processor Unit CPUA1 (13).

The CPUA1 module is the basic processor unit used in all the VME readout subsystems. Its main features are: M68010 8MHz processor, VME/VMX bus master, 256Kb dynamic memory, 8Kb static memory dual ported CPU-VME, NS 16081 6MHz floating point processor, MK68901 peripheral controller (interrupt handler, timer, RS232 serial interface), a variety of control and status registers for CPU identification, address modifier control, VME bus arbiter control and VMX base address setting.

5.2) Dual Port Memory DPRX (14).

The DPRX is used both for the parallel readout and the event builder units. Its main features are: 128Kb/256kb static RAM VME/VMX dual port memory 32-bit data. 400 ns 32-bit word data transfer on both ports, programmable VME memory base address via a VME register, write broadcast mode implemented via address modifier selection (this mode allows the loading of several event builder units by a single DMA transfer, when all the corresponding memory units are set to the same VME address).

A version of the DPRX with 1Mbyte dynamic RAM is used as a local memory extension of an event builder CPU.

5.3) Remus VME/VMX Branch Driver RVMEX (15).

The RVMEX is used in the parallel readout unit as a detector bus driver. It is a multi-path REMUS-VMX, REMUS-VME and VME-VMX bus driver module.

It implements the Remus branch driver read/write functions and, acting as secondary master of the VMX bus, it handles autonomously the readout of a Remus branch and stores the data into an assigned VMX buffer. All of the module's functions are programmable via the VME port.

5.4) Crate Interconnect CI (16).

This module drives a high speed (10.7 Mbyte/sec) vertical bus allowing the linking of a VME crate (master) with up to 15 VME crates (slaves). The vertical bus master crate can operate in two modes (figure 8): the window mode and the DMA mode. In the window mode a master crate CPU can map 64Kb memory of a slave crate into a 64Kb segment of the master crate interconnect module. In the DMA mode any length of data block transfer can be executed under the master control between any two crates on the vertical bus.

The 32-bit data transfer has a three phase pipeline: the source data read (a VME cycle in the source crate), the vertical bus data transmission and the destination data write (a VME cycle in the destination crate).

5.5) 168/E VME/VMX-Camac Fast Data Link (17).

This system consists of two modules, a VME/VMX data output driver and a Camac data input driver. The VME module acts as a secondary master of a VMX segment and provides the DMA transfer between a VME/VMX dual port memory and a Camac module. The latter is read by the 168/E PAX auxiliary controller, linked to the 168/E emulator memory via a 'Greyhound Bus' (8). The maximum data rate is determined by Camac, and is of the order of 4Mbyte/sec. The modules are part of the VME event builder unit dedicated to the third level trigger and mass storage (figure 5).

5.6) VME/VMX Parallel Input Output VXPIO (18).

This is a general-purpose input-output module. It performs synchronous and/or asynchronous 16-bit TTL/NIM parallel I/O via a front panel connection and either VME or VMX ports. Both input and output are driven by a high speed FIFO of 512 16-bit words. This allows for the special application of the module as a data communication unit with an external system, or as a programmable output sequencer or as a logic/ state analyzer.

5.7) VME Interrupt Vector Generator IVG (19).

This module generates interrupts from 8 TTL/NIM front panel inputs at two presettable levels. For each channel the VME interrupt vector, the mask and a semaphore flag are programmable. Each input provides a channel status output signal and an internal counter allows the detection of double 'click' situations.

Conclusion

In an experiment such as UA1, the detector complexity, high trigger rates, and large data volume per event require distributed intelligence at many stages of the readout system. In addition a very modular and easily upgradable system structure is desirable, so that developments in technology can be readily applied to improve system performance.

It is believed that these aims can be achieved by the introduction of a readout system based on the industrial VME bus standard. This approach appears to be powerful, flexible, and cost-effective, and to prepare the way for the efficent exploitation of the enhanced potential of the UA1 detector in the future.

Acknowledgements

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Finally we are indebted to C. Rubbia for much encouragement and support in all the phases of this project.

References

1) VME Bus. MVEBS/D1, Rev. B Aug. 82 Motorola. VMX Bus, Rev. A Nov. 83 Motorola;
2) UA1 proposal: A 4π solid-angle detector for the SPS used as a proton-antiproton collider at centre-of-mass energy of 540 Gev, CERN/SPSC 78-6;
M. Barranco Luque et al., Nucl. Instrum. Methods 176 (1980) 175;
M. Calvetti et al., Nucl. Instrum. Methods 176 (1980) 255;
K. Eggert et al., Nucl. Instrum. Methods 176 (1980) 217,233;
A. Astbury, Phys. Scr. 23 (1981) 397;
M. Calvetti, The UA1 central detector, Proc. Intern. Conf. on Instrumentation for colliding beam physics (SLAC, Stanford, 1982) (SLAC-250, Stanford, 1982) p. 16;
M. J. Corden et al., Rutherford & Appleton Laboratory Report RL-83-116 (1983);
A. Astbury et al., Rutherford & Appleton Laboratory Report RL-84-025 (1984);
3) S. Cittolin, The UA1 data acquisition system, Proc. Intern. Conf. on Instrumentation for collidingbeam physics (SLAC, Stanford, 1982) (SLAC-250, Stanford, 1982) p. 151;
S. Cittolin, M. Demoulin, W.J. Haynes, W. Jank, J.P. Porte, P. Rossi, V. Vuillemin, The UA1 Data-Acquisition and Online-Monitoring System. To be submitted to Nucl. Instrum. Methods;
4) CERN/SPSC/83-48, SPSC/P92 Aug. 83;
5) P.J. Ponting, A guide to Romulus/Remus data-acquisition systems, (preprint CERN-EP/80-01 1984);

6) S. Cittolin and B. Lofstedt, A Remus crate controller for the autonomous processing of multichannel data streams. Proc. Topical Conf. on the Application of Microprocessors to High-Energy Physics Experiments, CERN 81-07 (CERN, Geneva, 1981), p. 91;
7) L.O. Hertzberger, J.C. Vermeulen, L.G. Wiggers, FAMP: an example of multiprocessing in High Energy Physics. Paper presented at: Three-day in-depth review on the impact of specialized processors in elementary particle physics (Padua 1983), p. 229;
8) J.T. Carrol, S. Cittolin, M. Demoulin, A. Fucci, B. Martin,A. Norton,J.-P Porte, P. Ross and K. M. Storr, Data acquisition using 168/E, Paper presented at: Three-day in-depth review on the impact of specialized processors in elementary particle physics (Padua, 1983), p. 47;
9) S. Cittolin and B.G. Taylor, CAVIAR: Interactive microcomputer control and monitoring of multi-crate CAMAC systems, Proc. Conf. on microprocessors in automation and communications, Univ. of Kent, 1978 (IERE No. 41, London, 1978), p. 309;
S. Cittolin and B.G. Taylor, Super CAVIAR: Memory mapping the general-purpose microcomputer. Proc. Topical Conf. on the Application of Microprocessors to High-Energy Physics Eperiments. CERN 81-07 (CERN, Geneva, 1981), p. 533;
10) S. Centro , STAR system description, (Padua INFN note 1984) PD. 29.5.84 ;
11) P.F. Kunz et al., The 3081/E Processor. Paper presented at this conference;
12) S. Centro, S. Cittolin, M. Demoulin, W.J. Haynes, L.O. Hertzberger, W. Jank, E. Pietarinen, P. Rossi and C. Rubbia, The UA1 VME readout system, UA1 technical note, (CERN UA1 TN-83/103) 1983;
13) The VME/VMX bus CPU module, DSSECPUA1 PHM 1.0 June 1984, Data Sud Systems S.A. 22, rue de CLaret VII 34007 Montpellier France;
14) The VME/VMX bus Dual Port Memory, DSSECDPRX June 1984, Data Sud Systems S.A. 22, rue de Claret VII 34007 Montpellier France;
15) C. Engster and L.G. van Koningsveld. REMUS-VME-VMX branch driver (RVMEX) type V385, CERN-EP 1984 note to be puplished;
16) E. Pietarinen. The VME Crate Interconnect module, UA1 technical note to be published
17) P. Gallno, B. Martin,VME-VMX-CAMAC high speed long distance data link, CERN-DD 1984 note to be published;
18) VME-VMX Parallel Input Output, LAPP 1984 note to be published;
19) A. Arignon, Ph. Farthouat, VME Interrupt Vector Generator, DPhPE-SEIPE CENS 91191 GIF sur Yvette Cedex (6).908.33.86;
20) B. Hallgren,H. Verweij,IEEE Trans. Nucl. Sci. NS-27(1980)33; see also CTD, CERN-EP 279 (1982);

Table 1. Number of Channels and Data/Event

Detector	No. Channels	Raw Data (Bytes)	Formatted Data (Bytes)
Central Detector	6200	1600000	≈80000
Hadron Calorimeter	1200	2400	2400
Electromagnetic Cal.	2200	4400	4400
Cal. Position Detector	4000	8000	8000
Forward Chamber	2000	32000	8000
Muon Chamber	6000	≈2000	2000
Iarocci Tube	40000	40000	≈4000

Average Event Size	100 Kb
Parallel Readout and Data Reduction dead time	3÷40 ms
Third Level Trigger Maximum Rate (90% Efficiency)	30 Hz
Event Data Mass Storage Maximum rate	4 Hz

Table 2. Data Acquisition Components

VME Modules	50	Dual Port Memory VME/VMX DPRX 128/256Kb Static RAM.	
	12	VME Crate Interconnect.	
	12	256Kb EPROM.	
	10	512Kb Dynamic RAM.	
	20	Parallel I/O, Interrupt Generator, Graphics	
Readout	200	Camac crates.	Data Digitization
	28	Remus branches.	Parallel Readout
	12	VME crates.	Readout Data Handling
8 bit Processors	200	M6800 µP .	Electronics Control
	110	Signetics 8X300 µP.	Data Reduction/Formatting
	20	Super Caviars.	Equipment Test and Control
16 bit Processors	7	FAMP M68000 10MHz.	Muon Second Level Trigger
	60	VME CPUA1 M68010 8MHz. 256Kb, NS 16081 FP.	Parallel Readout, Data Formatting and Event Data Sampling
32 bit Processors	6	168/E IBM Emulators.	Event Filter and Online Monitor
Main Computers	2	NORD 100/500 2 Mbyte	Data Acquisition and
	6	6250 BPI 125 IPS	Software Development

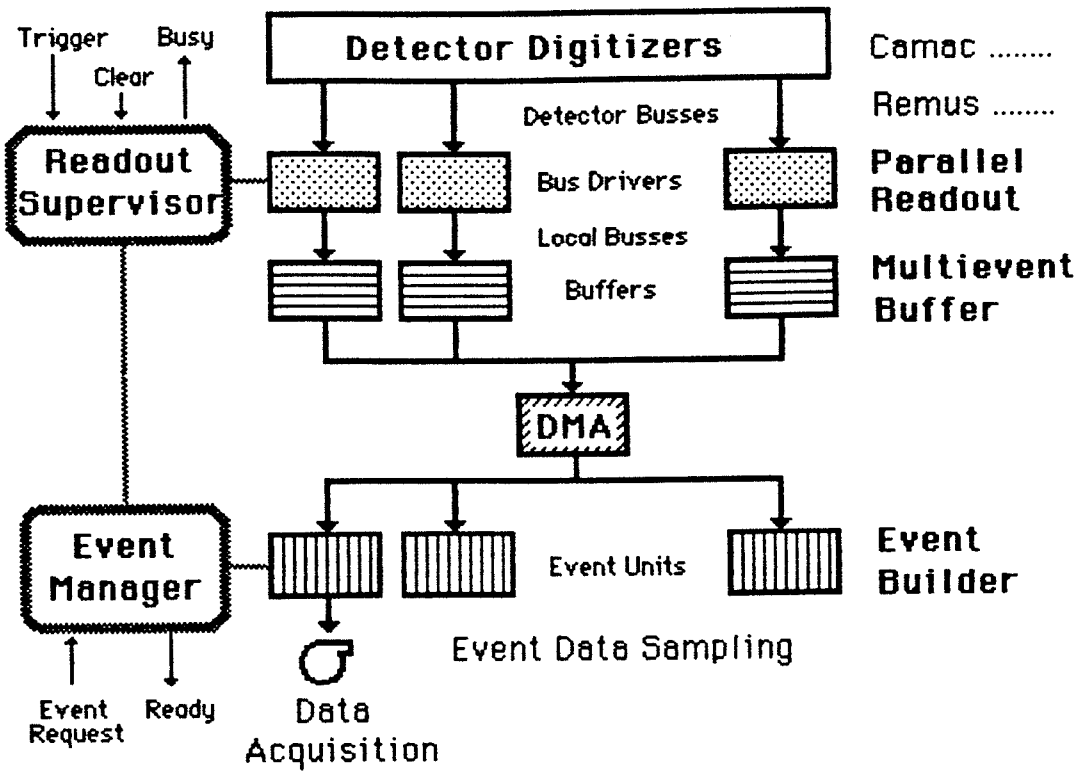

Figure 1. Data Readout Structure

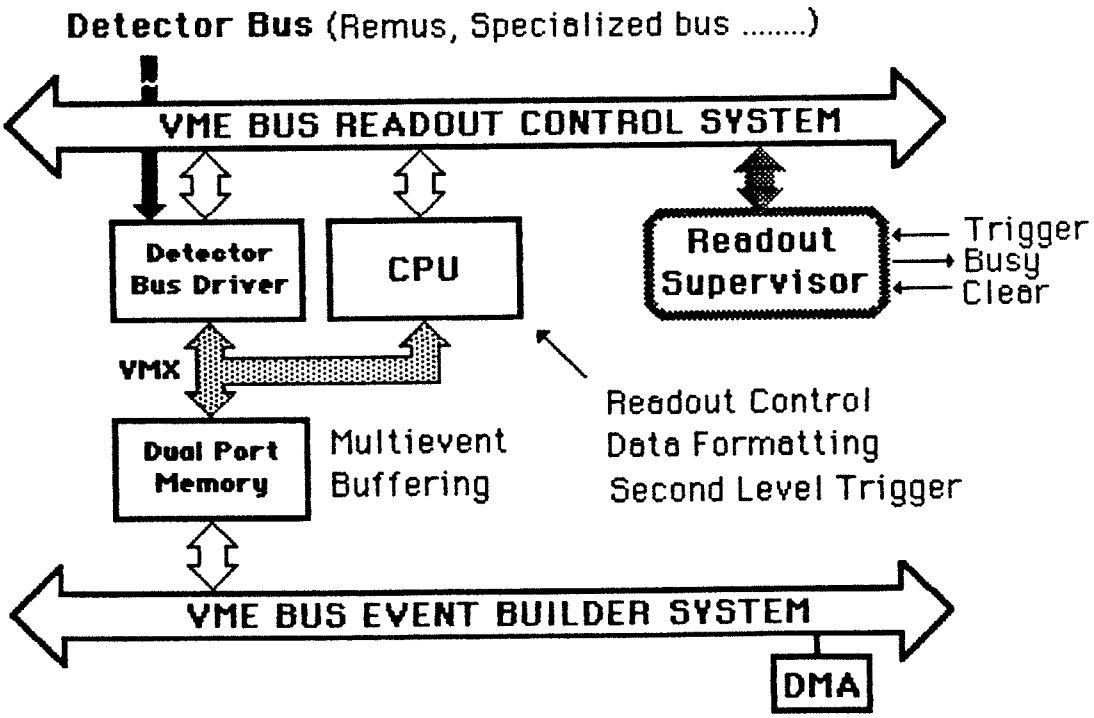

Figure 2. VME Parallel Readout Unit

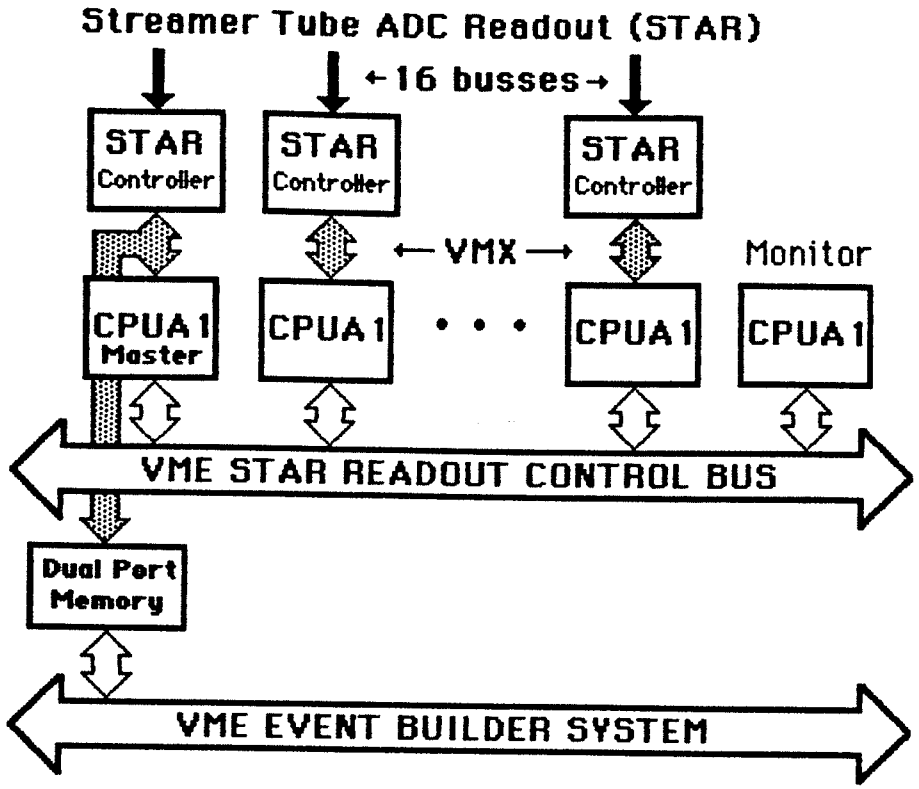

Figure 3. VME STAR Parallel Readout Unit

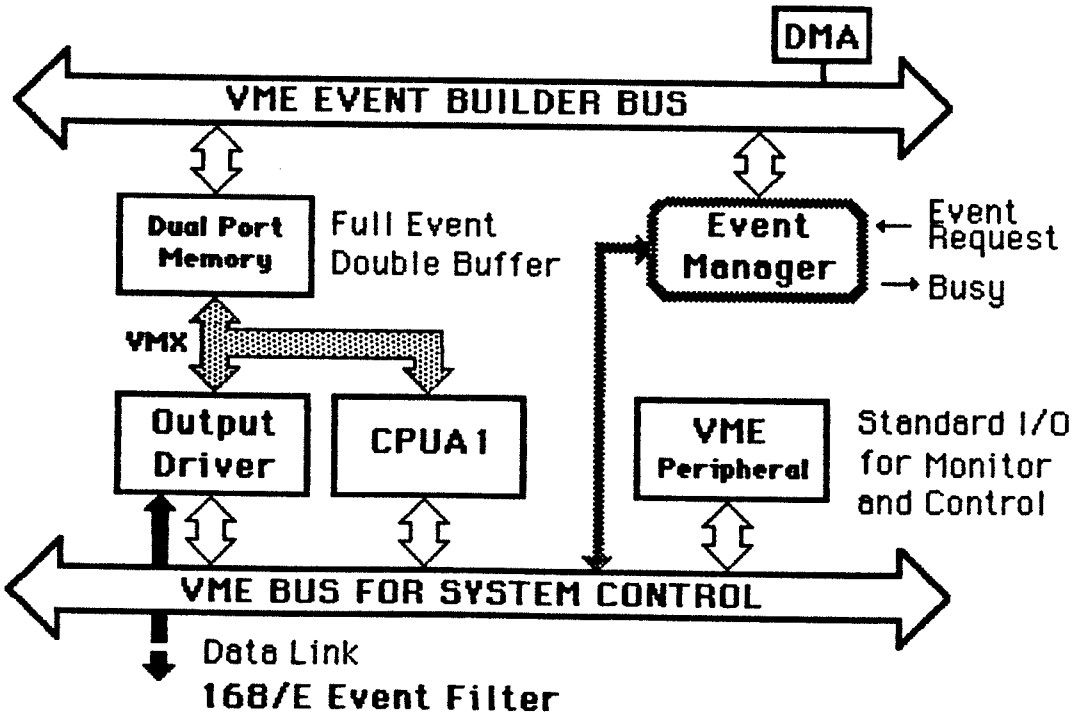

Figure 4. VME Event Builder Unit

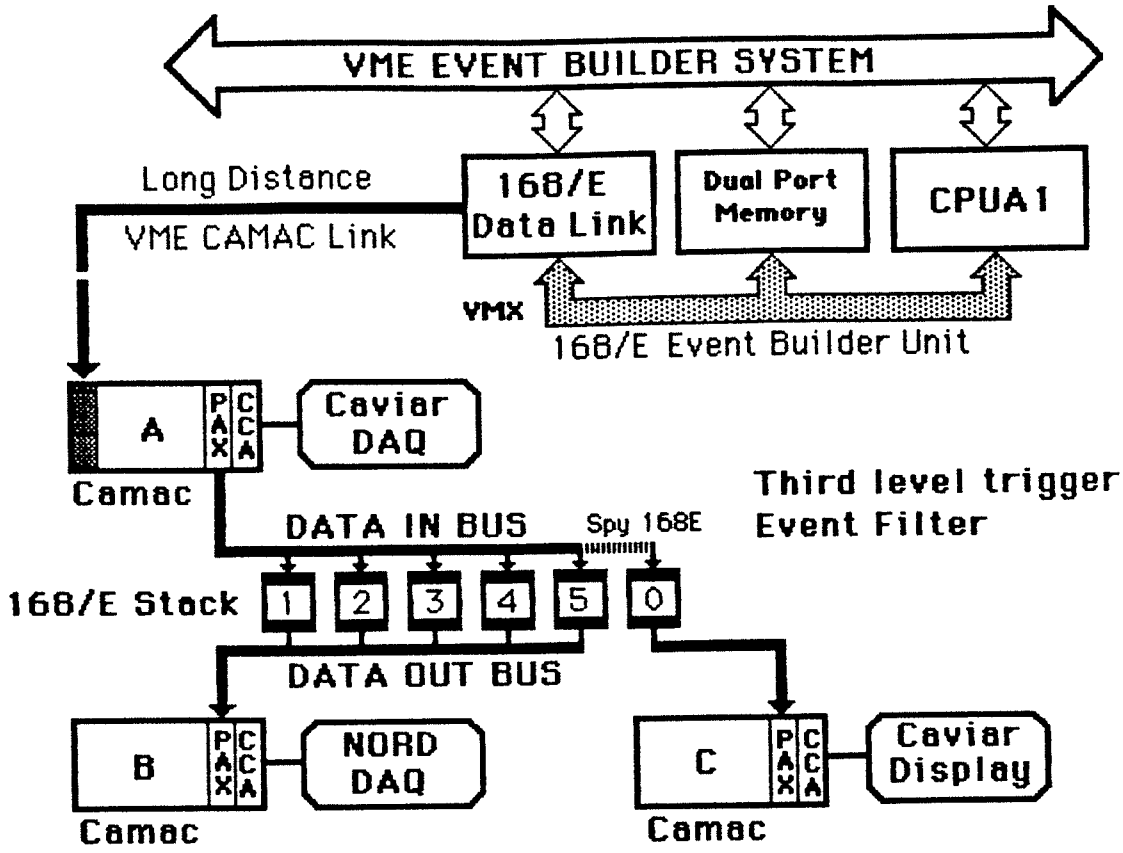

Figure 5. VME-VMX-CAMAC Link. 168/E Event Builder Unit

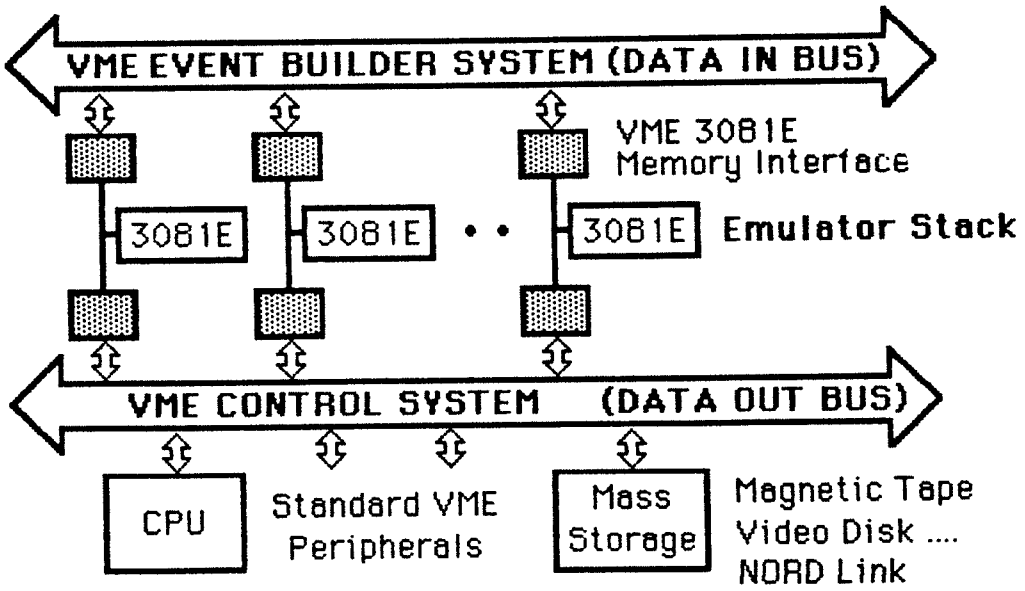

Figure 6. 3081/E VME Event Builder Stack

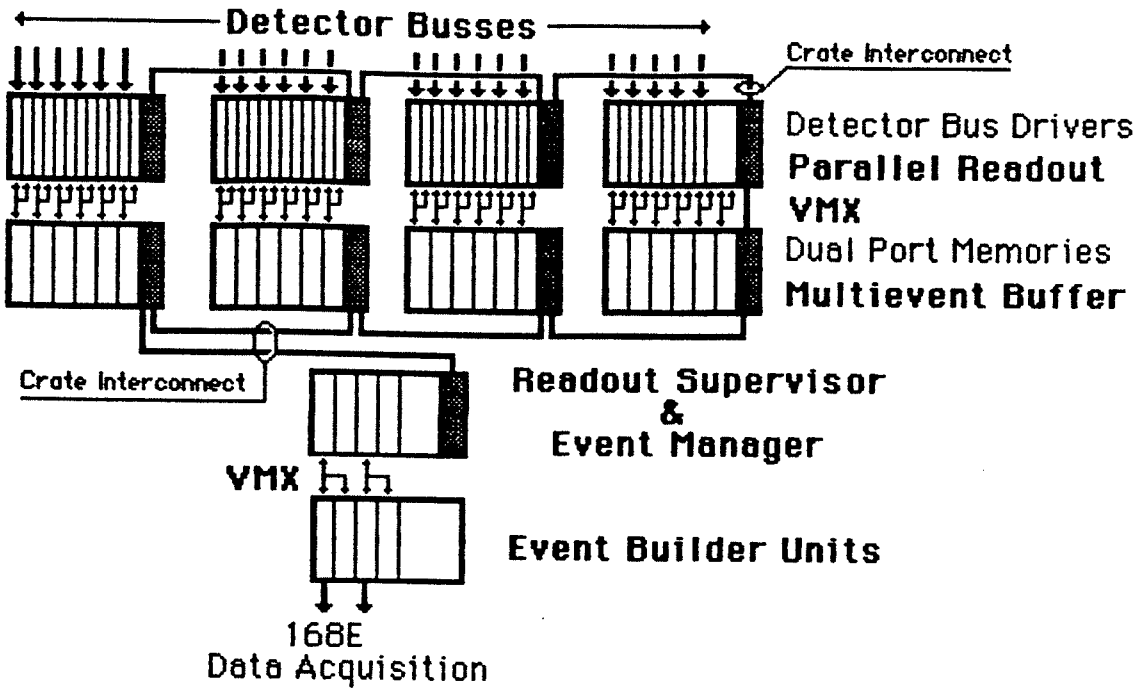

Figure 7. VME Crate Physical Layout

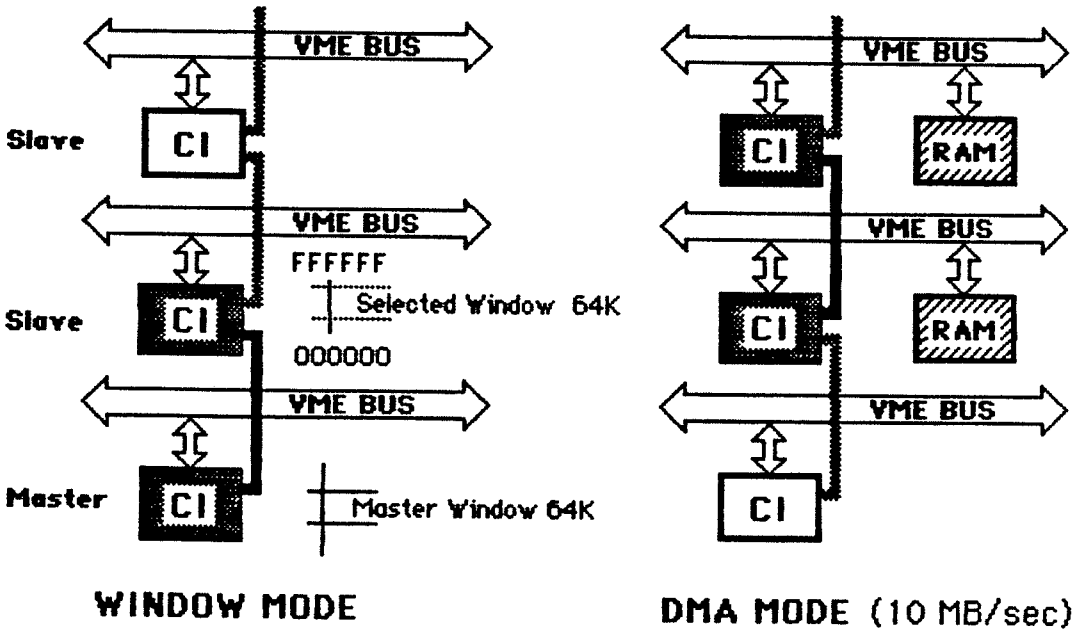

Figure 8. Crate Interconnect

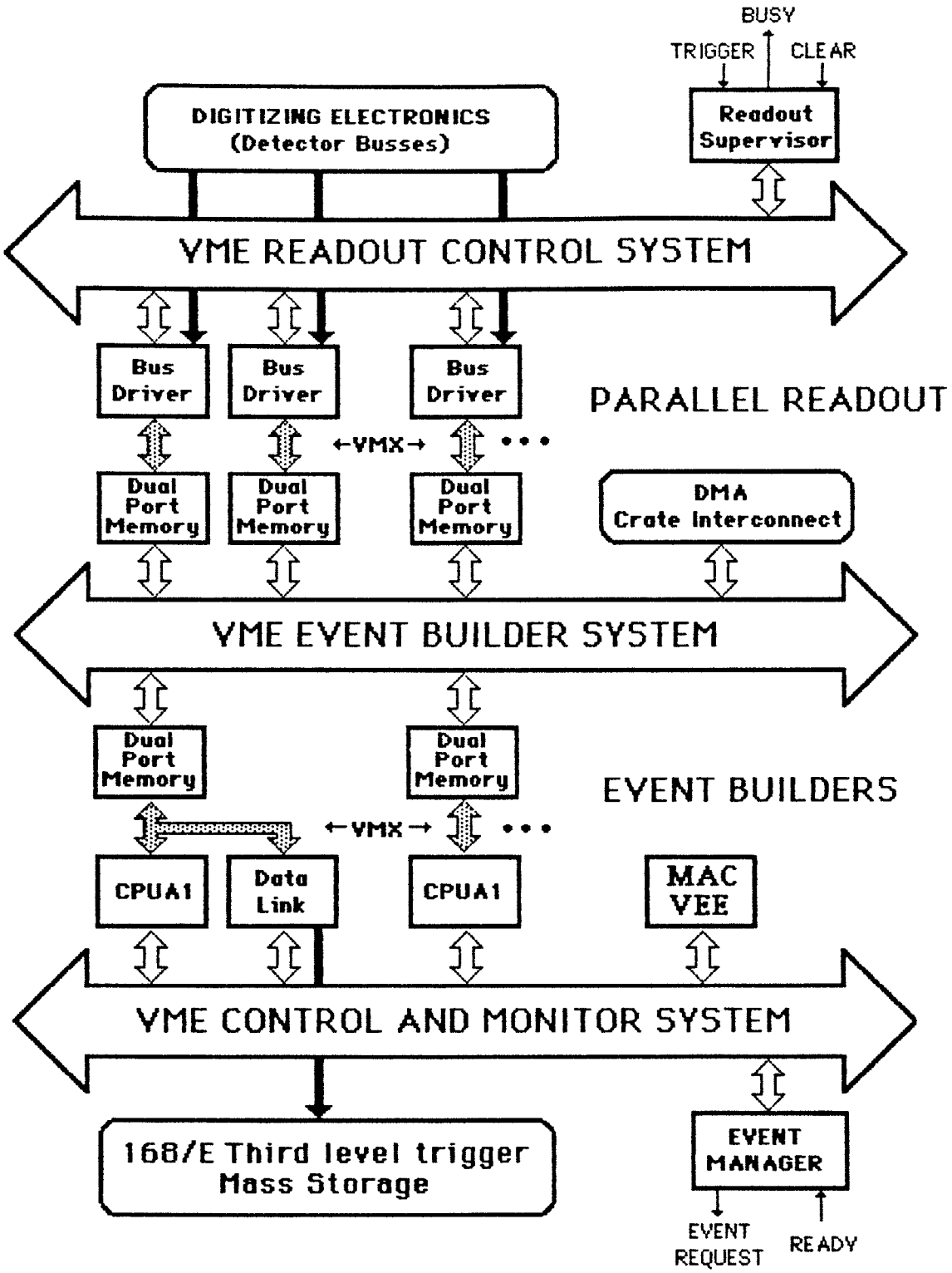

Figure 9. VME Readout Logical Layout