Electronics R&D for CMS Upgrade Fast Timing Muon detector

(on behalf of the CMS collaboration)

I.Laktineh & H.Mathez

OUTLINE

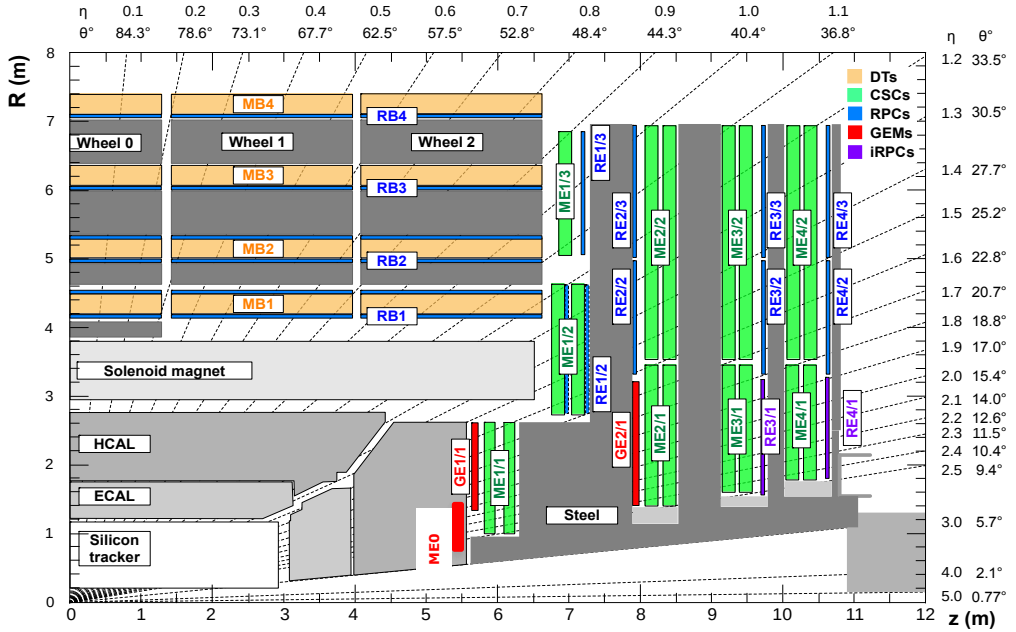
- CMS muon detectors upgrade
- MRPC and FTM detectors
- Fast-Timing Electronics R&D
- Conclusion

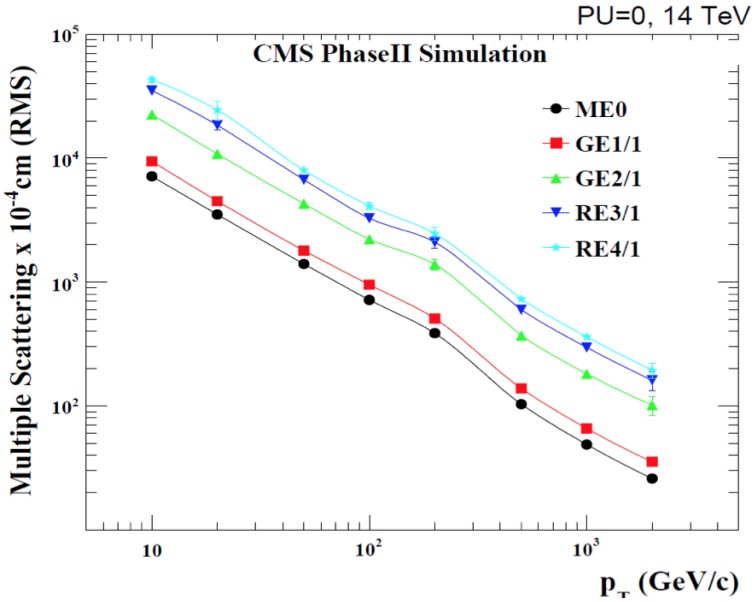
Goals of the CMS high η muon detector upgrade

→Improve on muon trigger efficiency in high η region by increasing redundancy (only CSC are present in Run1 phase)
→With the luminosity and pile-up increase at HL-LHC, one needs to keep the same trigger rate without increasing Pt cuts

❑High rate capability detectors are needed
❑Space and time resolution are the key words

MPGD could provide excellent space resolution and sub nanosecond time resolution, while MRPC could provide excellent timing sub 100 ps. MPGD could stand very high rates (> 1 MHz/cm2). MRPC using low-resistive material electrodes could stand high rates (> 10 kHz/cm2) .

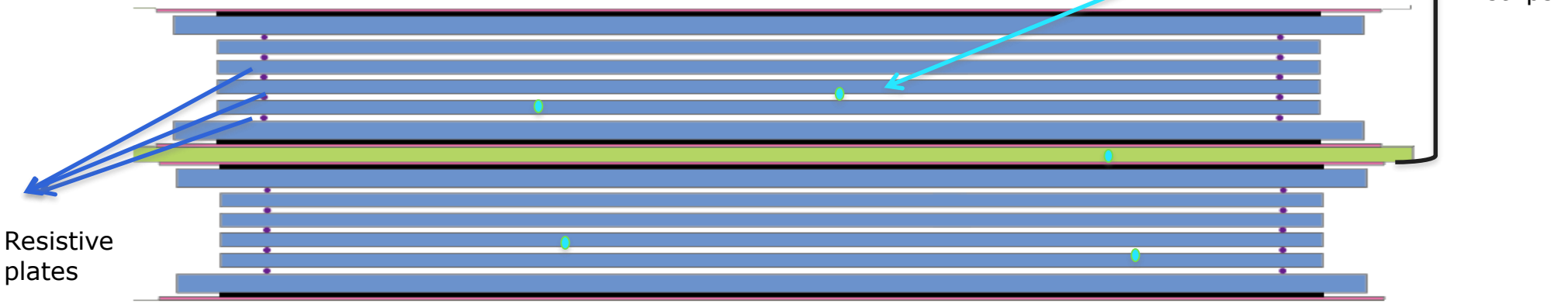




iRPC: well known technology, suited for large detection surface and moderate particle rate.
Charge: few pC
Two scenarios are proposed:

- **Double single-gap RPC**: **time resolution < 1ns**

- **Double multi-gap RPC: time resolution < 100 ps**

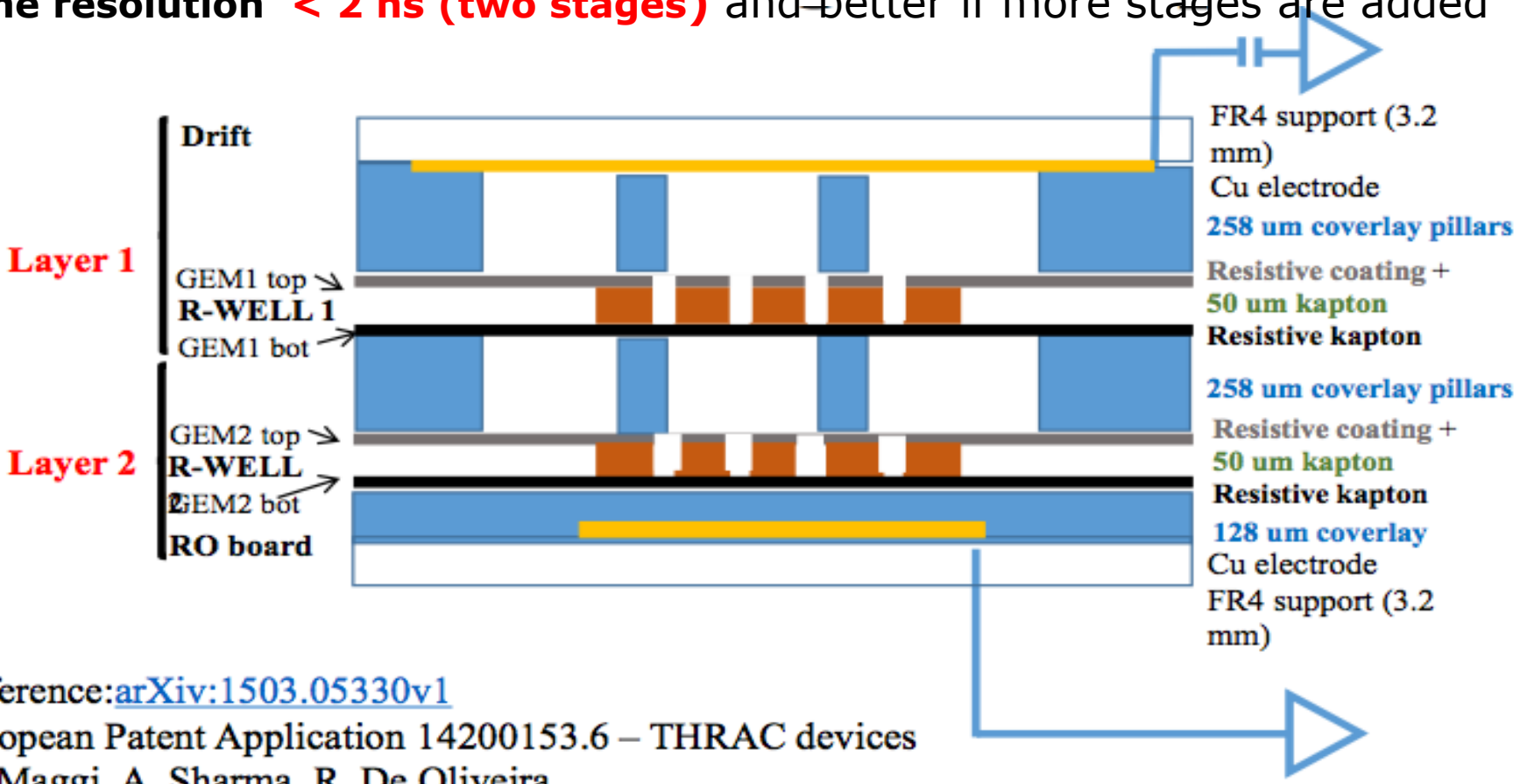


Fast-Timing detectors

Fast Timing Micropattern (FTM) detector : new technology, based on combining GEM and resistive MICROMEGAS concepts. Several stages are needed, each with with small drift space.

Charge: few tens of fC.

time resolution **< 2 ns (two stages)** and better if more stages are added

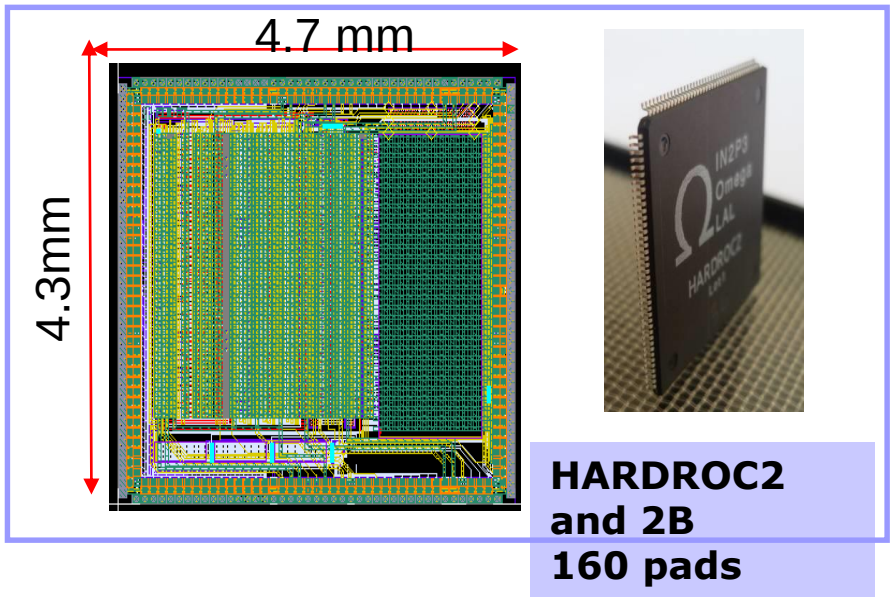


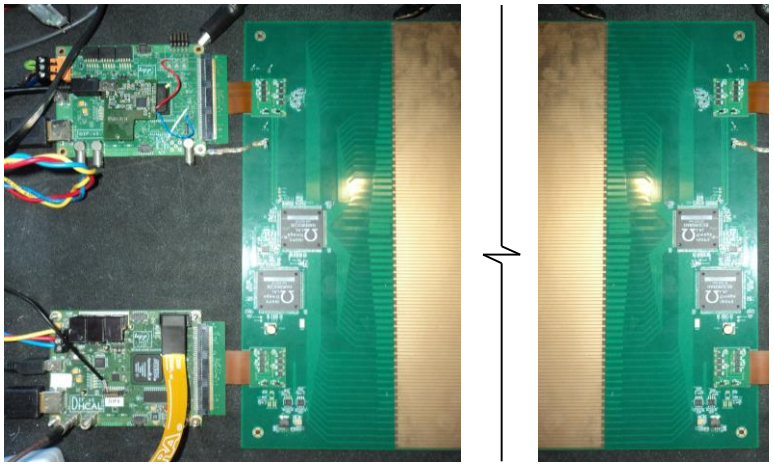
Reference:arXiv:1503.05330v1
European Patent Application 14200153.6 – THRAC devices
M. Maggi, A. Sharma, R. De Oliveira

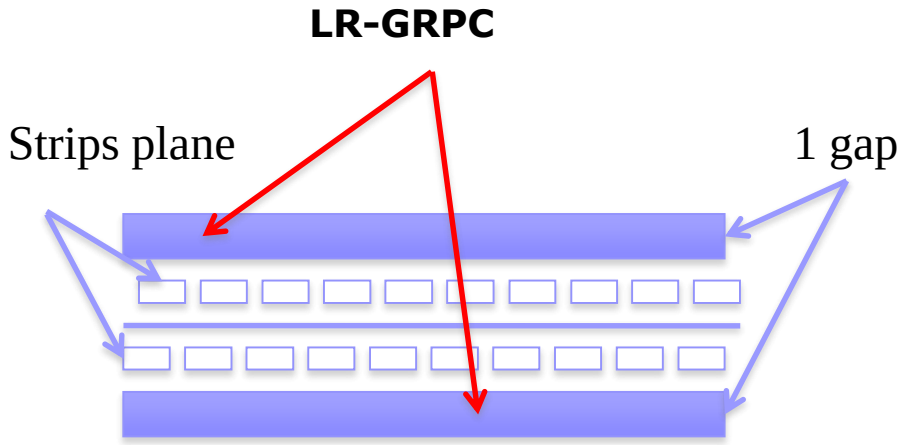
Electronics for double single-gap GRPC

HARDROC ASICs :
developed by OMEGA group,
SiGe technology, 64 ch, 3 thresholds,
dynamic range 10 fC-15pC,
low power consumption < 1mW/ch

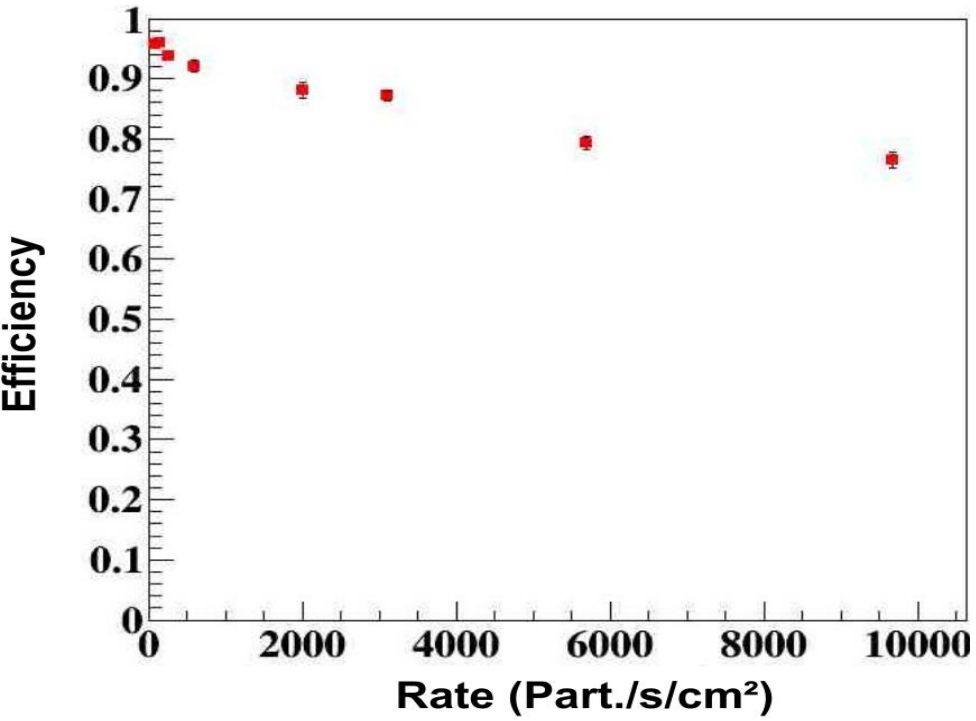
PCB :
PCB with strips of 2.5 mm pitch

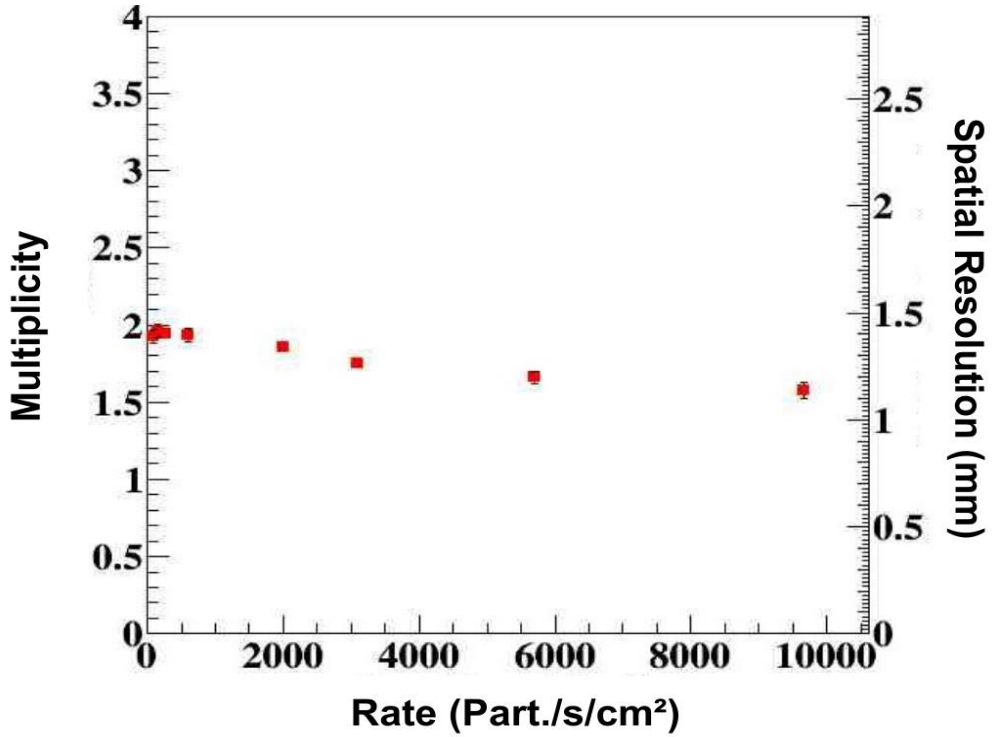






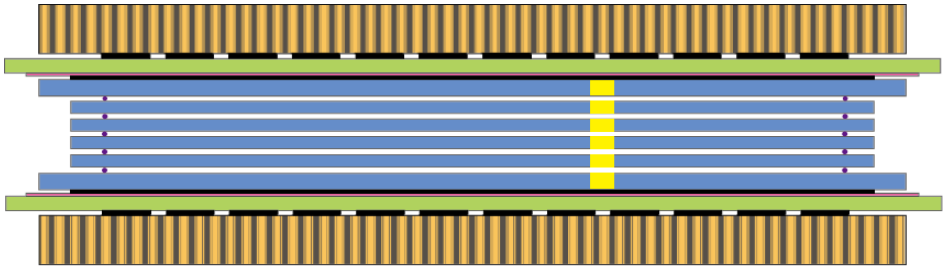
Efficiency, cluster size and spatial resolution

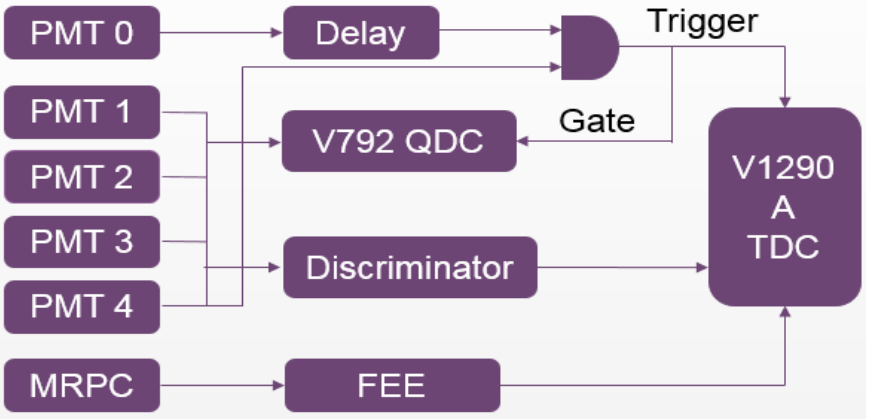




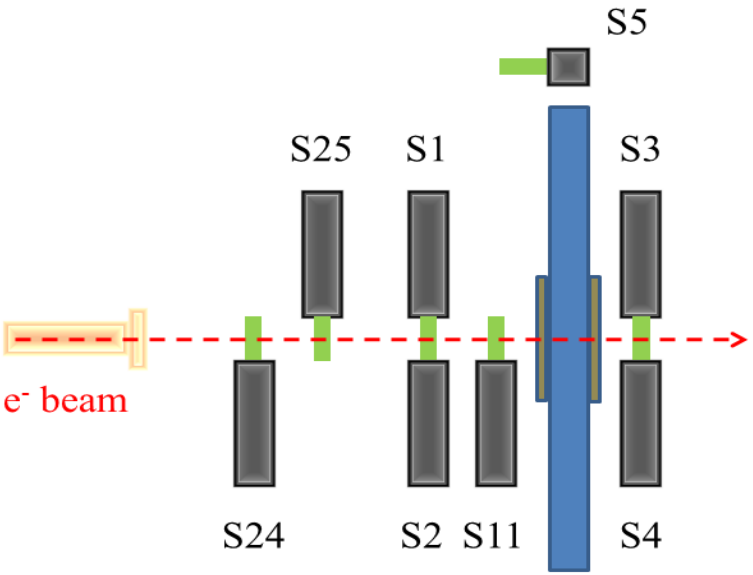
PS-CERN TB
HV: 7.2 kV
gas mixture: TFE(93%), CO2(5%), SF6(2%)

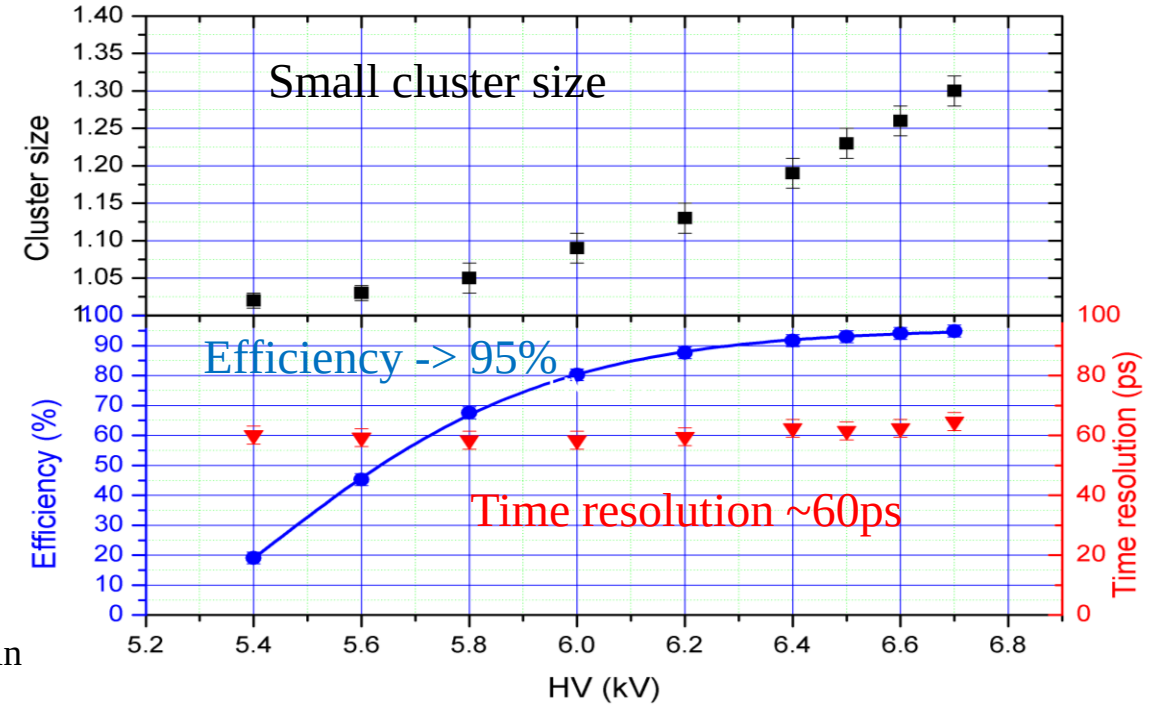
Electronics for double multigap GRPC





Beam test @ HZDR, Sep, 2015





Gas supply : 90% Freon, 5% iso-butane, 5% SF6, 50ml/min

Electronics for Multi-gap CMS-GRPC

PETIROC2

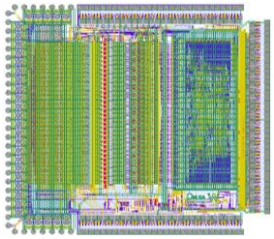
- Front-end (0.35µm SiGe technology)

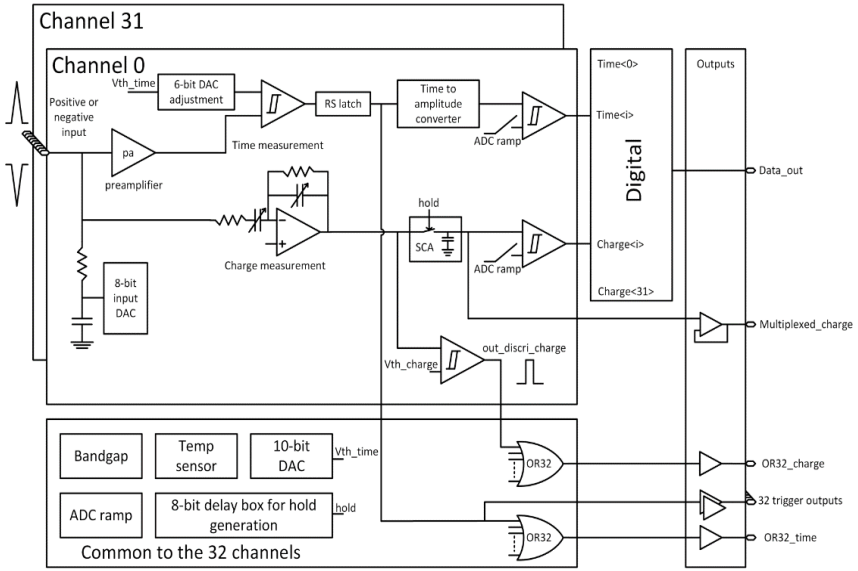
SiGe fast amplifier (BW> 1GHz), DC coupled to detector
Fast **SiGe** discriminator

- Time of Flight read-out chip with embedded TDC (25 ps bin) and ADC
- Dynamic range: 160 fC up to 400 pC
- 32 channels (negative input)

32 trigger outputs
NOR32_chrage
NOR32 time
Charge measurement over 10 bits
Time measurement over 10 bits
One multiplexed charge output

- Power consumption 6 mW/ch



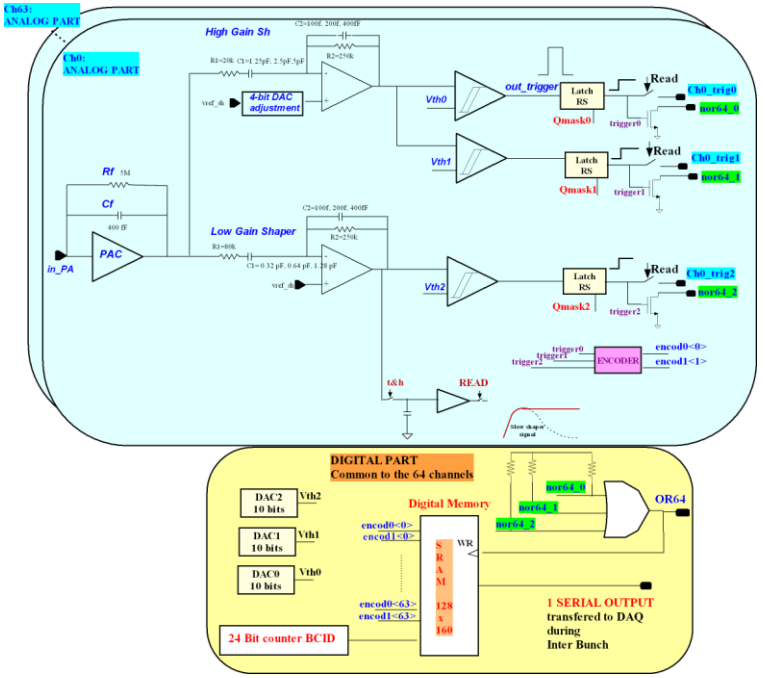


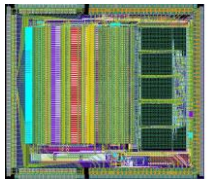
MICROROC

- Same as HARDROC but with charge preamp input stage + HV protection [R. Gaglione] and slower shaping + 4bit DAC/channel [N. Seguin]
- Preamp optimized for Cd=80 pF, noise = 0.2 fC. Cf=0.4pF Rf=5M

–2.5 mV/fC

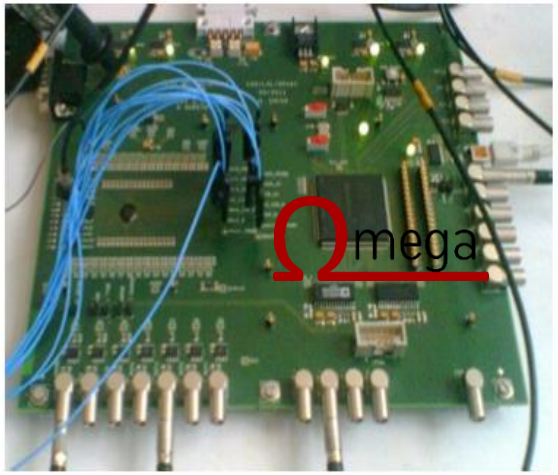
- Maximum input charge : 500 fC
- Bi-gain shaper (G1-G4), peaking tunable 50-200 ns (2 bits)
- 3 thresholds
  - Lowest threshold ~2 fC

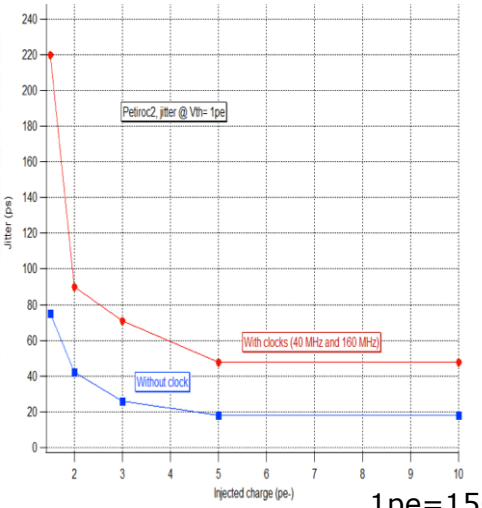




Electronics for Multi-gap CMS-GRPC

- PETIROC ASIC : 32-channel, high bandwidth preamp (GBWP> 10 GHz), <3 mW/ch, dual time and charge measurement (160 fC-400 pC) vey fast and low-**jitter < 25 ps rms**





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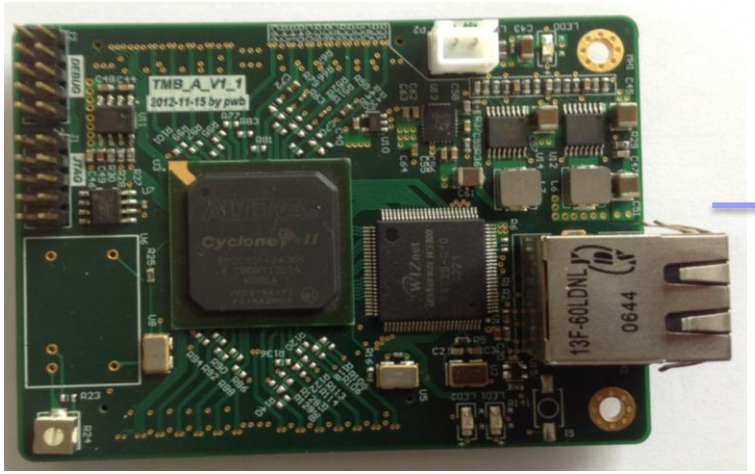
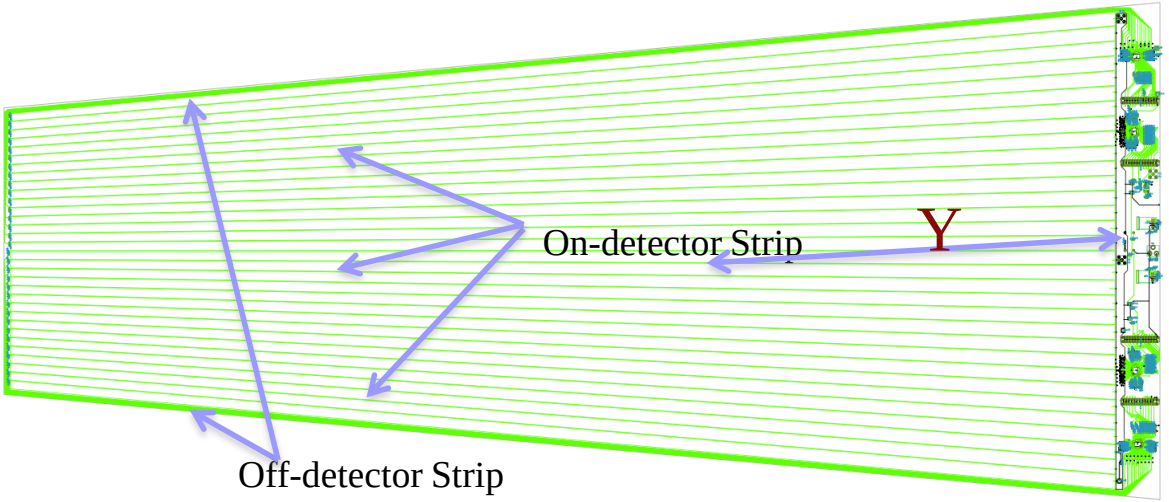


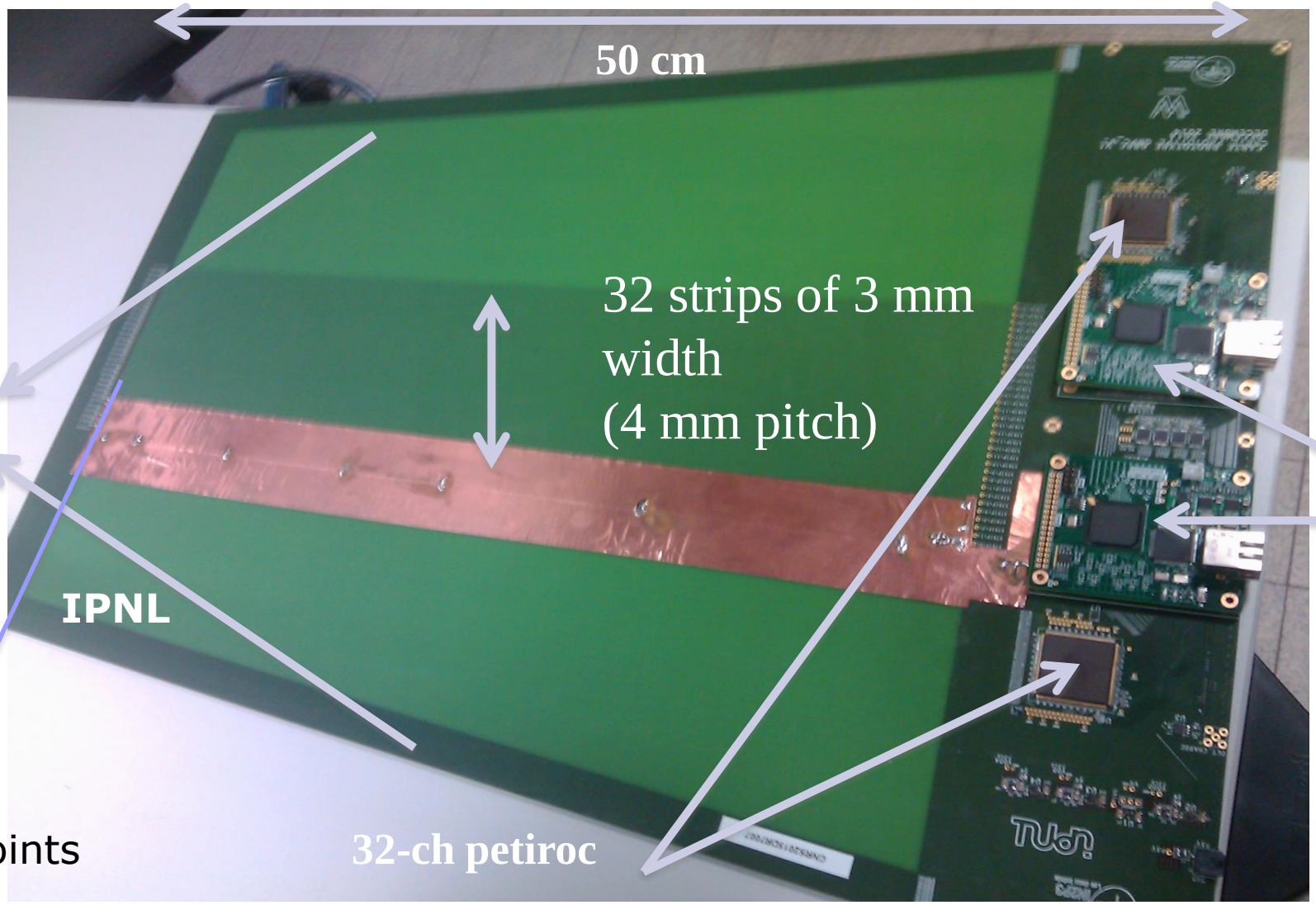
- 24-ch, TDC of 25 ps time resolution developed by the Tsinghua university will be used to demonstrate the RPC/MRPC time capability

- New PCB with pick-up strips read from both sides is being designed information with the aim to achieve Y-position determination **$Y= L/2-v*(t_2-t_1)/2$**. Time resolution can be measured: **$(t_1+t_2)- L/v$**



Electronics for Multi-gap CMS-GRPC

A PCB was conceived to host : Pickup strips, 2 PETIROC, 2 TDC
A DAQ system was developed. The PCB is intended to equip large chambers



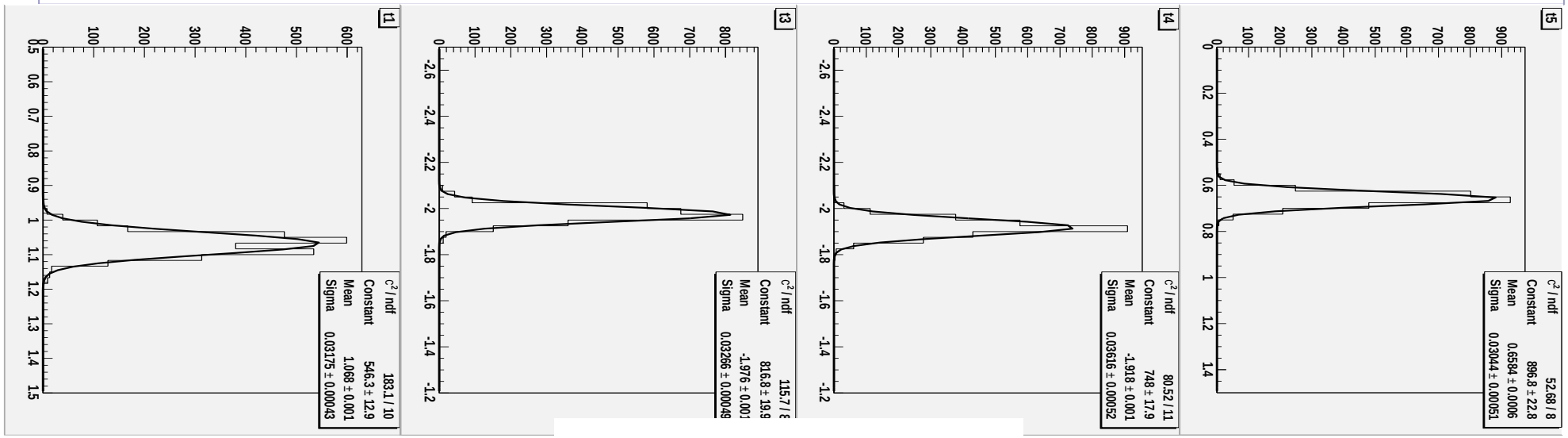
Return strips outside the detector

Tsinghua FPGA TDC

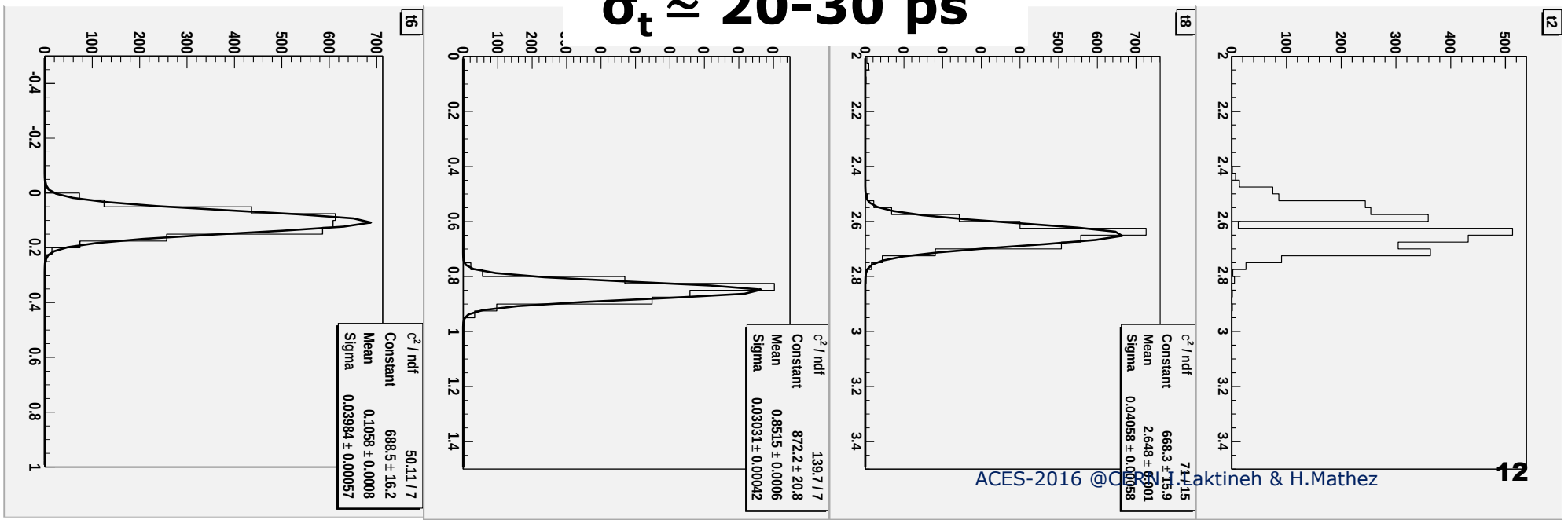
Test points

Electronics for Multi-gap CMS-GRPC

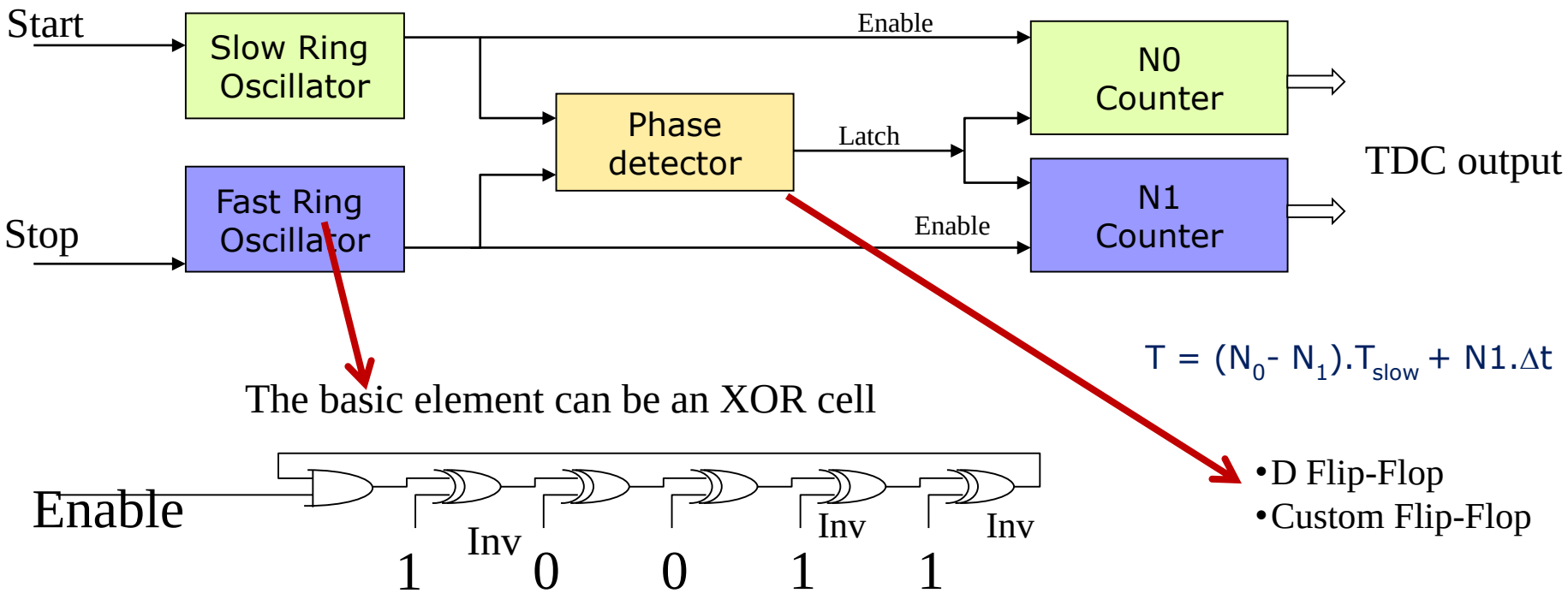
Injecting charge on test points and then recording time difference $\Delta T = T_2 - T_1$



$\sigma_t \simeq$ 20-30 ps



To ensure an excellent timing measurement while reducing, jitters, power consumption, we proposed to include the TDC in PETIROC. One TDC based on the Vernier architecture that was successfully tested on FPGA (*10 ps RMS resolution over a range of 1 ns*) is being studied.



Electronics for Multi-gap CMS-GRPC
(ASIC Design)

IBM130

Oscillators:

- Period Range ~[2.8 ns , 3,1 ns] pour 20° C < Temp < 60° C
- Tuneable range (LSB) : ~ 200 ps over 512 code (0.4 ps/code)
- Good agreement with simulations

Phase detector with custom Flip-Flop (S-curves):

- 6 ps width
- RMS resolution = 1 ps (including generator jitter)

- Over a dynamic range of 1ns all the steps are well separated
  - LSB = 65 ps
  - DR = 1 ns

Main limitations:

- Dead Time
- Cumulated Jitter
  - Power supply Noise
  - Transistor Noise

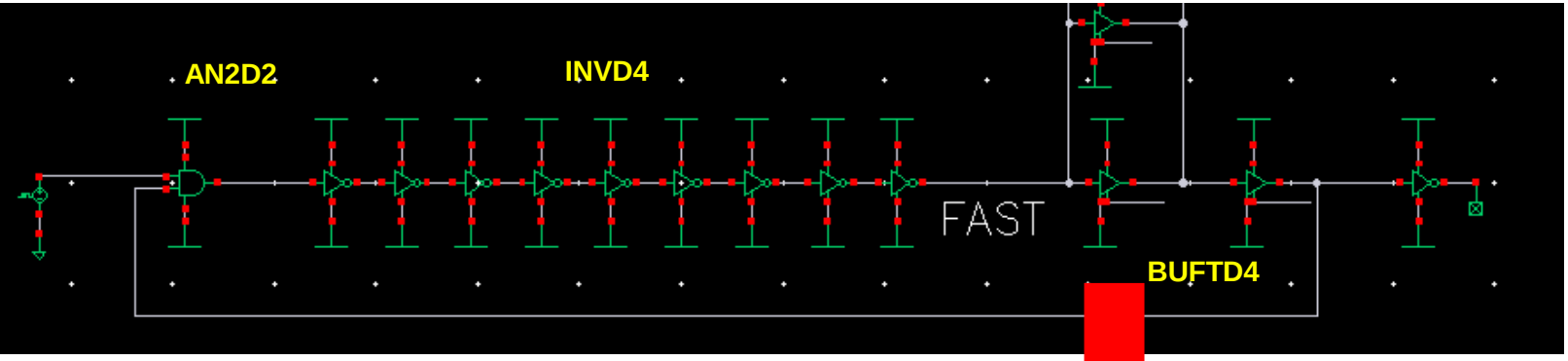
$$J_{XOR}(RMS) = \frac{LSB^{\frac{3}{2}}}{K*\sqrt{T_0*2*N_s}}$$

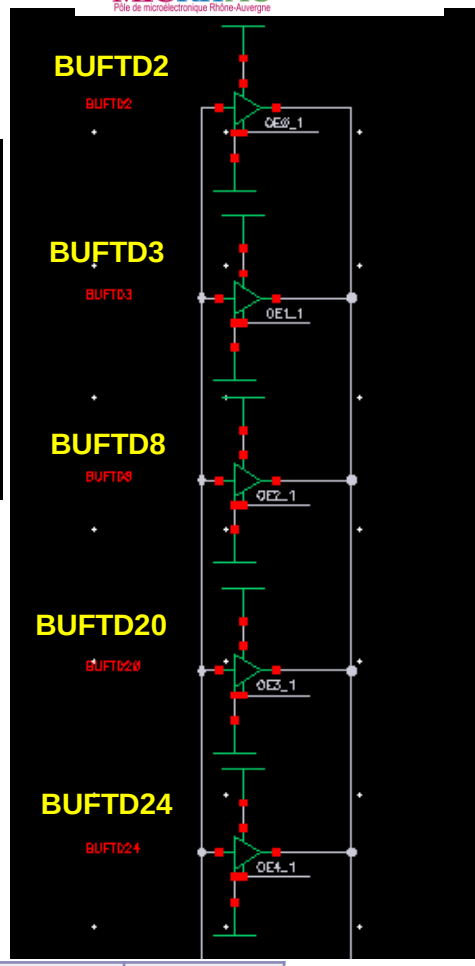
$$J_{@Edge\ number}(RMS) = J_{XOR} * \sqrt{2 * N_s * E_N}$$

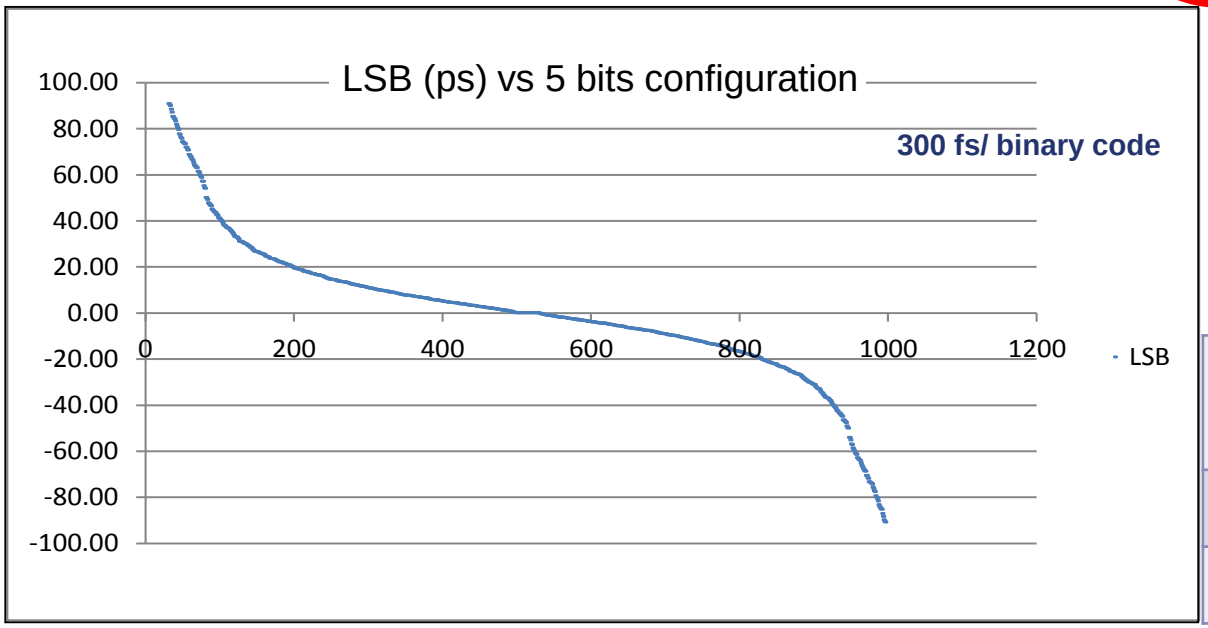
- K : fraction of LSB
- T0 oscillation frequency
- Ns : number of stage in the RO
- To = 2ns, LSB = 20ps, K = 10, Ns = 9
- E_N : Edge Number
- Jxor (RMS) = 47 fs
- $J_{xor\text{-}IBM}$ (RMS) = 82 fs → LSB = 30ps, Design new XOR gate

Electronics for Multi-gap CMS-GRPC
(ASIC Design)

TSMC130



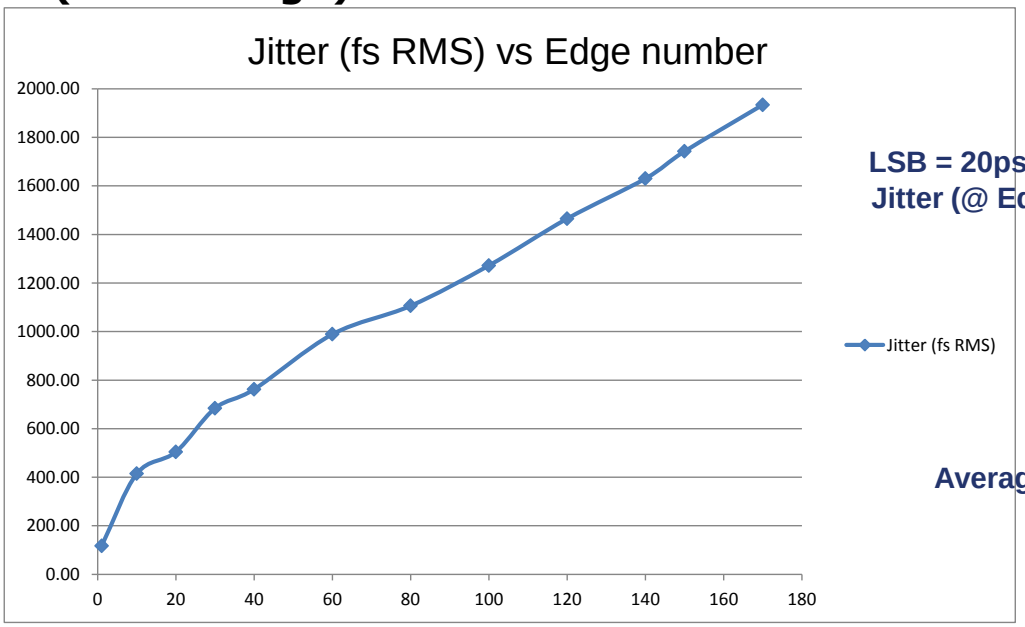




	F (MHz)	T (ps)	Tp (ps)
Max	1140	875,7	43,4
Min	961	1040,9	36,5

Electronics for Multi-gap CMS-GRPC
(ASIC Design)

Simulated

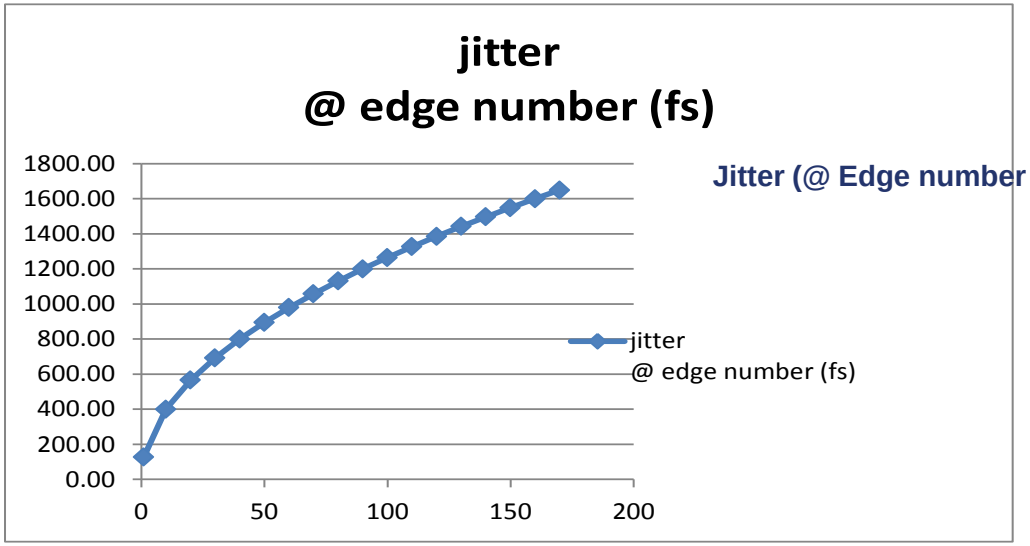


LSB = 20ps, jitter < 2ps
Jitter (@ Edge number = 170) = 1,934ps

Average Jitter per gate = 32 fs

Calculated

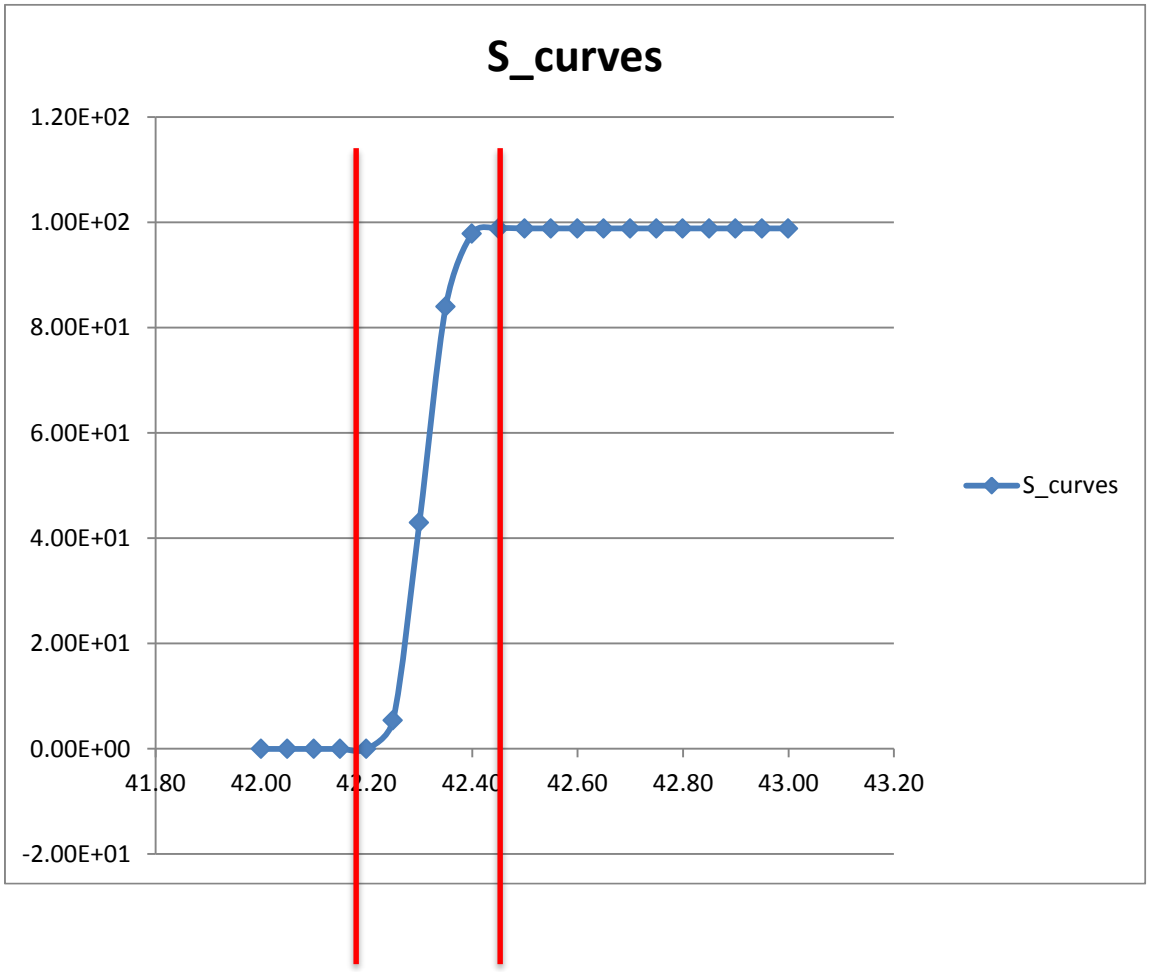
(F=1,1GHz, Jitter/Gate=40fs)



Jitter (@ Edge number = 170) = 1,649ps

S-curves for Phase detector based on 2 D Flip-Flop + And Gate

250 fs min-max, 40 fs RMS



Conclusions

Both detectors and electronics R&D for the muon detector upgrade of CMS are in advanced stage,

Fast Timing detectors are important asset to improve on trigger and physics performance.

Electronics to achieve time resolution better than 50 ps for large surface detectors is ongoing.

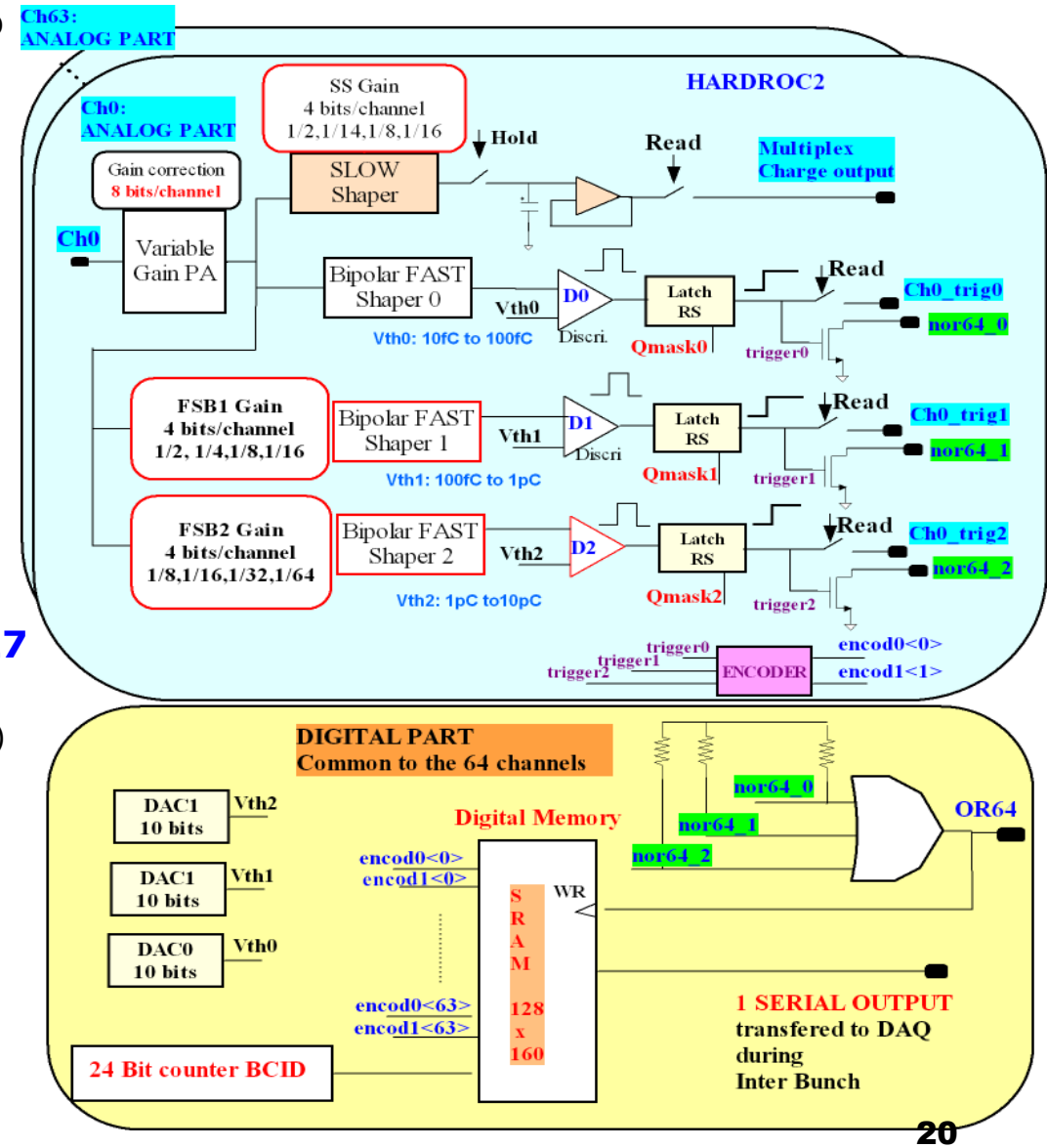
Preliminary results are encouraging but there is still much to do to validate the nice results on large prototypes.

Backup Slides

HARDROC2

http://omega.in2p3.fr/

- **64 inputs**
- Current preamp with **8 bits** gain correct: G=0 to 255 (analog G=0 to 2)
- **3 shapers**, variable Rf,Cf and gains:
  - Fsb1, G= ½,**1/4**,1/8,1/16
  - Fsb2, G= 1/8,**1/16**,1/32,1/64
- **3 discriminators**
  - 3 10 bit-DACs to set the thresholds (100fC, 1pC, 10pC)
  - Encoded in 2 bits
- **Auto-trigger down to 10fC up to10pC**
- Store all channels and BCID for every hit in a **127 bit deep digital memory**
  - Data format : 127 (depth)*[2bit*64ch+24bit(BCID)
  - +8bit(Header)] = 20 320 bits
- **872 SC registers**, default config
  - Mask of bad channels
- **1 mW/ch**

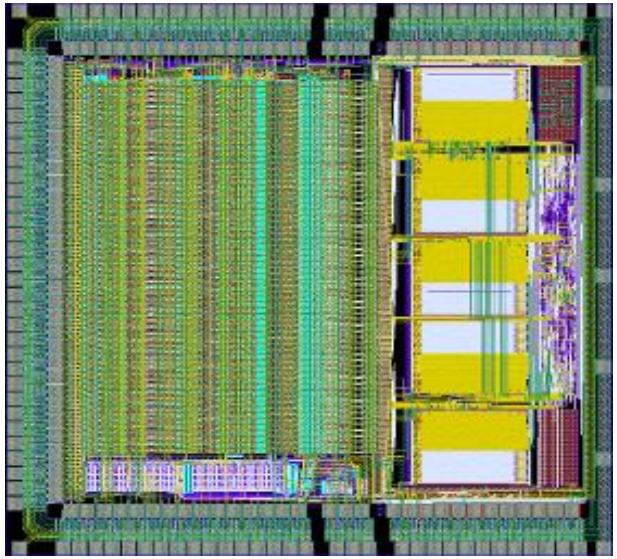


ASIC : HARDROC versions

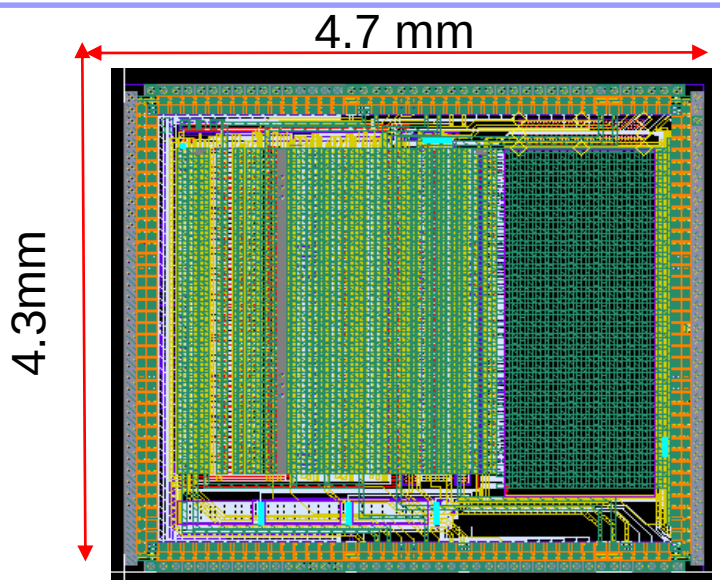
- **AMS 0.35µm SiGe**

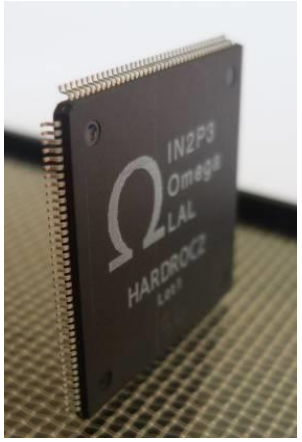
- **HARDROC1** (Sept 2006):
  - **1 FSB and 2 discriminators**
  - **240 staggered pads, QFP240 package 3.4 mm thickness**

- **HARDROC2 (June 2008) and 2B (June 2009):**
  - **Versions 2 and 2B very similar, 3 FSB, 3 discris**
  - **160 aligned pads, Thin package TQFP160 = 28 mm x 28 mm x 1.4 mm**



HARDROC1,
240 staggered pads



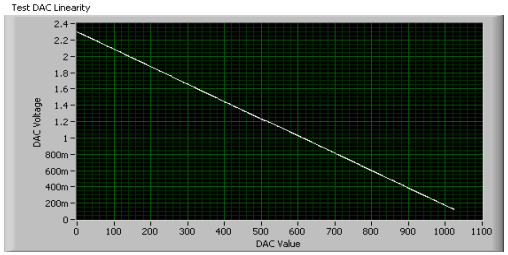


HARDROC2 and 2B
160 pads

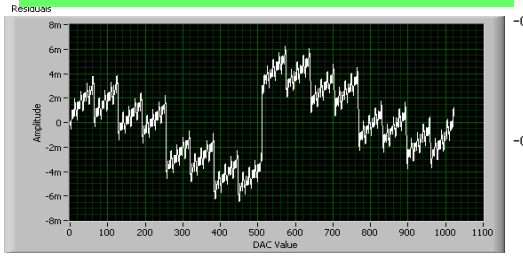
HR2 Trigger path : fast shaper, DAC, Xtk

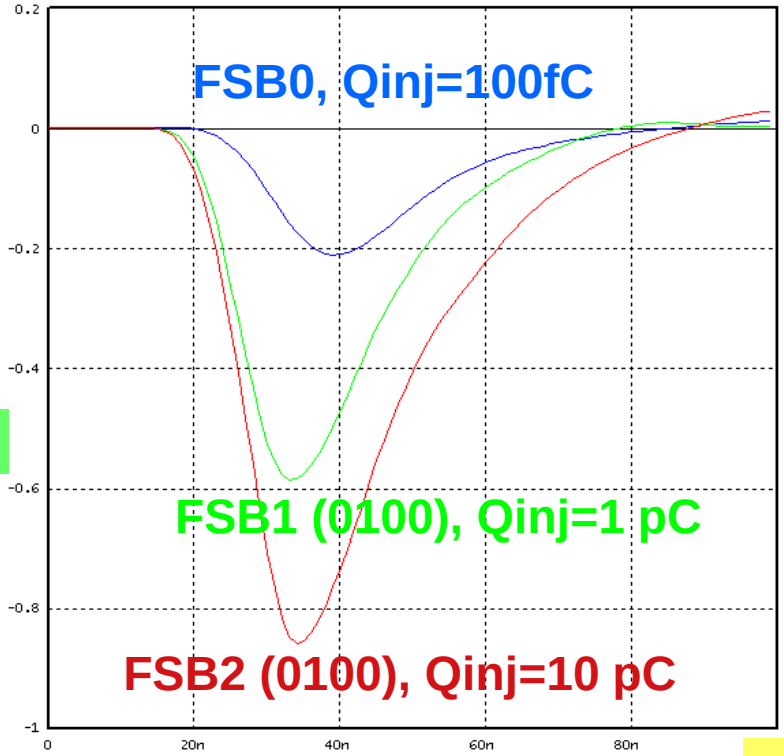
- Fsb0: **Typically 2mV/fC**
- 3 integrated DACs to deliver threshold voltages
  - Residuals within ±5 mV / 2.2V dynamic range. INL= 0.2% (2LSB)
- **2.1 mV/DAC Unit ie 1 fC/DAC Unit (fsb0)**

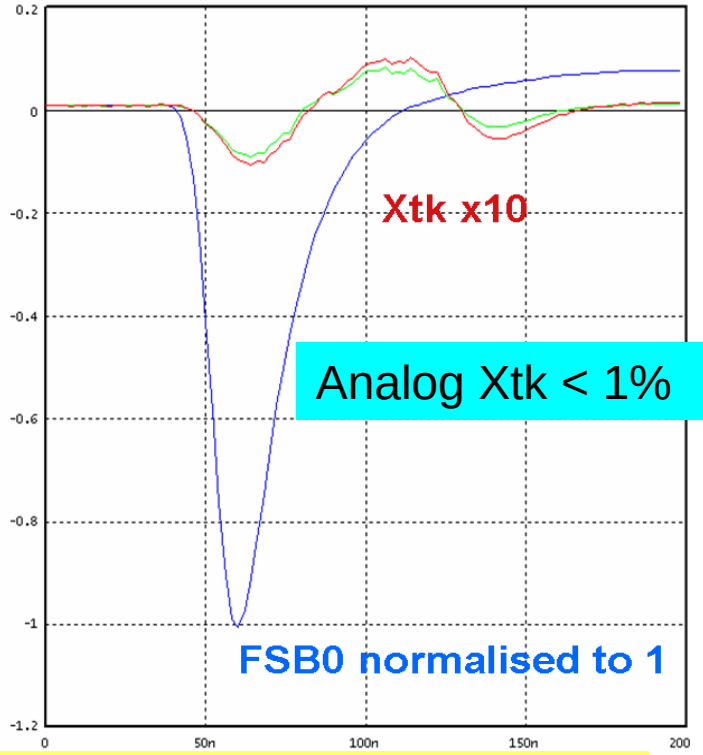
2.1mV/DAC Unit



Residuals within ±5 mV





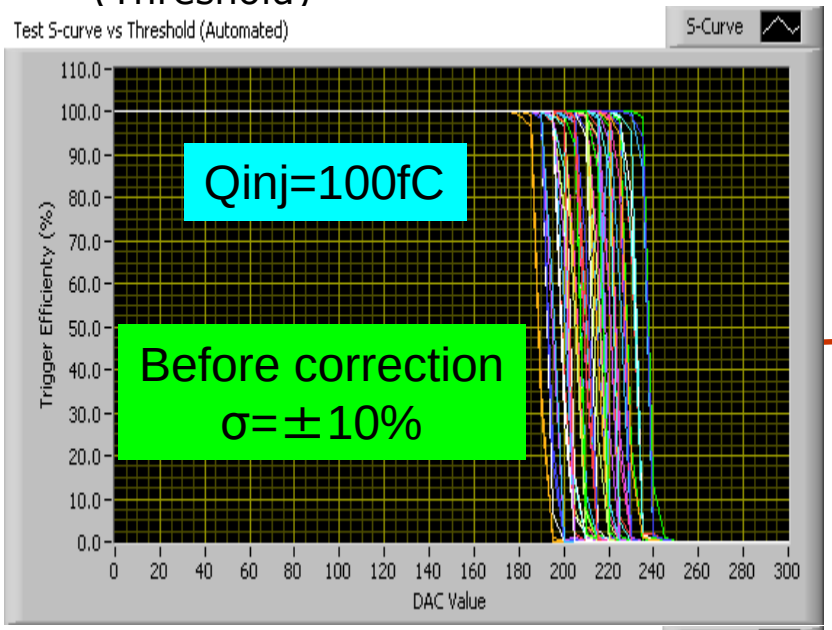


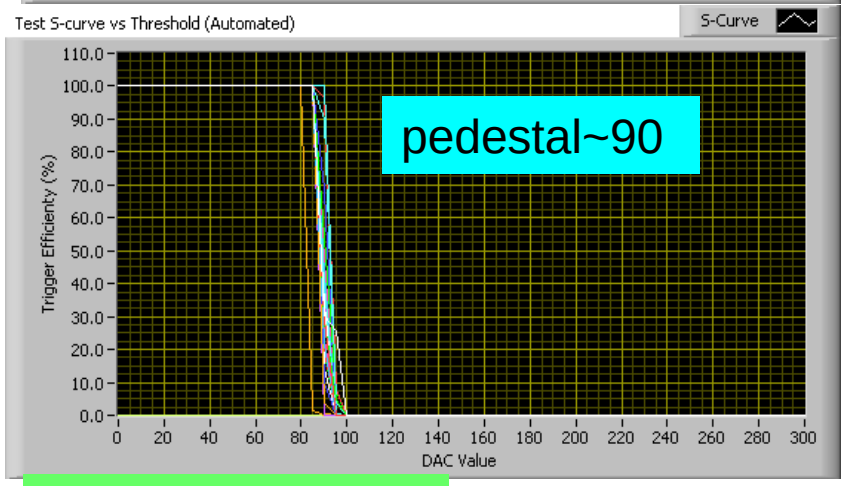
Analog Xtk < 1%

Testboard wo any decoupling cap.

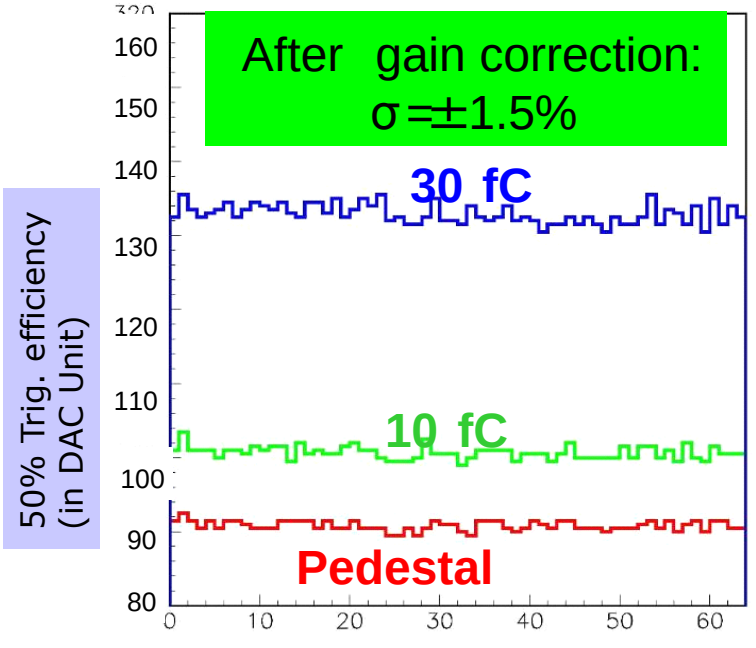
Trigger efficiency measurements

- Scurves performed on FSB0 by varying the DAC value (Threshold)





FSB0, 100K, 100fF, G=144



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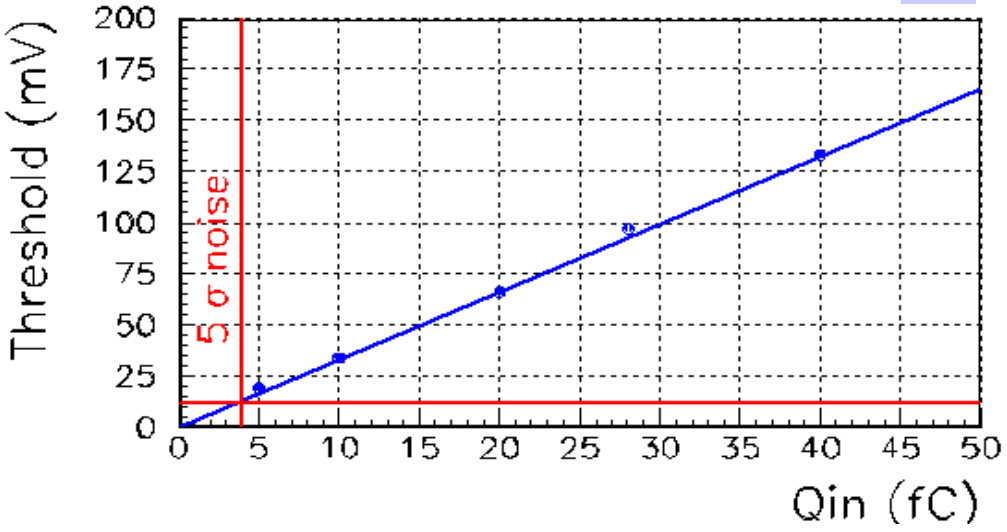
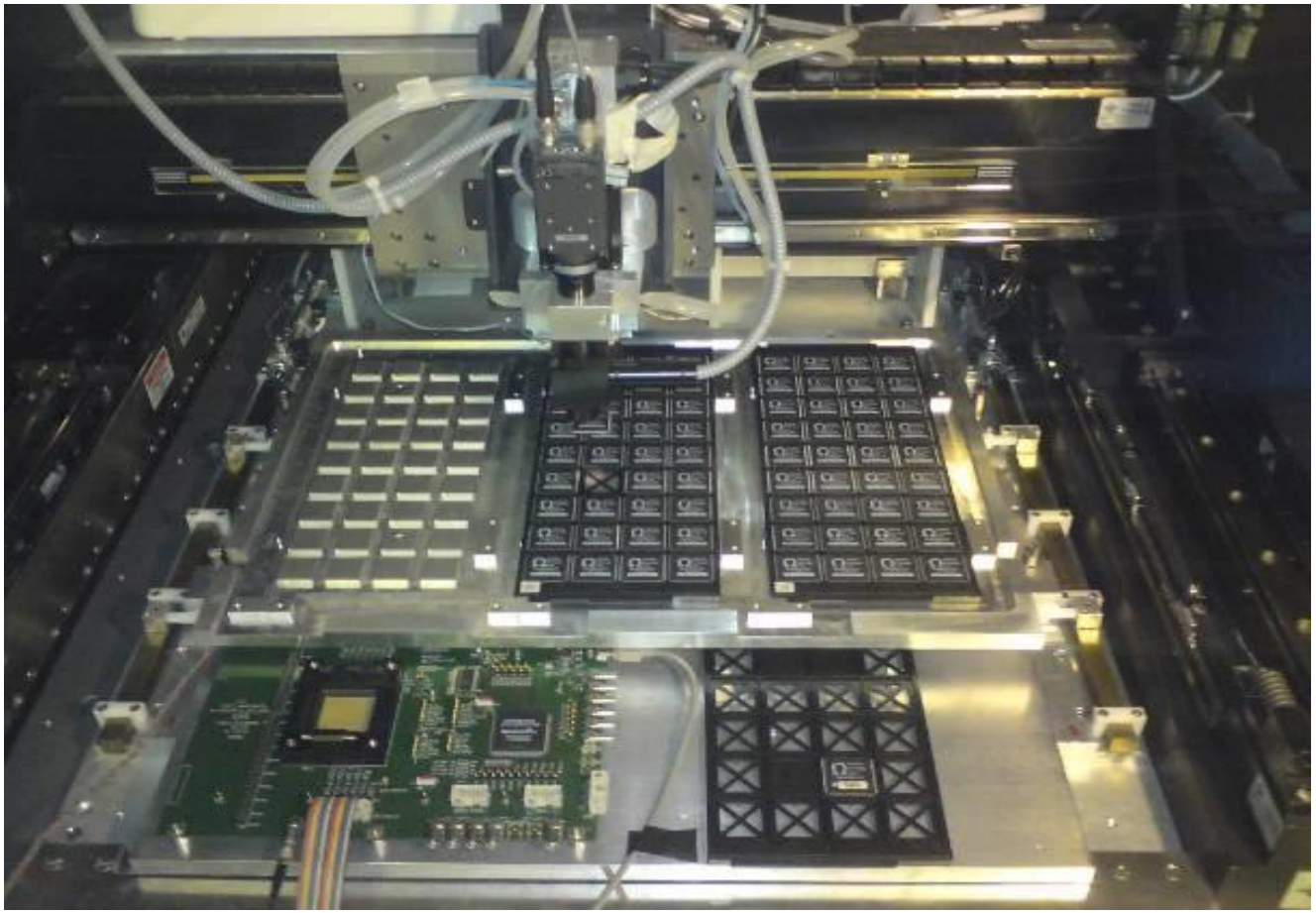


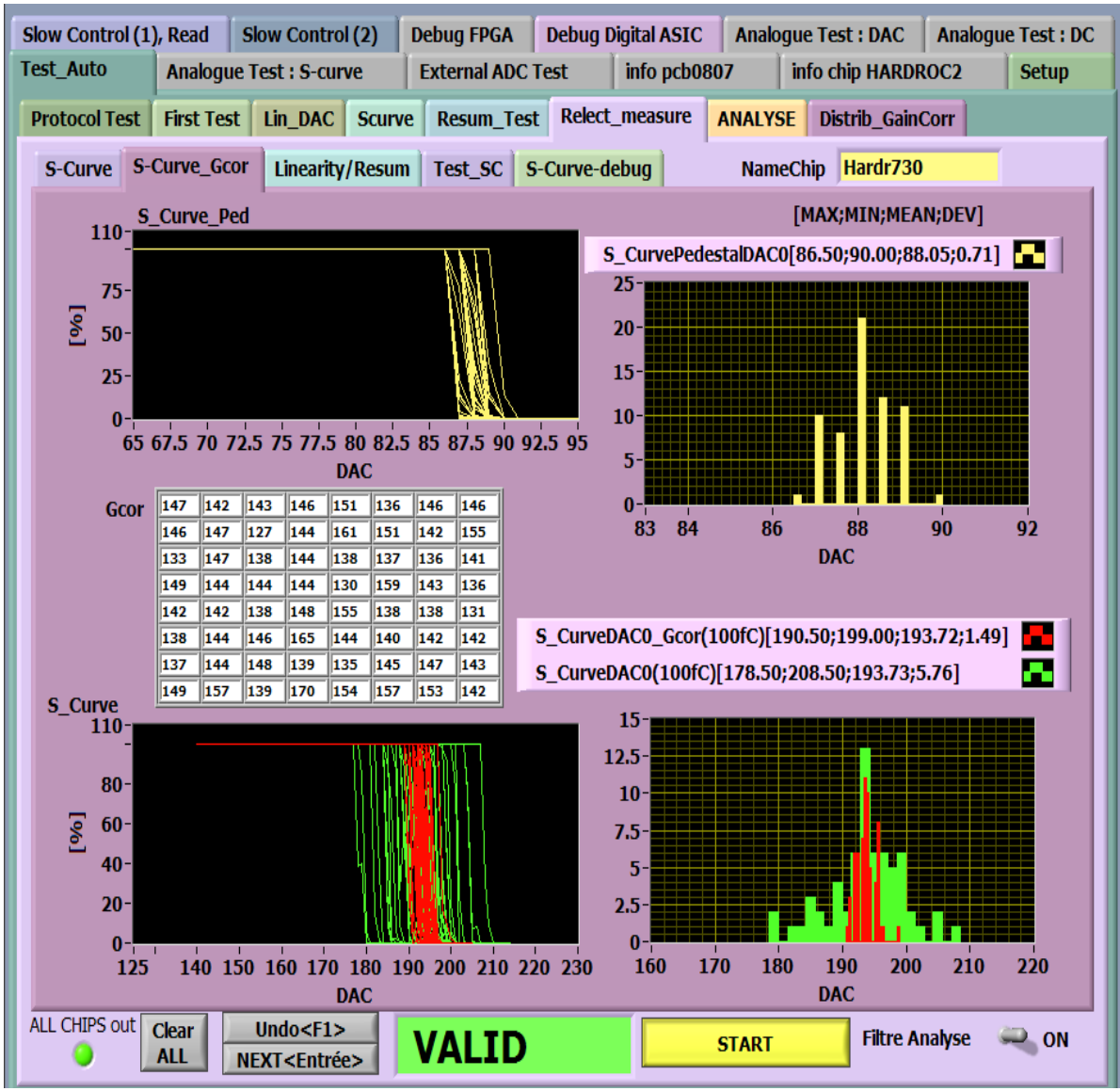
PRODUCTION TESTS

- ~10 000 chips were tested with a dedicated testbench in IPNL Lyon for the SDHCAL project.
- Dedicated Labview program, USB interface, testboard, programmable generator (GPIB), precise multimeter (Keithley)

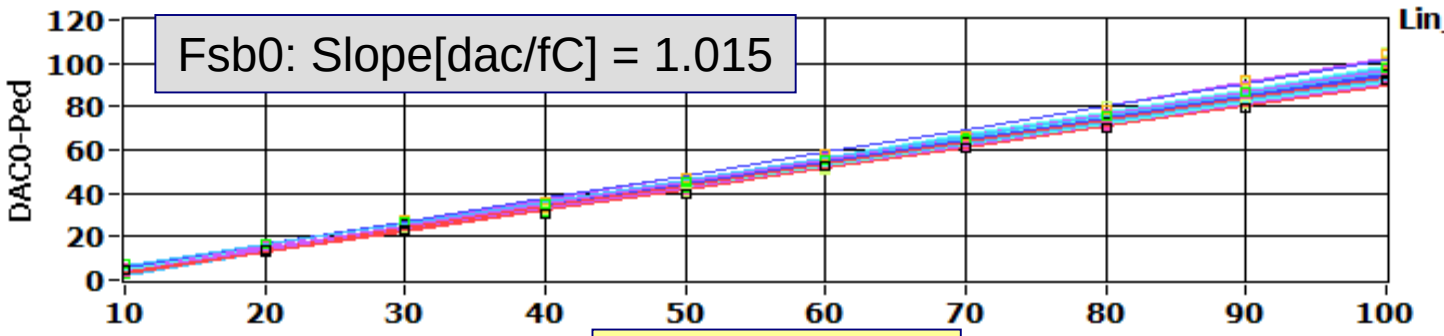


PRODUCTION TESTS

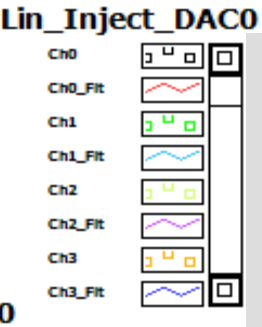
- Measurement of the DC levels and power consumption
- Test of the Slow Control loading
- Memory test
- DACs linearity
- Trigger efficiency measurement
  - Pedestal for the 3 shapers
  - 100 fC trigger efficiency measurement for fsb0 + gain correction for each channel
  - 1 pC trigger efficiency measurement for fsb1 and fsb2



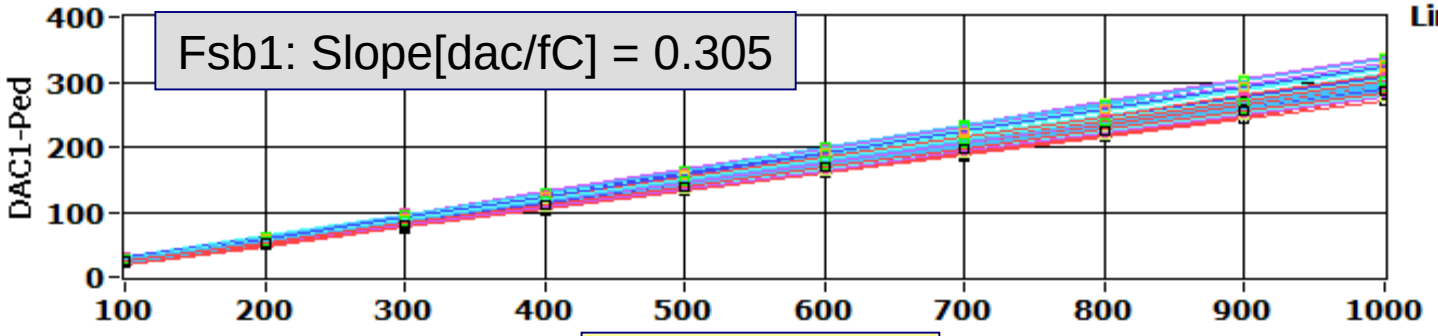
Fast Shaper Linearity: 64 channels



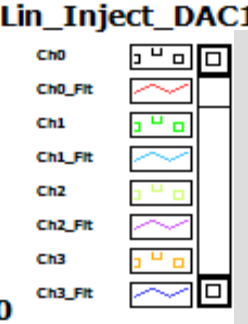
Inject [10fC-100fC]



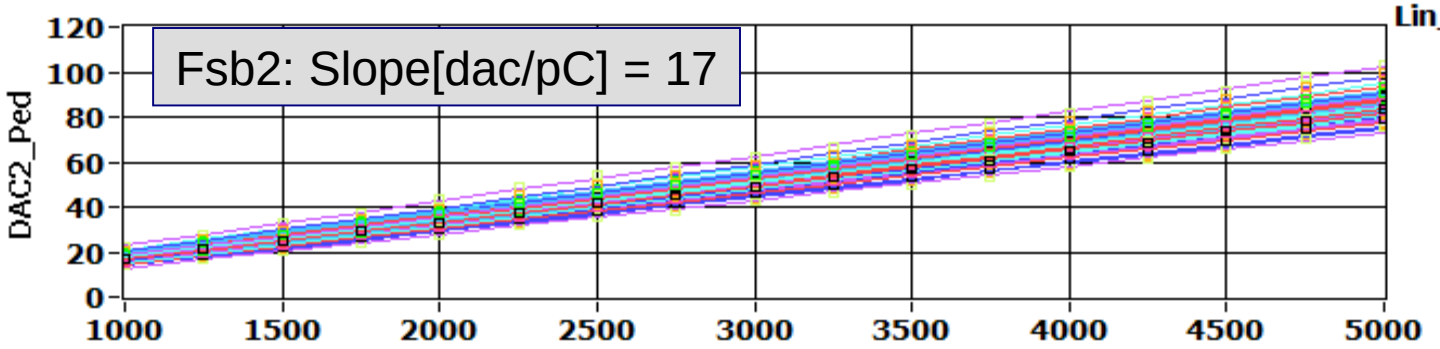
PARAM:
SS Gain : 1111
Sw_50k0:Off
Sw_100k0:On
Sw_100f0:On
Sw_50f0:Off
Measures 64 channels:
Dev : 0.022 [dac/fC]
Max: 1.082 [dac/fC]
Min : 0.961 [dac/fC]



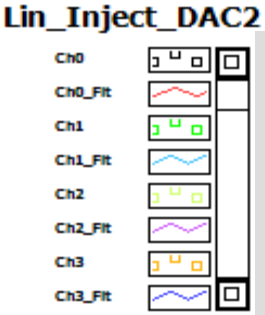
Inject [100fC-1pC]



PARAM:
FSB1 Gain : 1000
Sw_50k1:On
Sw_100k1:On
Sw_100f1:On
Sw_50f1:On
Measures 64 channels:
Dev : 0.016 [dac/fC]
Max: 0.346 [dac/fC]
Min : 0.277 [dac/fC]



Inject [1pC-5pC]



PARAM:
FSB2 Gain : 0010
Sw_50k1:On
Sw_100k1:On
Sw_100f1:On
Sw_50f1:On
Measures 64 channels:
Dev : 0.001 [dac/fC]
Max: 0.0198 [dac/fC]
Min : 0.0151 [dac/fC]

Electronics for Multi-gap CMS-GRPC

We conceived and produced a PCB to host : Pickup strips, 2 PETIROC, 2 TDC