The Detector Control System for the ATLAS Semiconductor Tracker Assembly Phase

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***Abstract*—The ATLAS Semiconductor tracker (SCT) consists of 4088 silicon microstrip modules, with a total of 6.3 million readout channels. These are arranged into 4 concentric barrel layers and 2 endcaps of 9 disks each. The coherent and safe operation of the SCT during commissioning and subsequent operation is an essential task of the Detector Control System (DCS). The main building blocks of the SCT DCS, the cooling system, the power supplies and the environmental system, are described. First results from DCS testing are presented.**

***Index Terms*—ATLAS Semiconductor tracker, detector control system, ELMB, PVSS, STC assembly.**

I. Introduction

A. The ATLAS Detector

The Large Hadron Collider (LHC) is a proton-proton (p-p) collider being constructed at CERN. Bunches of protons intersect at 4 points, with a separation of 25 ns and collision energy of 14 TeV. ATLAS, a general purpose collider detector, is placed in one of the two high luminosity regions (peak luminosity of $10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$) [1].

ATLAS consists of 3 main parts. Close to the beam axis, the tracking system employs pixel detectors, silicon microstrip modules and transition radiation straws, all located within a 2 Tesla superconducting solenoid. The tracker is surrounded by the calorimeter, the inner part of which is the electromagnetic calorimeter, using liquid argon as the sampling medium. The hadron calorimeter uses scintillation tiles in the barrel and liquid argon in the forward part as the sampling medium. In the outer part, muon trajectories are measured using 3 stations of muon chambers in a geometry defined by 8 superconducting toroid magnets.

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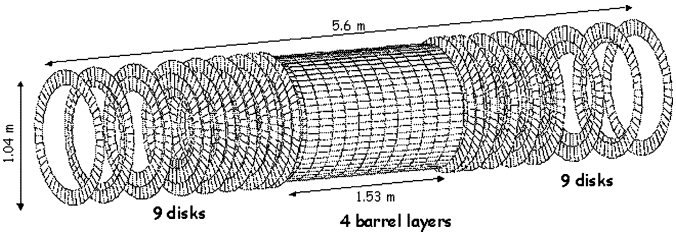

Fig. 1. The ATLAS Semiconductor Tracker, consisting of 4 co-axial barrel layers and 2 endcaps of 9 disks each.

B. The Semiconductor Tracker

The silicon microstrip modules are the building blocks of the ATLAS Semiconductor Tracker (SCT). The SCT consists of 4 co-axial barrels and 2 endcaps of 9 disks each (Fig. 1).

The modules are mounted on the barrels and endcaps. Most modules consist of 4 silicon sensors assembled in 2 daisy-chained pairs that are glued back-to-back with a small stereo angle (40 mrad) and bonded to the Front End (FE) electronics hybrid. Each module has 1536 readout channels. The binary readout architecture is a cost-effective implementation meeting the performance requirements [2]. Optical communication has been chosen to minimize the electrical pickup and to reduce the material. The modules are designed to operate at a temperature of $-7\ ^{\circ}\mathrm{C}$, implying the need for coolant temperatures of about $-25\ ^{\circ}\mathrm{C}$ and associated thermal enclosures. An extremely light evaporative cooling system (coolant C_3F_8) is used [3].

II. SCT Detector Control System (DCS)

A. Scope of the ATLAS DCS

Each of the 4088 SCT modules ($\approx 60\ \mathrm{m}^2$ silicon surface) requires several power lines for the electronics hybrid and silicon sensors, plus 3 fibers for the optical readout. Each of the electrical lines is individually controlled and monitored. The reliable operation of the cooling system is mandatory for the stable detector operation. A total number of almost one thousand sensors, placed at various points through the SCT, provide information on the humidity, temperature and pressure. The large number of parameters to be monitored and controlled demands a robust and secure Detector Control System (DCS) to ensure electrical operation of the modules as well as reliability under the extreme environmental conditions.

The ATLAS DCS supervises the full slow control of the experiment and provides hardware and software tools for monitoring, interlocks and controls. It provides communication between all the subdetectors and interaction between ATLAS and the LHC accelerator, as well as other external services such as cooling, ventilation and safety systems.

The overall control of ATLAS includes the monitoring and control of the detector hardware and the related infrastructure, as well as the supervision of the software involved in the event readout, this latter task being provided by the Data Acquisition (DAQ) system. The two systems (DCS and DAQ) are independent but their interaction is essential; the DCS is a vital component for the reliable and safe operation of the detector, and for the data taking [4].

B. The LHC and ATLAS DCS Organization

All ATLAS detectors use a common DCS architecture and share the same utilities to develop their DCS systems. A Joint Controls Project (JCOP) [5] at CERN addresses common points of control. It is within this framework that the SCT DCS has been developed.

The DCS consists of a distributed Back-End (BE) system running on PCs and Front-End (FE) systems ranging from simple elements like temperature sensors to complex controllers.

For the LHC needs, the BE is implemented with PVSS II [6], a commercial Supervisory Control and Data Acquisition system (SCADA). It is a powerful and flexible package that provides easy communication between the PC and the hardware, allowing the developer to create a Graphical User Interface for the monitoring and control of the latter. The building blocks of each PVSS project are *datapoints*, each of which corresponds to a hardware unit or to a monitored parameter. Datapoints are the upper level of a tree structure and can be built into functional objects. This type of structure makes the project development flexible, comprehensive and maintainable.

The organization of the DCS is hierarchical and simulates the hardware structure of the experiment. DCS consists of independent partitions that can be operated in standalone or integrated mode. The Finite State Machine (FSM), a tool written in SMI++ and developed under the JCOP framework, handles the states and transitions of the different partitions, by means of commands and messages [7].

The essential FE component used for the ATLAS DCS is the ELMB (Embedded Local Monitor Board), developed for standard analog and digital I/O (Fig. 2). It is radiation hard, has low power consumption and can either be embedded into a custom motherboard or used in standalone mode [8].

The ELMB communicates with the BE system via the CAN (Controller Area Network) field bus [9], using a high level protocol, CANopen. The CAN interface [10] card that has been chosen (Kvaser card), gives the possibility to have 4 different CAN buses connected and readout simultaneously by one PC-slot. An OPC (Object linking and embedding for Process Control) server [11], developed at CERN, provides the configuration software to allow easy monitoring of the ELMB.

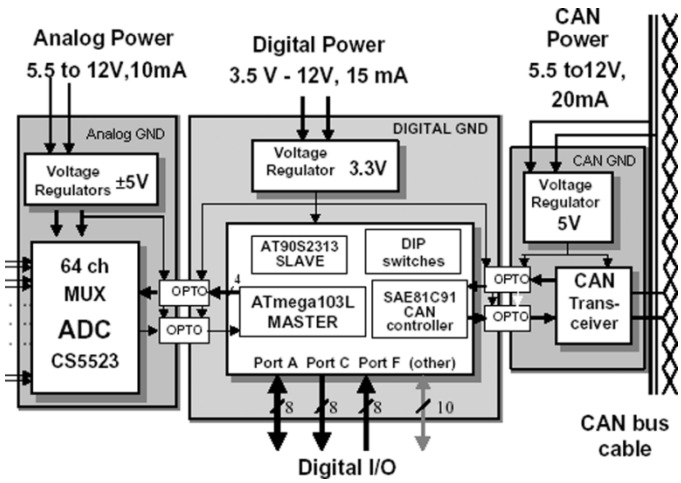

Fig. 2. Simplified diagram of the ELMB. It has digital and analogue channels for input and output. The main purpose of the ELMB is the conversion of the analogue information from the connected sensors into digital information that is provided to the DCS via CANbus.

C. SCT DCS Hardware Description

The SCT hardware is naturally divided in groups depending on its function, namely the cooling system, the environmental system and the power supplies [12].

1) The Cooling System: The radiation-induced leakage current and doping changes affecting the depletion voltage of the silicon modules depend on the operating temperature of the SCT modules. The operating temperature of the SCT varies from $+15$ °C, while startup and commissioning, to -7 °C, during operation in the ATLAS pit. Thermal stability of better than 2 °C and a tolerance to thermal shocks are two issues that have to be ensured for all the operations [13].

An evaporative fluorcarbon cooling system has been chosen for both the SCT and the pixel detector. The coolant is C_3F_8, a nonflammable, nonconductive and radiation resistant liquid. The temperature can be tuned by a change in the operating pressure.

The control of the cooling processes (starting up, operation and shutting down) and the monitoring of the main cooling parameters (pressure and concentration of the cooling fluid) are performed by a Programmable Logical Controller (PLC). DCS has monitoring functions.

2) The Power Supplies (PS): The silicon modules mounted on the SCT detector are powered by the High Voltage (HV) and Low Voltage (LV) power supplies (Fig. 3).

Each LV card [14] controls 4 electrically independent LV channels. It outputs logical signals for the FE electronics of the modules (RESET and clock SELECT) and 4 different voltages: the analog (Vcc) and digital (Vdd) voltages for the readout chips as well as VCSEL and PIN bias voltages for the optical communication of the module. Two thermistors mounted on each barrel module and one thermistor mounted on each endcap module are read out through the LV cards. Each HV card controls 8 electrically independent HV channels, providing bias voltage to the detector modules [15]. Typical values for the most important parameters supplied via the LV and HV cards are shown in Table I.

The control and monitoring of the LV and HV cards relies on the Crate Controller (CC), the ELMB based interface between

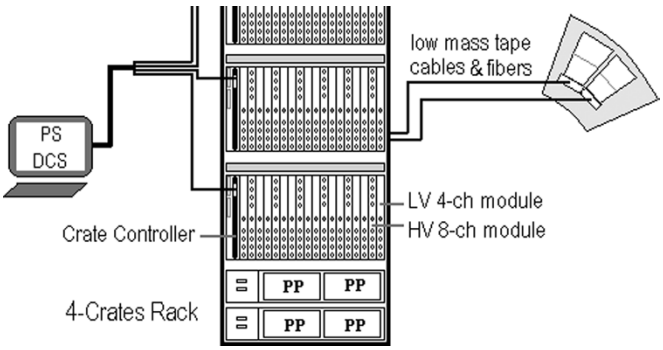

Fig. 3. Layout of one power supply rack. Two of the four crates in a rack can be seen in the drawing.

TABLE I
TYPICAL VALUES FOR PS PARAMETERS

Parameter	Voltage (Volts)	Current
HV	150 (max 500)	300nA (max 5mA)
Analogue LV	3.5 (max 10)	900mA (max 1300mA)
Digital LV	4 (max 10)	570mA (max 1300mA)
VCSEL	1.6 - 6.6 (max 9.6)	4mA (max 10mA)
PIN	5 - 10 (max 13)	0.5mA (max 2.5mA)

the PS modules and the higher levels of the DCS system. The ELMB used in the CC is custom programmed.

Four Power Packs (PP) are placed in each rack providing redundant powering to four PS crates.

3) The SCT Environmental System: The detector environmental system deals with the monitoring of the environmental sensors placed on the barrels and endcaps of the SCT. These are temperature and humidity sensors located at appropriate positions to provide information about the following parameters:

1. the temperature close to the outlets of the cooling pipes (Fig. 4);
2. the temperature near the edge of the barrels, to give information about possible deformations in the shape of the support structures;
3. the air temperature inside the detector;
4. the humidity inside the detector.

Negative Temperature Coefficient (NTC) thermistors are used for the temperature monitoring. Radiation hard Xeritron sensors are used for the humidity monitoring [16].

To separate the cold SCT volume from the transition radiation straws detector operating at room temperature, the SCT will be surrounded by a thermal enclosure and maintained in a dry, cold nitrogen atmosphere. For the assembly phase, a temporary thermal enclosure dedicated to single barrel acceptance tests has been built, allowing the barrel to be placed in a dry environment and under controlled environmental conditions. Humidity, differential pressure and temperature sensors are installed. A flow meter measures the dry airflow into the enclosure.

All the environmental sensors are connected to ELMBs and monitored by software. For the temperature sensors on the cooling pipes, there is an additional hardware interlock. The ELMBs used for the monitoring of these sensors are not embedded in the standard motherboard but in motherboard cards mounted in the Building Block Interlock Monitoring (BBIM) crates, where the Interlock Boxes (IBOXs) are also mounted [17]. Each sensor is connected in parallel to the ELMB and the IBOX. The IBOX, designed within the ATLAS pixel collaboration, is a board that allows setting a threshold to the input voltage and acts as a discriminator resulting two logic states at the output of the IBOX. Therefore, if the cooling temperature exceeds a predefined value, the output of the IBOX triggers the Interlock Matrix (IMatrix) [18]. The IMatrix provides the hardware mapping between the temperature sensors in a cooling stave and the corresponding to the modules mounted in this stave, PS cards. The mapping is implemented in a Complex Programmable Logic Device (IspMACH5000VG, LC5768VG from Lattice Semiconductor), programmed with VHDL to switch off the affected power supplies in case of high temperature trigger. A System Interlock Card (SIC), mounted in each crate, distributes the signals from the interlocks to the LV and HV cards via the backplane. A diagram of the monitoring and interlock chain of the temperature sensors on the cooling pipes is shown in Fig. 5.

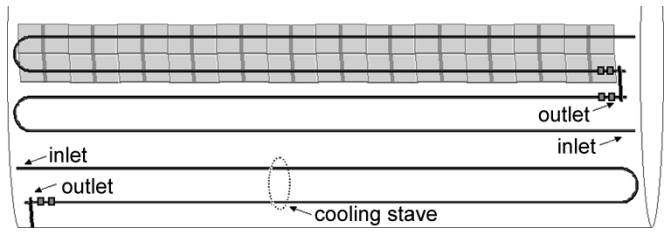

Fig. 4. Schematic diagram of a cooling loop. The inlet and outlet of each cooling stave (half cooling loop) are shown. On each cooling stave, 24 modules are mounted. For redundancy, two temperature sensors are placed near each cooling outlet.

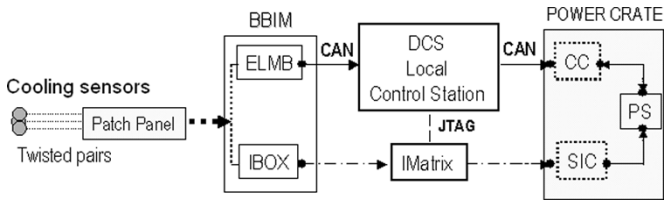

Fig. 5. Environmental cooling DCS overview. Each cooling sensor is software (ELMB) and hardware (IBOX) interlocked.

D. SCT DCS Software Description

All the hardware connected to the SCT detector is under DCS supervision. The different groups of this hardware define the DCS software building blocks. Three main projects have been developed: the Cooling, the Environmental and the Power Supply Projects.

1) DCS BE Structure: The SCT DCS BE system is a part of the ATLAS distributed BE system. The structure is hierarchical, with the Atlas Global Control Station (GCS) at its head, controlling the whole experiment. The Subdetector Control Stations (SCS) coordinate the subdetectors. The base of the hierarchy consists of the subsystems for each subdetector, called Local Control Stations (LCS). The SCT LCSs are the environmental system and the power supply system. The cooling system is common to both SCT and Pixels and belongs to the Inner Detector SCS. The LCSs are the part of the system that the user

can interact with, sending commands and viewing its status at the lowest possible level.

2) The SCT DCS Projects: Physically, the LCSs correspond to the PCs where the monitoring and control projects are installed. The projects are distributed, giving the possibility of exchanging datapoints, and therefore information. The large number of parameters to be monitored or controlled demands the use of databases presently in text file format where all the information about the systems is stored and from which changes are loaded. PVSS archiving tools are used for storing the running conditions. In the future, the ATLAS conditions database, based on Oracle [19], will be used for that purpose.

a) Cooling DCS: Monitoring of the operations of the cooling circuit is provided. Warnings and alarms are communicated to the PS project. This DCS project is common for Pixels and SCT and provides only monitoring.

b) Power supply DCS: Through the crate controller, about 1500 parameters are read out for each crate, and all these parameters have to be monitored and controlled by the PS DCS project. The GUI developed for that project can be used for actions on the crates (i.e., SWITCH ON/OFF) and for monitoring of the LV and HV parameters of the SCT modules, such as input voltage, current and hybrid temperature. Warnings and alarms are implemented. If a warning or alarm occurs in any of the other DCS subsystems, safety actions are taken by the PS, such as ramping down the voltage of the modules. Some more functionality (module current readouts, masking on or off crate modules) has been added where needed.

The Power Supplies can be in 3 basic states: On, Off and Standby. The database of the project is very large and gives information about the safe, warning and alarm ranges of each state and parameter. The PS DCS and the DAQ share the database.

The communication between the two systems (DAQ and DCS) is achieved by the DDC (DAQ and DCS Communication) project. It provides bi-directional exchange of data between the two systems, such as states and parameters, transmission of DCS alarms to the DAQ and the ability for the DAQ to issue commands to the DCS [20].

c) Environmental DCS: The environmental DCS project handles all the environmental sensors in the detector itself and in the thermal enclosure.

The dew point temperature is calculated using the air temperature and the humidity values. Alarms are created and propagated to the PS project if the monitored parameters are outside the safe range. The detector environmental project uses a configuration file that provides the mapping of the physical position of the sensors on the detector to the ELMB channels. The mapping of the cooling sensors is also used by the Cooling DCS project.

A summary of the DCS BE structure with all the DCS software components is presented in Fig. 6.

d) Finite State Machine (FSM): The FSM is interconnecting and supervising all DCS projects. One FSM branch is installed and running in each PVSS project, all of them being accessed, supervised and summarized, in the present implementation, by the PS FSM.

The state of each project gives information about the current running condition of the project. A project can be in three different states: READY, NOT READY and ERROR, with bi-directional transitions between them, apart from the transition READY to ERROR. If a project is in the state READY, it can provide reliable information about the status of the system, which can be OK, ALARM, WARNING and NOT PHYSICAL. The states and status are summarized in the FSMof each project and propagated to the upper levels of the DCS hierarchy.

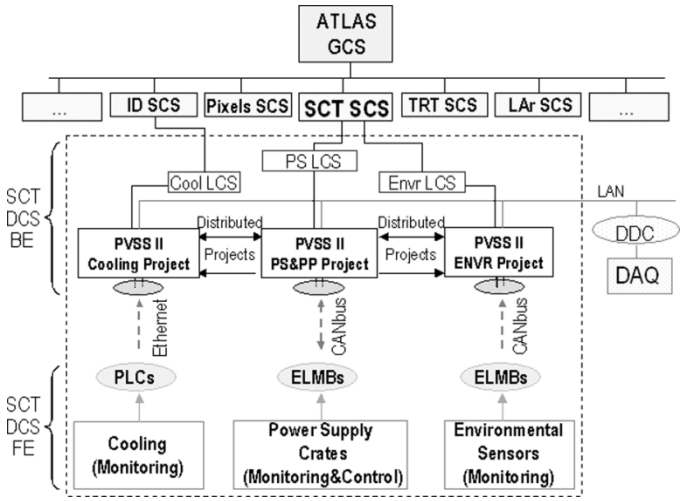

Fig. 6. SCT DCS structure (framed area)—BE hierarchical levels and principal FE units. The SCT supervisor is the PS project, in the present implementation.

TABLE II
ALARM DEFINITIONS AND CORRESPONDING ACTIONS

Case of	Action
$T_{cool}<T_{Dewpoint}+10^{\circ}C$	Flush dry air
$T_{cool}<T_{Dewpoint}+5^{\circ}C$	Switch off LV/HV
$T_{air}>30^{\circ}C$	Switch off LV/HV
$T_{mech}<-10^{\circ}C \| T_{mech}>30^{\circ}C$	Switch off LV/HV
$I_{bias}>I_{alarm}$	Switch off HV
$T_{module}>T_{alarm}$	Switch off LV/HV
Off state HV>20V	Switch off HV
Off state LV output ON	Switch off LV
CC/HV/LV communication loss	Reset Communication
Any Fatal from Cooling and CIC	Switch off LV/HV, prevent from ramping on
Communication loss between projects	Pop up messages, operator to reestablish communication. Interlock to ensure safety

The safety and reliability requirements during operation, as well as the experience obtained during the system tests and the module assembly, determined the definition of the DCS alarms as well as the corresponding actions to be taken in such cases. Table II summarizes the alarm definitions and the corresponding actions.

III. DCS TESTS DURING THE SCT ASSEMBLY

The implementation of the described DCS system for the SCT assembly phase has already been completed. The SCT assembly is underway, therefore the DCS functionalities are currently being tested and used at several SCT assembly sites.

The performance of the DCS system has been checked for the PS project. In the case of a problem, such as an increase in hybrid temperatures indicative of a problem with the cooling system, it is desired to ramp down the power within $\sim$10 seconds. The CC will take at most 6 seconds after each readout to

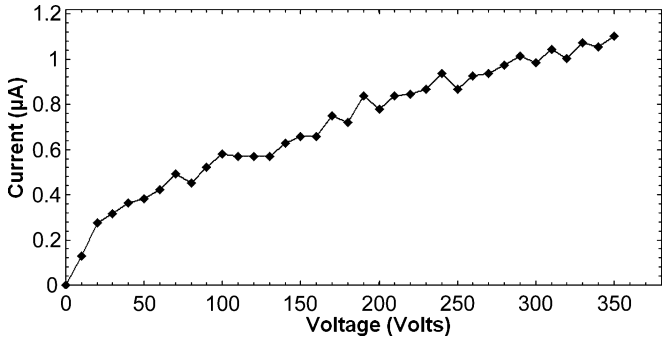

Fig. 7. IV curves of one module used in the ATLAS SCT test beam, with data taken by the PS project. The intrinsic precision in the HV cards for the current readout is 50 nA corresponding to 5 ADC counts.

initiate a controlled shutdown of a problematic channel, hence the time interval between two successive readouts is set to 4 seconds such that shutdown takes place within the allowed time.

In each readout about 1500 messages are transported through the CANbus and is has been measured that these messages are separated in the CANbus by a time interval of 0.9 ms. According to the ATLAS DCS requirements, the maximum CANbus occupancy during operation should not be larger than 60%, to prevent situations of overloaded CANbus in cases of emergency. Therefore, a maximum of 11 crates on each CANbus is allowed, when reading out every 4 seconds. Ethernet communication is used between the different DCS projects. Therefore, the alarm messages sent to the PS project by the other projects are received immediately.

1) SCT DCS in the ATLAS Combined Test Beam: A DCS chain including Environmental and Power Supply systems has been set up for the ATLAS SCT test beam. Two temperature sensors on the cooling pipe, two air temperature and two humidity sensors have been monitored successfully by a simplified environmental project. Eight silicon modules were powered by a crate that was controlled and monitored by the PS project. The dependence of the leakage current as a function of the bias voltage (IV curve) for one silicon module using data from the PS project is shown in Fig. 7.

2) DCS Tests During Barrel Assembly: At the SCT assembly sites, acceptance tests with working DAQ and DCS systems are being performed. At Oxford University, the assembly of the innermost barrel layer has been completed. All DCS functionalities, as well as the DDC, have been tested and verified to work satisfying the safety requirements. DCS data have been stored using both the PVSS and the DAQ archiving tools, propagated through the DDC. Fig. 8 shows the distribution of the module temperature along a cooling stave, for a "cold" run (coolant temperature ~ -2 °C) and a "warm" run (coolant temperature $\sim$ 15 °C). The temperatures of the 24 modules are stable along a cooling stave.

3) DCS Tests During the Integration Phase: The final SCT assembly site is at CERN, where a dedicated facility for the Inner Detector assembly and integration has been prepared. Acceptance tests will initially be performed on each barrel. Module cooling, power supplies and readout (analog and digital) will be checked. The goal of these tests is to verify that each barrel functions properly after transportation and before final four-

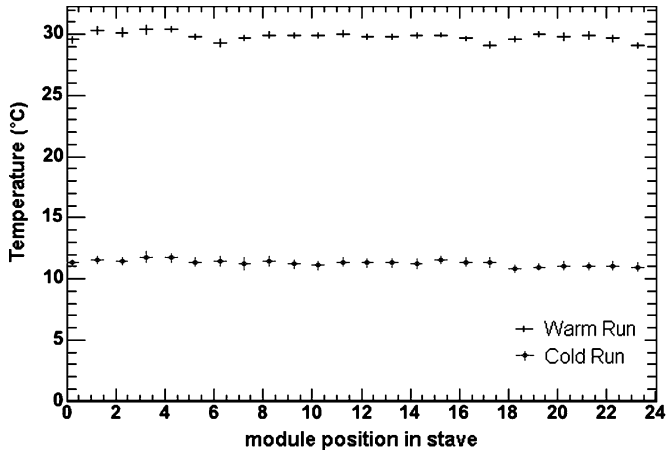

Fig. 8. Temperature profile along a cooling stave. For the warm run, the mean temperature is 30.1 °C, (RMS variation 1.0 °C) and for the cold run the mean temperature is 11.6 °C (RMS variation 1.5 °C).

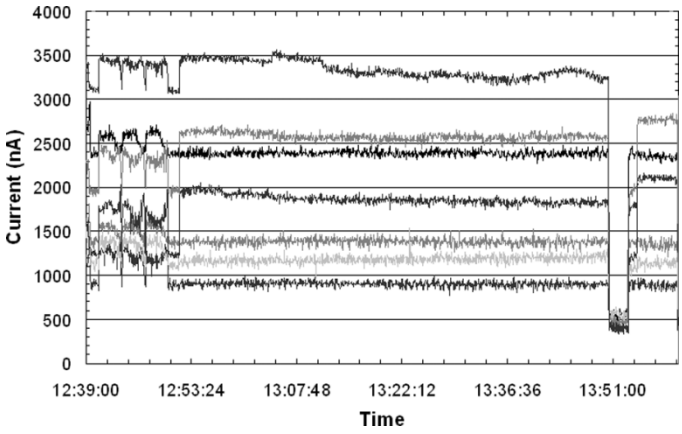

Fig. 9. Current readouts for 7 modules during a run of the barrel sector. The monitoring of the currents is stable. Current fluctuations are recorded according to the operations performed by the DAQ.

barrel assembly. For these tests, approximately 700 cables and 2400 fibers have been tested and installed inside the temporary thermal enclosure.[1]

A barrel sector with 15 modules has been tested at CERN. The stability of all the DCS projects could be verified, using a full DCS chain running continuously for several days. The PS DCS is successfully ramping on and off the power supplies and provides stable monitoring of the module currents (Fig. 9). The evaporative cooling is functioning correctly. In Fig. 10, the thermal enclosure temperatures as well as the temperatures in the outlet of the cooling stave are shown for one run of the barrel. The cooling procedure is shown: the temperature falls from ~ 24 °C to ~ 12 °C, and even after the modules are powered, the temperature remains practically stable; at the end of the run the temperature of the cooling pipes rises again to the room temperature.

A successful monitoring of the main PS DCS parameters is also provided by the DAQ GUI, through the DDC. Summary panels show the module temperatures, as well as the analogue and digital voltages and currents.

[1]Two ATLAS internal notes summarize the cable and fiber tests and results: ATL-IC-TP-0001 and ATL-IC-TP-0004.

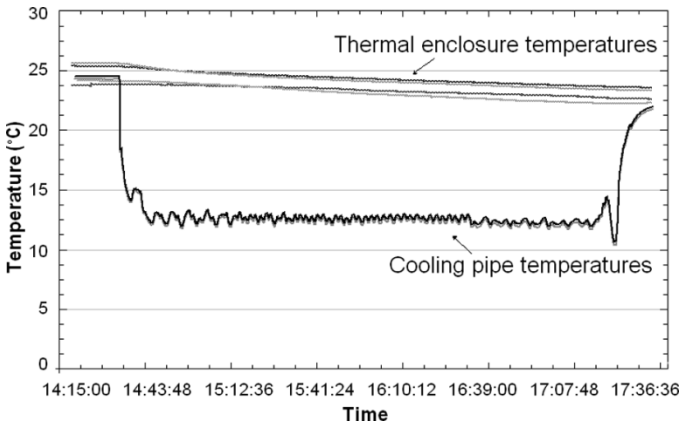

Fig. 10. Temperature readout during a barrel sector run. Temporal evolution of the temperatures on cooling pipes and thermal enclosure temperatures are shown.

TABLE III
NUMBER OF ENVIRONMENTAL SENSORS IN THE BARRELS

SCT Component	Cooling Temp	Mechanical Temp	Air Temp	Humidity	Total Number
Barrel 3	36	9	32	3	80
Barrel 4	46	9	32	4	91
Barrel 5	52	9	32	4	101
Barrel 6	60	9	32	4	111
Total Barrel	192	36	128	15	371

In the CERN assembly facility, for single barrel acceptance tests up to 15 PS crates will be used simultaneously, while for full barrel tests, 44 crates will be fully occupied. The number of barrel environmental sensors to be monitored is shown in Table III. A similar number of sensors will be installed in the endcaps.

The system will become even more demanding once the endcap disks will be integrated. The stability of the DCS performance is therefore essential.

IV. CONCLUSION

The complexity and fragility of the SCT detector and its infrastructure demand an extremely stable DCS that will ensure the safe operation of the silicon modules. The software and hardware components of the SCT DCS building blocks (the power supplies, the cooling and the environmental systems) for the SCT commissioning phase are prepared and have been extensively tested. The DCS satisfies the required performance and the safety specifications.

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