Advanced Front End Signal Processing Electronics for ATLAS CSC System: Status And Post Production Performance.

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Abstract

The ATLAS muon spectrometer will employ Cathode Strip Chambers (CSC) to measure high momentum muons in the extreme forward regions. Preamplification of the charge on the strips is performed in the Amplifier Shaper Module I. Amplifier Shaper Module II performs the analog buffering, digitization of the charge signals from individual cathode strips and multiplexes the data into two fibre optics links at 1 Gbps each. We present the design architecture of the complete front end electronics chain and its performance. We also report on the production and testing status of overall on detector electronics.

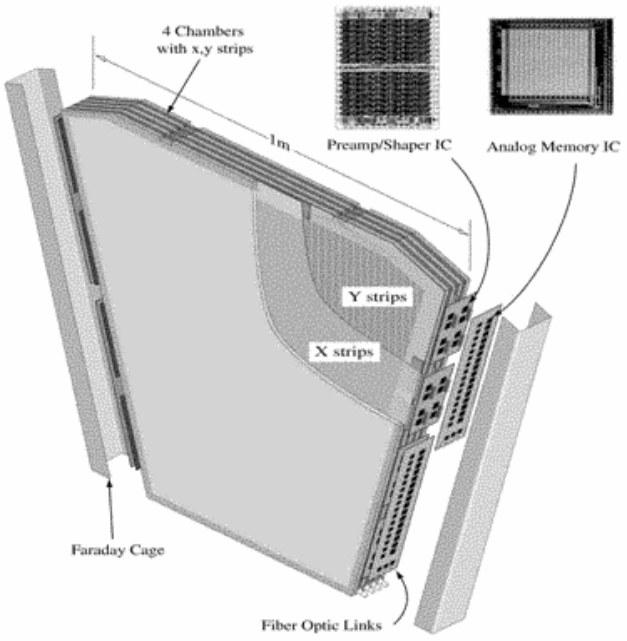

Figure 1: Cathode Strip Chamber with Electronics

I. Introduction

Cathode Strip Chambers (CSC) form the first station of the endcap muon spectrometer in the ATLAS experiment. The CSC system consists of 32 four-layer readout planes of 192 x- and four-layer readout planes of 48 y-strips each. Each CSC is served by 5 front end electronics packs called Amplifier Shaper Module Packs (ASM-Pack), which consist of two ASM-I and one ASM-II printed circuit boards (PCB). ASM-Pack together employs 4 different custom designed Application Specific Integrated Circuits (ASIC) fabricated using Agilent Technology (AT) 0.5µm CMOS, Single Poly, Linear Capacitor, Triple metal process, along with a switched-capacitor array analog memory in a radiation-hardened 0.8µm CMOS process and various COTS components. Both PCBs use radiation hard electronic circuits consistent with the ATLAS radiation policies.

Figure 10: summarizes signal flow on CSCs. Charge induced on the cathode strips by the ionized gas is amplified by the ASM-I. The ASM-II assembly stores analog samples from the output of the ASM-I, digitizes the samples to 12-bits then multiplexes and serializes the Analog to Digital Converter (ADC) data to two gigabit optical links which transmit these data to the off-detector electronics. Control to the sampling and digitizing circuitry is provided via fiber optic link from the off chamber electronics.

II. Spatial Resolution And Electronic Noise Charge

In a CSC the precision coordinate is obtained by a relative measurement of charges induced by the avalanche on adjacent cathode strips. The primary factor limiting the CSC spatial resolution is the electronic noise of the preamplifier. The precision in the determination of the centre of gravity of the induced charge depends linearly on the signal-to-noise ratio. A design consideration of the readout amplifier is an electronic noise level such that the chamber can be operated with a total anode charge of about 1pC per minimum ionizing particle at the target spatial resolution.

Uncertainty in determination of the precision coordinate $\sigma_{c.g}$ given an r.m.s error of σ (Electronic Noise Charge) in the charge measurement can be calculated by the following expression [1]:

$$\sigma_{c.g} = \frac{\sigma}{Q}\sqrt{2\sum_i X_i^2} \qquad (1)$$

Where Q is total charge induced on cathode plane. Monte Carlo simulation show that optimum number of strips lay between three and five.

$$\sigma_{c.g} = \frac{5.2\sigma W}{Q} \le 60\mu m \qquad (2)$$

Using maximum total induced charge of 200fC and strip pitch W=5.08mm give a required noise limit of

$$\sigma \le 0.53\, fC = 3200e^{-} \qquad (3)$$

Quantization noise as a function of full scale charge and input referred noise can be calculated as:

$$\frac{Q_{F.S}}{2^{NBits}.\sqrt{12}} << \sigma \therefore NBits >> 7.7 \quad (4)$$

To minimize the quantization noise of the ADC such that the predominant noise source is the preamp/shaper, an Analog Devices AD9042 12-bit ADC has been selected.

III. ASM-I

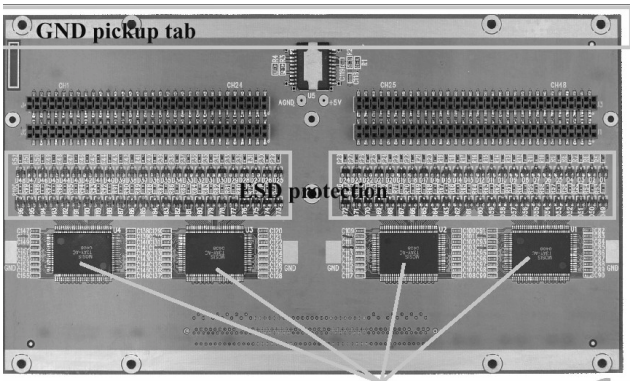

Figure 2: Preamplifier Shaper ASICs on ASM-I

Technology	0.5 µm CMOS
Channels	25
Die size	3.29 x 5.79 mm
Architecture	Single-ended
Intended Cdet	20 – 100 pF
Input device	NMOS W/L = 5000/0.6 µm, Id = 4mA
Noise	1140 + 17.6 e-/pF
Gain	3.8 mV/fC
Max. linear charge	450 fC
Class AB Output swing	To power supply - 250 mV
Pulse shape	7^{th} order complex Gaussian, bipolar
Pulse peaking time, 5% - 100%	73 ns
FWHM	340 ns
Max. output loading (3% distortion)	500 Ω, 500 pF
Crosstalk	0.8% adjacent, 0.5% non-adjacent
Power supply	Single +3.3V
Power Dissipation	32.5 mW/chan

Table 1: Preamplifier Shaper Specifications

A CMOS multi-channel ASIC (Figure 2:) was developed for charge amplification and signal shaping. Bipolar shaping and 70ns shaping time were chosen to minimize the effects of noise and pileup. In the 25-channel Preamplifier/Shaper, the NMOS input FET of the preamplifiers, DC feedback circuit and pole-zero compensation circuits were optimized to provide lower parallel and series noise to the front-end signal chain, staying within the allocated power budget [2].

Each ASM-I consists of 4 of the above mentioned ASICs processing signals from 96 cathode strips and its outputs are AC coupled into ASM-II for analog storage, digitization and transmission to off-detector ReadOut Driver (ROD) [3]. Power on ASM-I is regulated by CERN developed LHC-4913 voltage regulator from ST microelectronics. Three stages of Electro-Static Discharge (ESD) protection are provided for each channel.

IV. ASM-II

ASM-II serves total of 192 ASM-I outputs. For analog storage, the HAMAC Switched Capacitor Array (SCA) ASIC [4] is used. This chip originally developed for the ATLAS liquid argon calorimeter, has a separate "muon" mode which allows it to function as a 12-channel, single gain, 144 deep analog memory rather than the 4-channel, tri-gain mode used in the calorimeter. SCA cells are written at 20 MHz and read-out upon level 1 trigger to a 12 bit Analog to Digital Converter (ADC) AD9042 at 6.67 MHz. ASM2MUX, a digital multiplexer ASIC, multiplexes digitized 24 bits from two ADCs at 6.67 MHz into 4 bits out at 40 MHz. Control signals and clocks for SCAs and ADCs are distributed through MC10H116 Positive Emitter Coupled Logic (PECL) buffers, differentially to keep digital noise to a minimum. Custom clock fan-out ASIC designed in the same technology and fabricated on the same wafer as Preamplifier-shaper ASIC and ASM2MUX is used to distribute clocks to ASM2MUXs and on board Giga bit optical links (G-Link). Seven LHC-4913 voltage regulators on ASM-II distribute power to ASM-I and ASM-II. The data from the chambers are transmitted to and control signals for readout of the board are received from off detector ROD over G-Links, consisting of AT HDMP-1022, AT HDMP-1024 and SDX-19-4-1-S optical transceivers. Sparsification, event building, and other tasks involved in resolving the hit co-ordinates with a resolution of approximately 60µm are performed on the ROD [3]. The RODs are also responsible for generating the fast clock and control signals and distributing them to the ASMs, which function as slaves.

V. Power Consumption And Cooling

Each ASM-Pack consumes roughly 60W of power. Major heat dissipating components on the ASM-Pack are the LHC-4913 regulators, HDMP-1022 and 1024 G-Link chipset and AD9042 ADCs. Cooling arrangement consists of two layers of cooling plates. ASM-II is sandwiched between these two plates, and components are actively cooled. Each cooling copper plate is moulded with heat dissipating components impressions for making an optimal contact with them. These components are thermally coupled with the copper plate by thermally conductive gap fillers. A flattened copper tube is glued to the plate by thermally conductive epoxy. Shape of the tube is adjusted and at instances bent to place it on the thermal hot-spots for efficient cooling. These tubes carry cooling water at input temperature of 18^0C. Cooling assemblies for five ASM-Packs for one CSC are connected in

series. Cooling efficiency of such a system for one CSC at water flow rate of 20Gallons/Hour (GPH) is measured to be 85%. Figure 4:shows relation between water flow rate and efficiency of the cooling system for one CSC. Steady state temperature of the hottest component in this chain, which is measured to be 48^0C without water running in the system, is measured to be 25^0C with 20GPH of water flow, indicating effectiveness of the system.

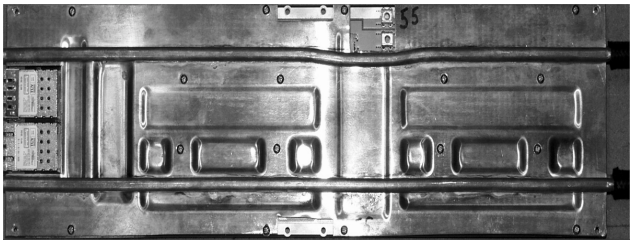

Figure 3: Cooling assembly (top) for ASM-pack

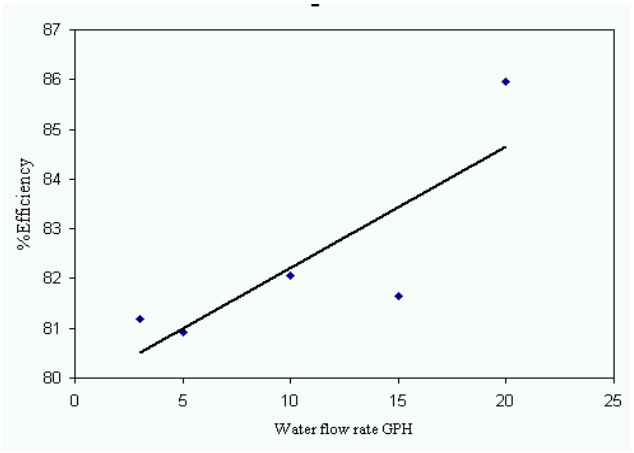

Figure 4: Cooling system efficiency vs Water flow rate in Gallons per hour

VI. RADIATION TOLERANCE

The worst case radiation conditions and RTC criterion for CSC front end electronics are listed in Table 2:. Development of the system architecture centred on single event effects (SEU's) of CMOS logic elements. The design approach adapted to minimize this problem was to remove as much digital hardware from the chamber as possible, specifically the SCA controller. All the COTS and ASIC components were successfully tested to pre-selection levels mentioned in Table 2: for TID, NEIL and SEE/SEU [7].

TEST	SRL	RTC Pre-sel.	RTC Qual.
TID (KRad/10years)	24.3	850.5	425.3
NIEL (1 MeV eq n.cm^{-2}/10years)	7.1x10^{12}	7.1x10^{13}	3.55x10^{13}
SEE/SEU (>20 MeV h.cm^{-2}/10years)	1.52x10^{12}	1.52x10^{13}	7.6x10^{12}

Table 2: Simulated radiation levels (SRL), Pre-selection Radiation Tolerance Criterion (RTC) and RTC Qualification levels.

VII. PRODUCTION TEST RESULTS

Test setup for ASM-I and ASM-II includes custom designed Peripheral Component Interface (PCI) based production test board called PCI ASM Control, Readout And Test (PACRAT) with a LabView based custom interface. Offline analysis is done using Root analysis software. Figure 7: shows baseline subtracted means of maximum amplitude of the positive lobe for half ASM-Pack. ASM-I response is consistently linear for the range of interest. A sample straight line fit to one CSC channel is shown in Figure 6:. Figure 7: shows that noise is around expected value of 0.5fC or 3 ADC counts. Slope is consistent with the decreased strip capacitance with the increasing strip numbers.

CSC front end electronics was tested on a cosmic ray stand as well as X5 beam at CERN. Muon track is seen in the raw data display in Figure 8:.At CERN X5 beam similar chain of electronics along with the ROD was used. Figure 9: depicts resolution of < 66μm obtained using first articles of the production ASM-Pack electronics. [6]

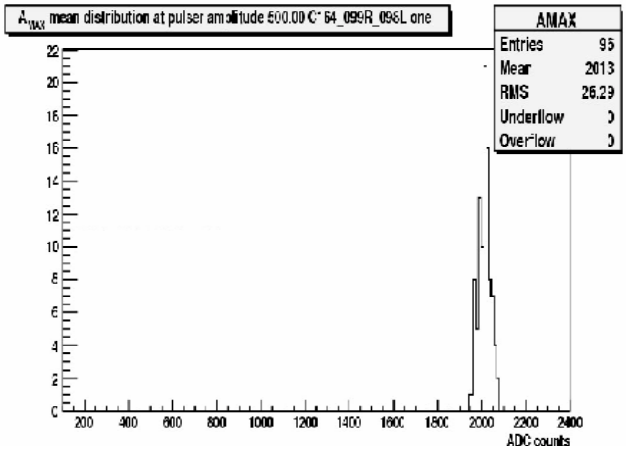

Figure 5: Maximum Amplitude Distribution in ADC Counts for 96 `CSC channels

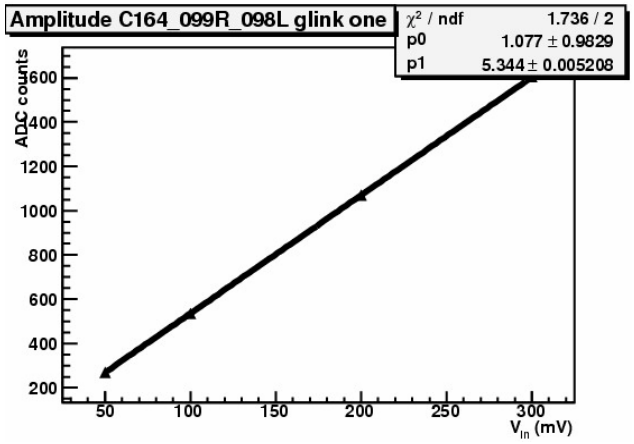

Figure 6: Linearity curve for one CSC Channel

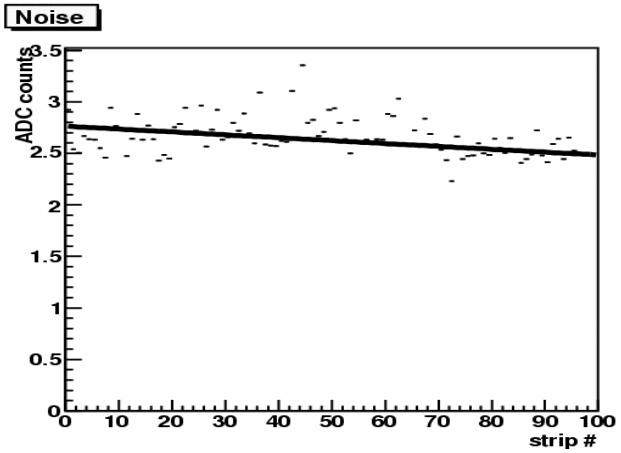

Figure 7: Noise in ADC counts vs. Strip number

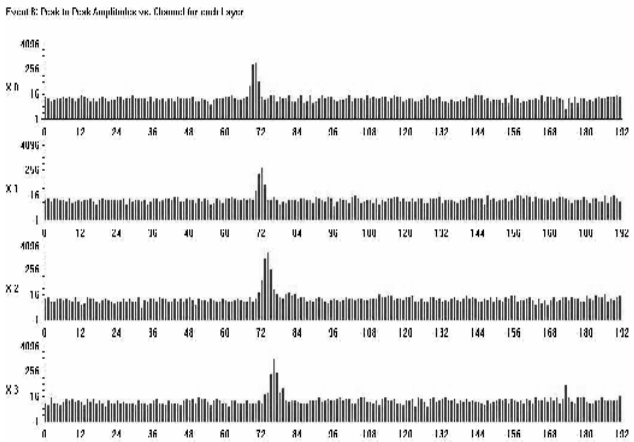

Figure 8: Raw data depicting Muon Track from the CSC Cosmic Stand system integration test

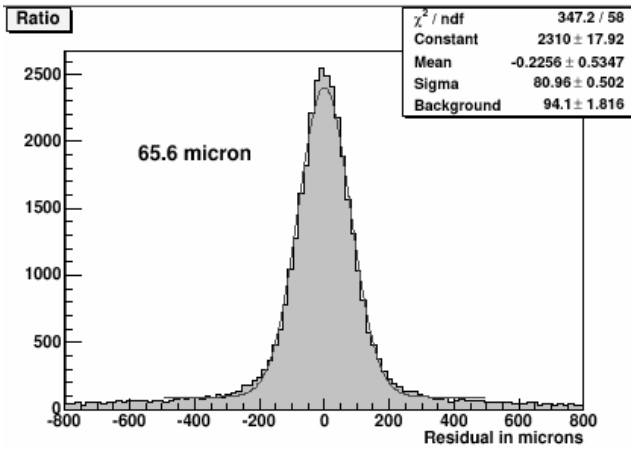

Figure 9: Resolution determined from muon data taken at CERN X5 (Y strip data not included)

VIII. Acknowledgements

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IX. References

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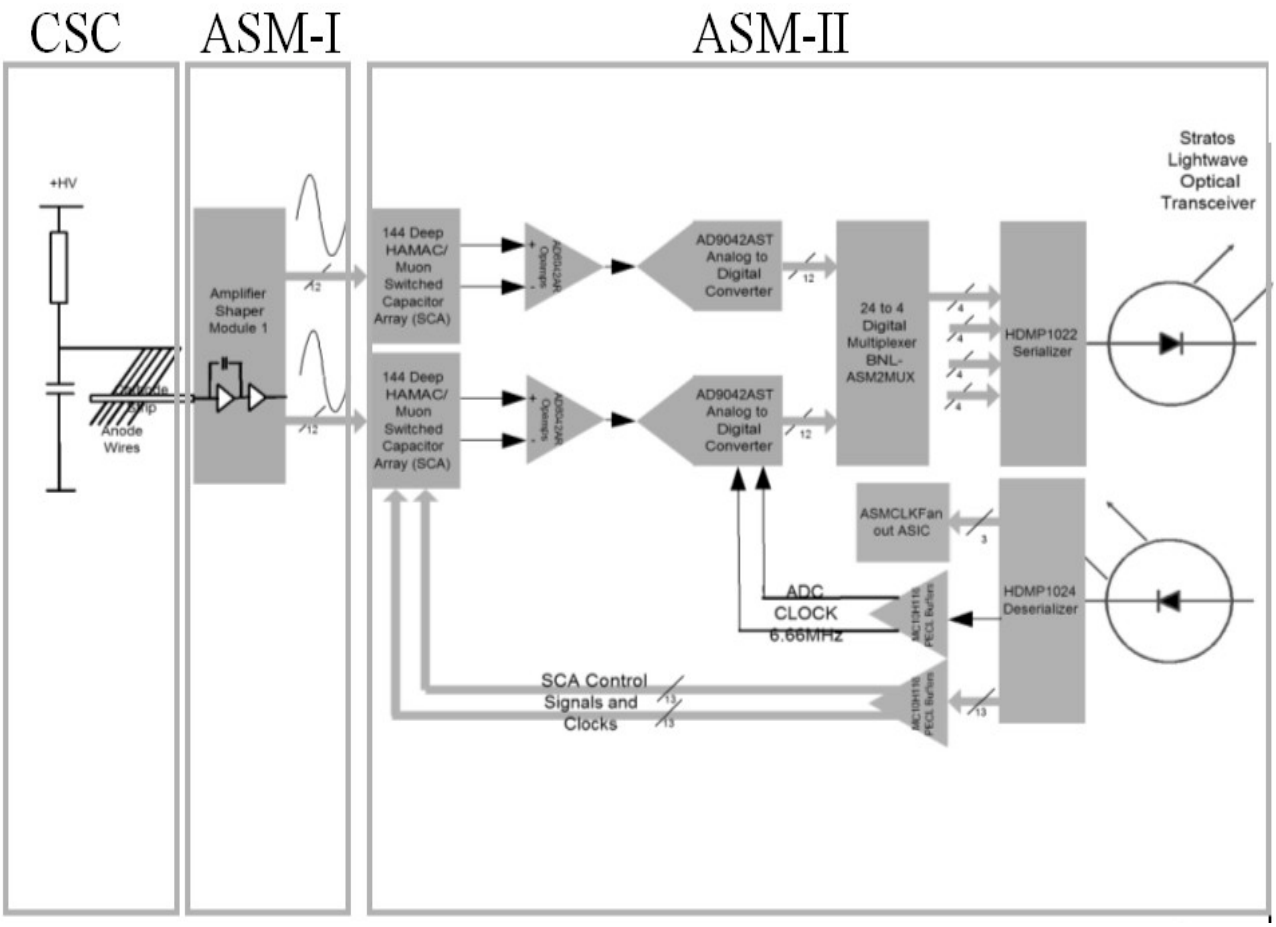

Figure 10: Signal Flow on Cathode Strip Chamber