The 0.25um Token Bit Manager Chip for the CMS Pixel Readout

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Abstract

To coordinate groupings of pixel readout chips, the Token Bit Manager (TBM), has been developed for the CMS experiment.

The TBM will coordinate passing of the readout token around a group readout chips (ROC). In addition it supplies the DAQ with a header and trailer record to facilitate event recognition.

Also present on the same chip is a Control Network Hub, which directs control commands to the TBM, as well as the ROC.

The Latest design details, and resent performance measurements will be presented, including the results of radiation and low temperature testing.

I. Introduction

The Token Bit Manager (TBM) is a critical element of the front-end readout for the CMS pixel detector. It is a custom, mixed-mode, radiation-tolerant IC that controls and orchestrates the readout of a group of pixel ReadOut Chips (ROCs). The TBM is designed to be located on the detector near to the pixel ROCs. In the case of the barrel, they will be mounted on the detector modules and will control the readout of 8 or 16 ROCs depending upon the layer radius. In the case of the forward disks, they will be mounted on the disk blades and will control the readout of 21 or 24 ROCs depending on blade side. [1] A TBM and the group of ROCs that it controls will be connected to a single analog optical link over which the data will be sent to the Front End Driver, a flash ADC module located in the electronics house. The relationship of the TBM to the group of ROCs it controls is shown in Figure 1.

The principle functions of the TBM include the following.

- It will control the readout of the ROCs by initiating a token pass for each incoming Level 1 trigger.
- On each token pass, it will write a header and a trailer word to the data stream.
- The header will contain an 8-bit event number and the trailer will contain 8-bits of error status. These will be transferred as 2-bit analog encoded digital.
- It will distribute the Level 1 triggers, and clock to the ROCs.

Each arriving Level 1 trigger will be placed on a 32-deep stack awaiting its associated token pass. Normally the stack will be empty but is needed to accommodate high burst rates due to either noise, high track density events or trigger bursts.

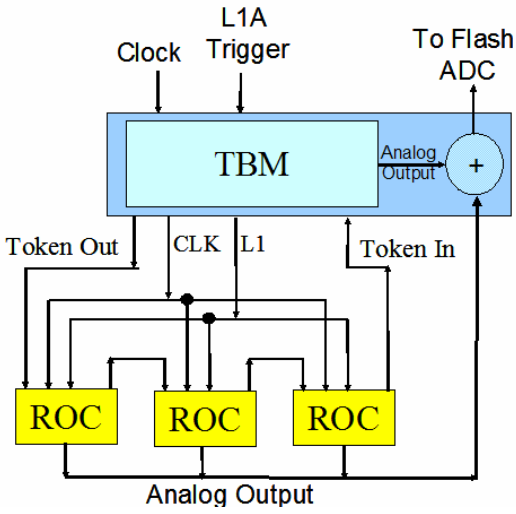


Figure 1: Schematic of a readout chain consisting of a TBM and a group of ROCs.

Since there will be two analog data links per module for the inner two layers of the barrel, the TBMs will be configured as pairs in a Dual TBM Chip. A block diagram of the Dual TBM chip is shown in Figure 2. In addition to two TBMs, this chip also contains a Control Network.

The Hub serves as a port addressing switch for control commands that are sent from the DAQ to the front-end TBMs and ROCs. These control commands will be sent over a digital optical link from a Front End Controller (FEC) in the electronics house to the front-end hubs. The commands will be sent using a serial protocol, similar to the I^2C protocol [2], but modified to run at a speed of 40 MHz. This high speed is mandated by the need to rapidly cycle through a refreshing of

the pixel threshold trim bits that can become corrupted due to single event upsets (SEU). There are four external ports on each Hub for communicating with the ROCs and there is one internal port for communicating with the TBMs within the chip. The first byte of each command will contain a 5-bit hub address and a 3-bit port address. When a Hub is addressed, it selects the addressed port, strips off the byte containing the hub/port address and passes the remainder of the command stream unmodified onto the addressed port. The outputs of the external ports consist of two low voltage differential lines for sending clock and data.

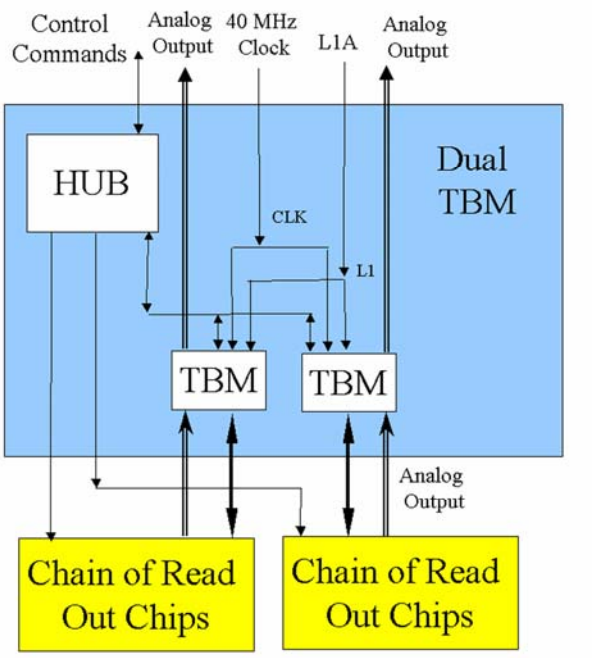


Figure 2: Block diagram of the Dual TBM chip.

II. Early Prototypes

The first TBM was built in an gate array. Originally built to test the basic architecture, the board has proven useful in prototyping design changes, and was used in test beams as recently as 2004.

The TBM02 was produced using the DMILL 0.8um process [3], and received in May, 2002. While this chip preformed as designed, but through miscommunication with the ROC designers, the ROC could not be programmed through the TBM02.

The first 0.25um, IBM process, token bit manager chip, the TBM03, was submitted November, 2003. The TBM03 contained many architectural changes from the DMILL version. These changes included:

- Removal of the independent Serial Clock Line. Serial data would now be clocked using the system clock, saving four differential pairs and the accompanying driver and receiver power consumption.
- Additional trigger sequences were added, providing multiple reset levels, and other fast signalling possibilities from the Front End Controller.
- The addition of analog inputs, and a summing amplifier. Instead of sharing an analog bus with the ROCs, the TBM03 received analog data from several groups of ROCs, combined them together with the its Header and Trailer, and sent this combined signal out to a port card. This allowed for lower trace capacitance, therefore greater analog bandwidth, and lower power consumption, i.e. only the TBM was required to drive signals from the front end to the analog opto-links.

III. Radiation Test

Among the many tests performed on the TBM03, was a radiation/SEU test conducted at the Indiana University Cyclotron Facility.

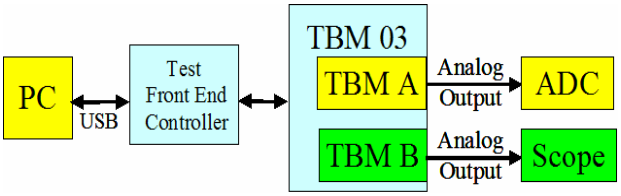


Figure 3: Radiation Test Setup

Using the test setup shown in Figure 3, the TBM was exposed to 200 MeV Protons at a fluxes from 10^7 to 2 x 10^{10} p/cm^2/sec, over 4 hours. The final hour, at maximum flux, was equivalent to 20 LHC days of running at the 4cm barrel layer. The 'A' half of the Dual TBM 03 receiving 7 Level One Accept Triggers (L1A), then reading back the contents of all control registers, and stack contents, the repeating this sequence of a thirty minute run. The 'B' half of the Dual TBM received no L1As and was used to monitor SEU events in the unprotected stack, and look for erroneous token passes. The following results were observed:

Effect	Rate Of Occurrence (Event/LHC Day)
Missing Events	none
Protected Register SEU	1 / 20 LHC days
Trailer Status Bit SEU	1 / 10 LHC days
~30 ns wide, -300 mV Pulse on Analog Output	1/LHC days
Erroneous Token Pass	none
Trailer Sent without Header or Token	1 / 10 LHC days

Table 1: Radiation Test Results

By recording the state of the unprotected stack, before and after each run, the SEU cross-section of the unprotected stack is as follows:

- Transitions from 0 → 1: $(4.2 \pm 0.4) \times 10^{-15}$ cm^2
- Transitions from 1 → 0: $(1 \pm 0.3) \times 10^{-15}$ cm^2

IV. Temperature Test

The TBM is designed to operate at a temperature of approximately -20c (+/- 5c). To test the TBM/ROC response to temperature, a TBM03, connected to a PSI46v1 readout chip, with temperature probes attach to the chip packages. The chips were then set to calibrate a single pixel on the ROC with a trigger rate of 100 kHz. The TBM & ROC were then temperature cycled from room temperature down to -43c & -37c respectively, and returned to room temperature.

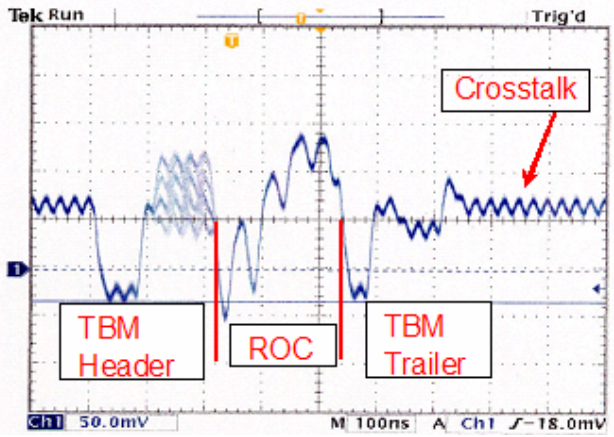


Figure 4: Temperature Test - TBM @-35c, ROC@-31c

As anticipated, adjustments to the comparator threshold on the ROC, and the output gain settings of both chips were required as the temperature was decreased. This can be attributed to the effect of temperature on the internal voltage references of both chips. The output gain decreased 0.3% per degree C over the 65 degree temperature range.

Despite crosstalk from nearby clock lines (see Figure 4), the TBM03 was also used by several groups to perform ROC/Sensor behaviour studies, and in to control ROC chips in test beams conducted at Fermi National Lab.

V. TBM04

In addition to minor logic changes, and an improved analog output driver, the TBM04 contained many improvements designed to minimize the crosstalk both within the token bit manager, and without. The TBM pin order was rearranged, to minimize crosstalk at the analog inputs, and new differential current drivers replaced the low voltage differential drivers to reduce any crosstalk present on the cable connecting the front end to the port card containing the opto-links to the Front End Control (FEC). These efforts proved very effective, as shown in figure 5.

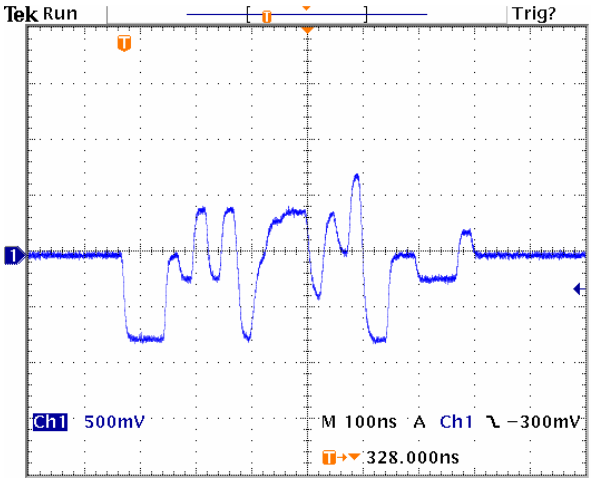


Figure 5: TBM04 controlling a PSI46v2 Readout Chip

VI. TBM05

While the TBM04 analog section was an improvement, over its predecessor, the bandwidth and linearity of the analog chain (shown in figure 6) were still below that needed to accurately digitize the signal in the DAQ.

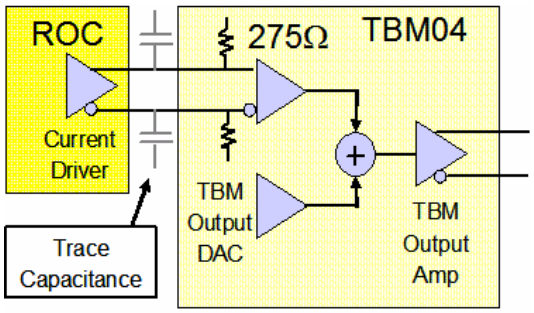


Figure 6: TBM04 Analog Block Diagram

The time constant (τ) of the TBM Header/Trailer was 4 ns, fast enough to reach a final value at the 40MHz readout speed. However the combined time constant of the ROC signal, measured at the output of the TBM was 6.3 ns. This problem was found to be the combination of the trace capacitance of the printed circuit board and the input resistor inside the TBM. Minimizing the PCB capacitance, along with decreasing the resistor from 275Ω τǫ150Ω would improve the system bandwidth.

Correcting the linearity would require modifying one stage of the internal amplifiers to prevent it from saturating at high signal levels. This would also permit the internal gain to be increased to compensate for the gain lost when the input resistance was lowered.

Secondly, data taken with the TBM03, at the Fermilab test beam (after the TBM04 submitted), revealed some minor improvements were needed in the TBM stack counter. It was also decided to reduce the maximum number of triggers sent to the ROC from sixteen to fifteen, as a safety precaution.

The TBM05 submission was received in August. 2005, and testing is well underway at Rutgers, PSI, and Fermilab.

The time constant of the TBM output is now 3.7ns, and the time constant for the ROC signal, at the TBM output is 5 ns. This will allow both signals to reach a final value at 40MHz.

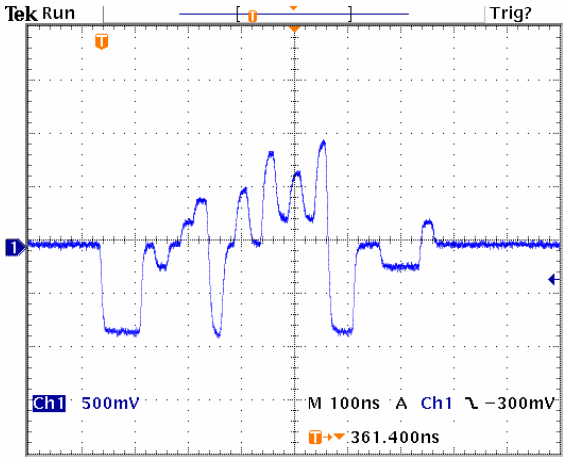


Figure 7: TBM05 controlling a PSI46v2 Readout Chip

Figure 8 shows the output of a TBM chip for a 1 MHz input trigger rate, far in excess of the expected to be 30 KHz with possible brief bursts to 100 KHz. In this figure, multiple traces for several outputs have been overlaid. The TBM clearly is able to function at this trigger rate, and the eye pattern formed by the overlapping of the 256 event number illustrates sufficient level separation and linearity.

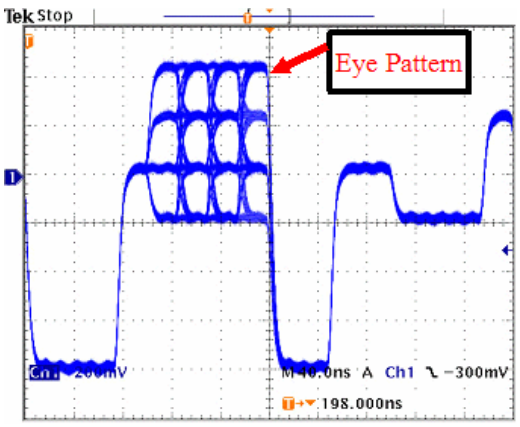
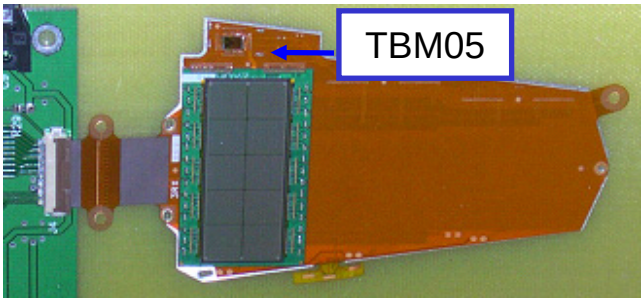


Figure 8: Performance of Dual TBM 05 chip at an input trigger rate of 1 MHz. Outputs of several events are overlaid.

At Fermilab, the TBM05 has been mounted on the new HDI layout, and is being used for tests of the HDI layout, in preparation for a full blade system test.



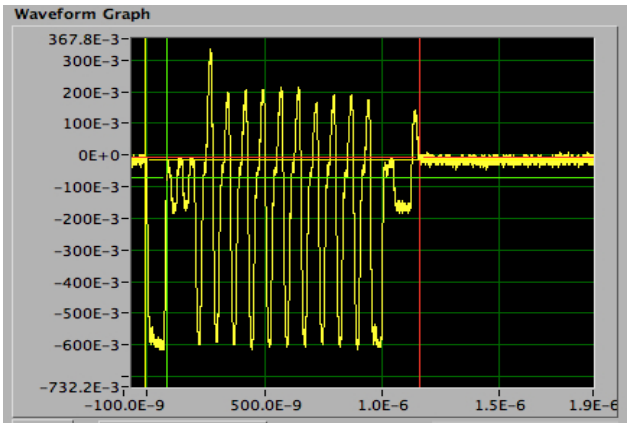


Figure 9: Forward Pixel HDI, with TBM05 and 10 ROC placquette under test

At Paul Scherrer Institute (PSI) the TBM04 & TBM05 were successfully used in a 300 MeV/c π+ test beam with a flux up to up to 100 MHz/cm^2 at PSI to record hundreds of thousands of events.

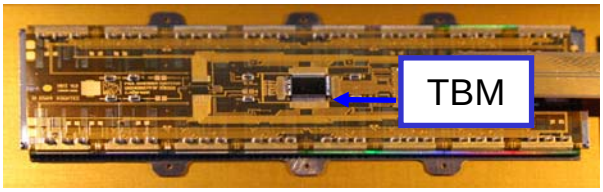


Figure 10: Barrel module with 16 Readout chips and TBM.

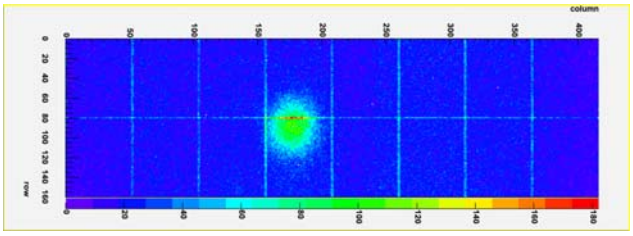


Figure 11: Plot of 90 k events, at a flux of 47 MHz/cm2, and a trigger rate of 18 kHz [4]

It was hoped that the TBM05 would serve as the production run for the CMS pixel detector, however a flaw has been discovered. When changes were made to the analog section of the TBM, an older version of the gain setting register block was used. This older block lacked an inverter on the reset line (see figure 12). This resulted in the gain settings continuously forced into a nominal position.

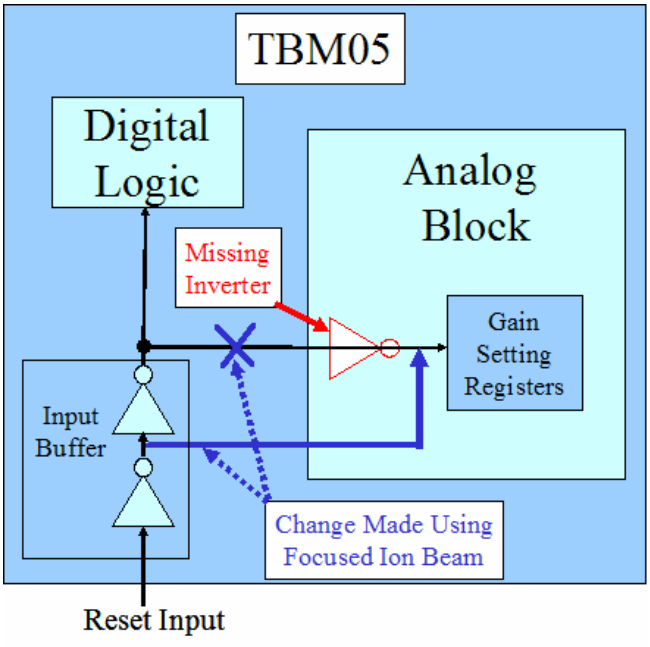


Figure 12: Block Diagram showing missing inverter.

While this nominal setting is perfectly adequate for bench tests and test beam work, radiation damage is expected to alter amplifier gains. For this reason, the potential for gain adjustment is imperative. Using a focused ion beam, it has been verified that a simple modification to the Metal 1 layer of the TBM05 corrects this problem. Since under normal circumstances IBM sets six wafers aside during the production process, just before the metal layers are applied, it is possible to remake the Metal 1 mask. This "Respin" of the MPW15 run would produce the eleven hundred TBM05a chips needed for the CMS Pixel Detector.

VII. Conclusions

The TBM is functional in a high radiation environment and at low temperatures, well below design specifications. It has been extensively tested by multiple groups and used successfully to test ROC/Sensor combinations in both Fermilab & PSI test beams. It is therefore reasonable to expect that the TBM05a will be the production run of the TBM for CMS Pixels

VIII. References

[1] "The CMS Tracker Technical Design Report", CMS/LHCC 98-6.

[2] "I ^{2} C Bus Specification", Application Note, Philips - Signetics, January (1992).

[3] M. Dentan et al., "Dmill (Durci Mixte Sur Isolant Logico-Lineaire): A Mixed Analog-Digital Radiation Hard Technology For High Energy Physics Electronics", Nucl. Phys. Proc. Suppl. 32, 530 (1998).

[4] W. Erdmann, "Beam Test of CMS Pixel Barrel Modules", Pixel 2005, International Workshop on Semiconductor Pixel Detectors for Particles and X-Rays, , Sept. 2005